PROGRAMMABLE 2-PLL VCXO CLOCK SYNTHESIZER WITH 1.8-V, 2.5-V and 3.3-V LVCMOS OUTPUTS

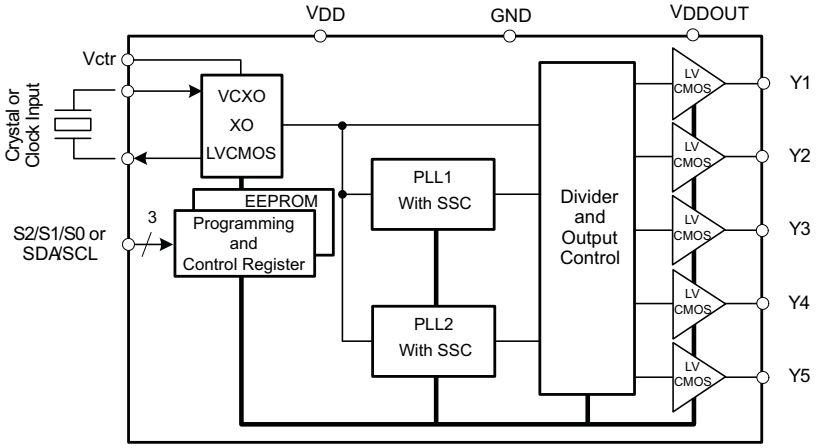
Check for Samples: CDCE925, CDCEL925

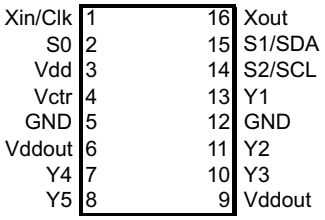
FEATURES

- Member of Programmable Clock Generator Family
  - CDCE913/CDCEL913: 1-PLL, 3 Outputs
  - *CDCE925/CDCEL925: 2-PLL, 5 Outputs*
  - CDCE937/CDCEL937: 3-PLL, 7 Outputs
  - CDCE949/CDCEL949: 4-PLL, 9 Outputs
- Flexible Clock Driver
  - Three User-Definable Control Inputs [S0/S1/S2] e.g., SSC Selection, Frequency Switching, Output Enable or Power Down
  - Programmable SSC Modulation
  - Enables 0-PPM Clock Generation
  - Generates Common Clock Frequencies Used With Texas Instruments DaVinci™, OMAP™, DSPs
  - Generates Highly Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, *Bluetooth*®, WLAN, Ethernet™, and GPS
- In-System Programmability and EEPROM
  - Serial Programmable Volatile Register
  - Nonvolatile EEPROM to Store Customer Settings
- Flexible Input Clocking Concept
  - External Crystal: 8 MHz to 32 MHz
  - On-Chip VCXO: Pull Range ±150 ppm
  - Single-Ended LVCMOS up to 160 MHz
- Selectable Output Frequency up to 230 MHz
- Low-Noise PLL Core
  - PLL Loop Filter Components Integrated
  - Low Period Jitter (Typ 60 ps)
- 1.8-V Device Power Supply
- Separate Output Supply Pins
  - CDCE925: 3.3 V and 2.5 V
  - CDCEL925: 1.8 V
- Temperature Range –40°C to 85°C
- Packaged in TSSOP
- Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock™)

APPLICATIONS

- D-TV, STB, IP-STB, DVD-Player, DVD-Recorder, Printer





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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CDCE925 and CDCEL925 are modular PLL-based low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. They generate up to five output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using up to two independent configurable PLLs.

The CDCEx925 has a separate output supply pin, V_{DDOUT}, which is 1.8 V for CDCEL925 and 2.5 V to 3.3 V for CDCE925.

The input accepts an external crystal or LVCMOS clock signal. In case of a crystal input, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 pF to 20 pF. Additionally, an on-chip VCXO is selectable which allows synchronization of the output frequency to an external control signal, that is, PWM signal.

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, *Bluetooth*, Ethernet, GPS) or interface (USB, IEEE1394, memory stick) clocks from a 27-MHz reference input frequency, for example.

All PLLs support SSC (spread-spectrum clocking). SSC can be center-spread or down-spread clocking, which is a common technique to reduce electromagnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

The device supports nonvolatile EEPROM programming for easy customization of the device in the application. It is preset to a factory default configuration and can be re-programmed to a different application configuration before it goes onto the PCB or re-programmed by in-system programming. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

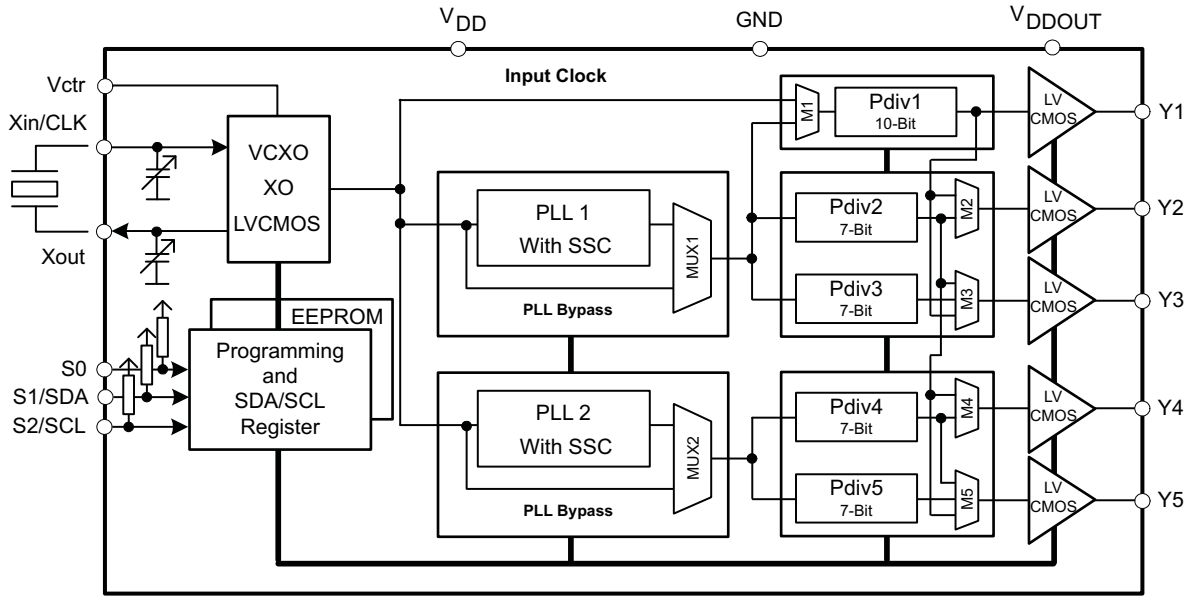
Three, free programmable control inputs, S0, S1, and S2, can be used to select different frequencies, or change the SSC setting for lowering EMI, or other control features like outputs disable to low, outputs in high-impedance state, power down, PLL bypass, etc.).

The CDCx925 operates in a 1.8-V environment. It operates in a temperature range of –40 °C to 85 °C.

Terminal Functions for CDCE925, CDCEL925

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Y1, Y2, ... Y5	7, 8, 10, 11, 13	O	LVCMOS outputs
Xin/CLK	1	I	Crystal oscillator input or LVCMOS clock Input (selectable via SDA/SCL bus)
Xout	16	O	Crystal oscillator output (leave open or pull up when not used)
V_{Ctrl}	4	I	VCXO control voltage (leave open or pull up when not used)
V_{DD}	3	Power	1.8-V power supply for the device
V_{DDOUT}	6, 9	Power	**CDCEL925**: 1.8-V supply for all outputs
			CDCE925: 3.3-V or 2.5-V supply for all outputs
GND	5, 12	Ground	Ground
S0	2	I	User-programmable control input S0; LVCMOS inputs; internal pullup
SDA/S1	15	I/O or I	**SDA:** Bidirectional serial data input/output (default configuration), LVCMOS; internal pullup **S1:** User-programmable control input; LVCMOS inputs; internal pullup
SCL/S2	14	I	**SCL:** Serial clock input (default configuration), LVCMOS; internal pullup **S2:** User-programmable control input; LVCMOS inputs; internal pullup

FUNCTIONAL BLOCK DIAGRAM for CDCE925, CDCEL925



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 2.5	V
V_I	Input voltage range(2) (3)	–0.5 to V_{DD} + 0.5	V
V_O	Output voltage range(2)	–0.5 to V_{DD} + 0.5	V
I_I	Input current (V_I < 0, V_I > V_{DD})	20	mA
I_O	Continuous output current	50	mA
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) SDA and SCL can go up to 3.6V as stated in the *Recommended Operating Conditions* table.

PACKAGE THERMAL RESISTANCE for TSSOP (PW) PACKAGE(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		AIRFLOW (lfm)	TSSOP16 °C/W
T_{JA}	Thermal resistance, junction-to-ambient	0	101
		150	85
		200	84
		250	82
		500	74
T_{JC}	Thermal resistance, junction-to-case	—	42
T_{JB}	Thermal resistance, junction-to-board	—	64
$R_{\theta JT}$	Thermal resistance, junction-to-top	—	1.0
$R_{\theta JB}$	Thermal resistance, junction-to-bottom	—	58

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.7	1.8	1.9	V
V_{DDOUT}	Output Yx supply voltage for CDCE925	2.3		3.6	
	Output Yx supply voltage for CDCEL925	1.7		1.9	V
V_{IL}	Low-level input voltage LVCMOS			0.3 V_{DD}	V
V_{IH}	High-level input voltage LVCMOS	0.7 V_{DD}			V
$V_{I(thresh)}$	Input voltage threshold LVCMOS		0.5 V_{DD}		V
$V_{I(S)}$	Input voltage range S0	0		1.9	V
	Input voltage range S1, S2, SDA, SCL; $V_{(Ithresh)}$ = 0.5 V_{DD}	0		3.6	
$V_{I(CLK)}$	Input voltage range CLK	0		1.9	V
I_{OH} /I_{OL}	Output current (V_{DDOUT} = 3.3 V)			±12	mA
	Output current (V_{DDOUT} = 2.5 V)			±10	
	Output current (V_{DDOUT} = 1.8 V)			±8	
C_L	Output load LVCMOS			15	pF
T_A	Operating free-air temperature	–40		85	°C

RECOMMENDED CRYSTAL/VCXO SPECIFICATIONS(1)

		MIN	NOM	MAX	UNIT
f_{Xtal}	Crystal input frequency range (fundamental mode)	8	27	32	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling range (0 V ≤ V_{Ctrl} ≤ 1.8 V)(2)	±120	±150		ppm
V_{Ctrl}	Frequency control voltage	0		V_{DD}	V
C_0/C_1	Pullability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration, and crystal recommendation, see application report (SCAA085).
(2) Pulling range depends on crystal-type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ±120 ppm applies for crystal listed in the application report (SCAA085).

EEPROM SPECIFICATION

		MIN	TYP	MAX	UNIT
EEcyc	Programming cycles of EEPROM	100	1000		cycles
EEret	Data retention	10			years

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature

			MIN	NOM	MAX	UNIT
CLK_IN REQUIREMENTS						
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0		160	MHz
		PLL mode	8		160	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
$duty_{CLK}$	Duty cycle CLK at V_{DD} / 2		40%		60%	

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
SDA/SCL TIMING REQUIREMENTS (see Figure 12)						
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{su(START)}$	START setup time (SCL high before SDA low)	4.7		0.6		µs
$t_{h(START)}$	START hold time (SCL low after SDA low)	4		0.6		µs
$t_{w(SCLL)}$	SCL low-pulse duration	4.7		1.3		µs
$t_{w(SCLH)}$	SCL high-pulse duration	4		0.6		µs
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	0	3.45	0	0.9	µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
t_r	SCL/SDA input rise time		1000		300	ns
t_f	SCL/SDA input fall time		300		300	ns
$t_{su(STOP)}$	STOP setup time	4		0.6		µs
t_{BUS}	Bus free time between a STOP and START condition	4.7		1.3		µs

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
OVERALL PARAMETER							
I_{DD}	Supply current (see Figure 3)	All outputs off, f_{CLK} = 27 MHz, f_{VCO} = 135 MHz; f_{OUT} = 27 MHz	All PLLS on		20		mA
			Per PLL		9		
I_{DDOUT}	Supply current (see Figure 4 and Figure 5)	No load, all outputs on, f_{OUT} = 27 MHz	CDCE925 V_{DDOUT} = 3.3 V		2		mA
			CDCEL925 V_{DDOUT} = 1.8 V		1		
I_{DDPD}	Power-down current. Every circuit powered down except SDA/SCL	f_{IN} = 0 MHz,	V_{DD} = 1.9 V		30		µA
V_{PUC}	Supply voltage V_{DD} threshold for power-up control circuit			0.85		1.45	V
f_{VCO}	VCO frequency range of PLL			80		230	MHz
f_{OUT}	LVCMOS output frequency	CDCE(L)925 V_{DDOUT} = 1.8 V		230			MHz
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7 V; I_S = –18 mA				–1.2	V
I_I	LVCMOS input current	V_I = 0 V or V_{DD}; V_{DD} = 1.9 V				±5	µA
I_{IH}	LVCMOS input current for S0/S1/S2	V_I = V_{DD}; V_{DD} = 1.9 V				5	µA
I_{IL}	LVCMOS Input current for S0/S1/S2	V_I = 0 V; V_{DD} = 1.9 V				–4	µA
C_I	Input capacitance at Xin/Clk	V_{IClk} = 0 V or V_{DD}			6		pF
	Input capacitance at Xout	V_{IXout} = 0 V or V_{DD}			2		
	Input capacitance at S0/S1/S2	V_{IS} = 0 V or V_{DD}			3		
CDCE925 - LVCMOS PARAMETER FOR V_{DDOUT} = 3.3 V – MODE							
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 3 V, I_{OH} = –0.1 mA		2.9			V
		V_{DDOUT} = 3 V, I_{OH} = –8 mA		2.4			
		V_{DDOUT} = 3 V, I_{OH} = –12 mA		2.2			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 3 V, I_{OL} = 0.1 mA				0.1	V
		V_{DDOUT} = 3 V, I_{OL} = 8 mA				0.5	
		V_{DDOUT} = 3 V, I_{OL} = 12 mA				0.8	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass			3.2		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 3.3 V (20%–80%)			0.6		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3			50	70	ps
		2 PLL switching, Y2-to-Y5			90	130	
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3			60	100	ps
		2 PLL switching, Y2-to-Y5			100	160	
$t_{sk(o)}$	Output skew (4)	f_{OUT} = 50 MHz; Y1-to-Y3				70	ps
		f_{OUT} = 50 MHz; Y2-to-Y5				150	
odc	Output duty cycle (5)	f_{VCO} = 100 MHz; Pdiv = 1		45%		55%	
CDCE925 – LVCMOS PARAMETER for V_{DDOUT} = 2.5 V – Mode							
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 2.3 V, I_{OH} = –0.1 mA		2.2			V
		V_{DDOUT} = 2.3 V, I_{OH} = –6 mA		1.7			
		V_{DDOUT} = 2.3 V, I_{OH} = –10 mA		1.6			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 2.3 V, I_{OL} = 0.1 mA				0.1	V
		V_{DDOUT} = 2.3 V, I_{OL} = 6 mA				0.5	
		V_{DDOUT} = 2.3 V, I_{OL} = 10 mA				0.7	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass			3.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 2.5 V (20%–80%)			0.8		ns

(1) All typical values are at respective nominal V_{DD}.
(2) 10,000 cycles
(3) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 135 MHz, f_{OUT} = 27 MHz. f_{OUT} = 3.072 MHz or input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz. f_{OUT} = 16.384 MHz, f_{OUT} = 25 MHz, f_{OUT} = 74.25 MHz, f_{OUT} = 48 MHz
(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider, data sampled on rising edge (t_r).
(5) odc depends on output rise- and fall time (t_r/t_f);

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{jit(cc)}$	Cycle-to-cycle jitter (6) (7)	1 PLL switching, Y2-to-Y3		50	70	ps
		2 PLL switching, Y2-to-Y5		90	130	
$t_{jit(per)}$	Peak-to-peak period jitter (7)	1 PLL switching, Y2-to-Y3		60	100	ps
		2 PLL switching, Y2-to-Y5		100	160	
$t_{sk(o)}$	Output skew (8)	f_{OUT} = 50 MHz; Y1-to-Y3			70	ps
		f_{OUT} = 50 MHz; Y2-to-Y5			150	
odc	Output duty cycle (9)	f_{VCO} = 100 MHz; Pdiv = 1	45%		55%	
CDCEL925 — LVCMOS PARAMETER for V_{DDOUT} = 1.8 V – Mode						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 1.7 V, I_{OH} = –0.1 mA	1.6			V
		V_{DDOUT} = 1.7 V, I_{OH} = –4 mA	1.4			
		V_{DDOUT} = 1.7 V, I_{OH} = –8 mA	1.1			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 1.7 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 1.7 V, I_{OL} = 4 mA			0.3	
		V_{DDOUT} = 1.7 V, I_{OL} = 8 mA			0.6	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		2.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 1.8 V (20%–80%)		0.7		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter (6) (7)	1 PLL switching, Y2-to-Y3		80	110	ps
		2 PLL switching, Y2-to-Y5		130	200	
$t_{jit(per)}$	Peak-to-peak period jitter (10)	1 PLL switching, Y2-to-Y3		100	130	ps
		2 PLL switching, Y2-to-Y5		150	220	
$t_{sk(o)}$	Output skew (11)	f_{OUT} = 50 MHz; Y1-to-Y3			50	ps
		f_{OUT} = 50 MHz; Y2-to-Y5			110	
odc	Output duty cycle (12)	f_{VCO} = 100 MHz; Pdiv = 1	45%		55%	
SDA/SCL PARAMETER						
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7 V; I_I = –18 mA			–1.2	V
I_{IH}	SCL and SDA input current	$V_I = V_{DD}$; V_{DD} = 1.9 V			±10	µA
V_{IH}	SDA/SCL input high voltage(13)		0.7 V_{DD}			V
V_{IL}	SDA/SCL input low voltage(13)				0.3 V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3 mA V_{DD} = 1.7 V			0.2 V_{DD}	V
C_I	SCL/SDA Input capacitance	V_I = 0 V or V_{DD}		3	10	pF

(6) 10,000 cycles
(7) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 135 MHz, f_{OUT} = 27 MHz. f_{OUT} = 3.072 MHz or input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz. f_{OUT} = 16.384 MHz, f_{OUT} = 25 MHz, f_{OUT} = 74.25 MHz, f_{OUT} = 48 MHz
(8) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider, data sampled on rising edge (t_r).
(9) odc depends on output rise- and fall time (t_r/t_f);
(10) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 135 MHz, f_{OUT} = 27 MHz. f_{OUT} = 3.072 MHz or input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz. f_{OUT} = 16.384 MHz, f_{OUT} = 25 MHz, f_{OUT} = 74.25 MHz, f_{OUT} = 48 MHz
(11) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider, data sampled on rising edge (t_r).
(12) odc depends on output rise- and fall time (t_r/t_f);
(13) SDA and SCL pins are 3.3-V tolerant.

PARAMETER MEASUREMENT INFORMATION

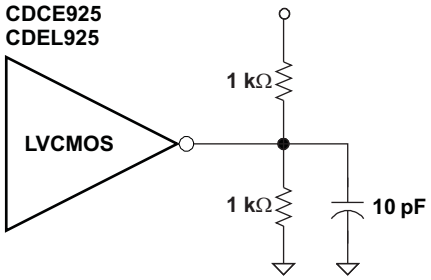


Figure 1. Test Load

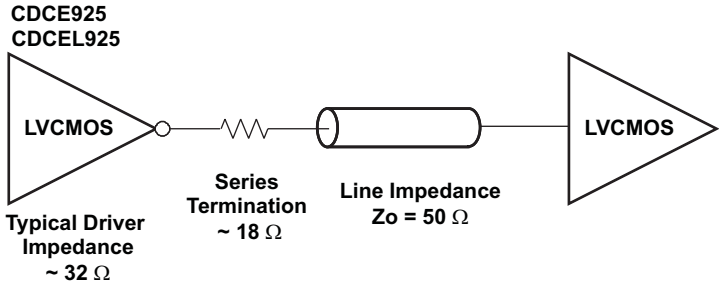


Figure 2. Test Load for 50-Ω Board Environment

TYPICAL CHARACTERISTICS

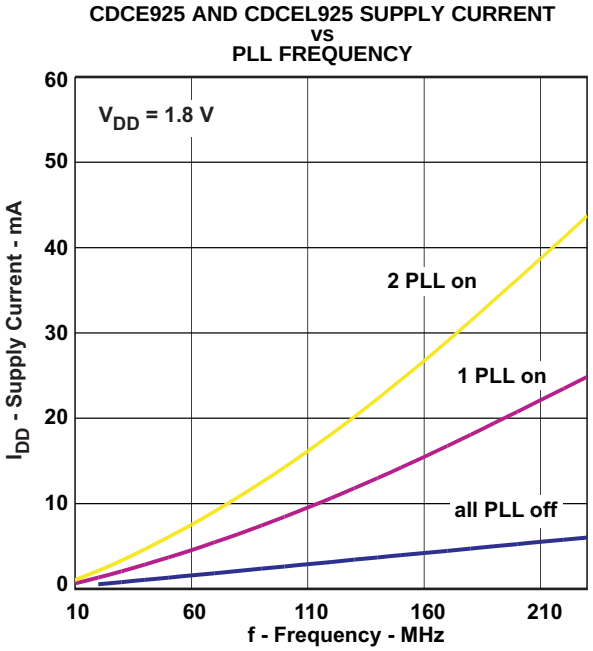


Figure 3.

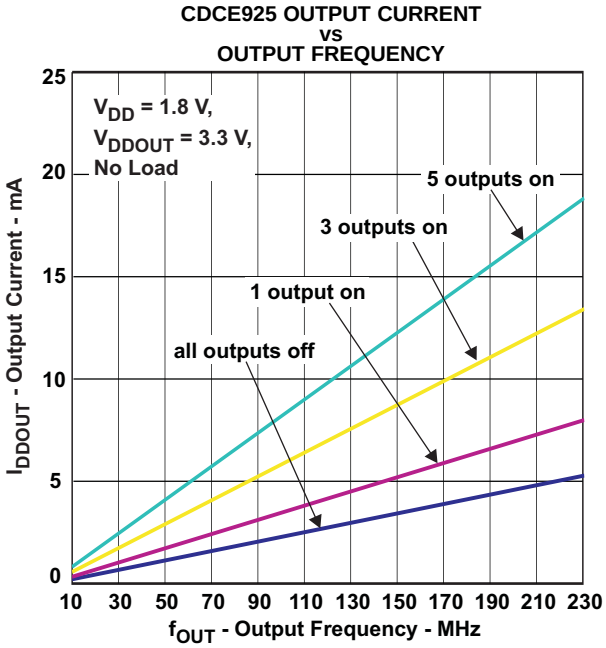


Figure 4.

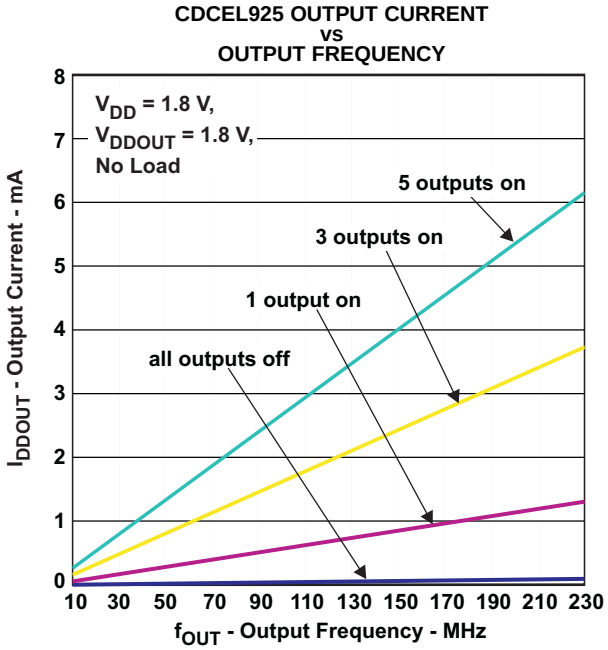


Figure 5.

APPLICATION INFORMATION

CONTROL TERMINAL SETTING

The CDCE925/CDCEL925 has three user-definable control terminals (S0, S1, and S2) which allow external control of device settings. They can be programmed to any of the following settings:

- Spread spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power-down control

The user can predefine up to eight different control settings. Table 1 and Table 2 explain these settings.

Table 1. Control Terminal Definition

External Control Bits	PLL1 Setting			PLL2 Setting			Y1 Setting
Control function	PLL frequency selection	SSC selection	Output Y2/Y3 selection	PLL frequency selection	SSC selection	Output Y4/Y5 selection	Output Y1 and power-down selection

Table 2. PLL Setting (Can Be Selected for Each PLL Individual)(1)

SSC SELECTION (CENTER/DOWN)				
SSCx [3-Bits]			Center	Down
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	–0.25%
0	1	0	±0.5%	–0.5%
0	1	1	±0.75%	–0.75%
1	0	0	±1.0%	–1.0%
1	0	1	±1.25%	–1.25%
1	1	0	±1.5%	–1.5%
1	1	1	±2.0%	–2.0%
FREQUENCY SELECTION(2)				
FSx			**FUNCTION**	
0			Frequency0	
1			Frequency1	
OUTPUT SELECTION(3) (Y2 ... Y5)				
YxYx			**FUNCTION**	
0			State0	
1			State1	

(1) Center/down-spread, Frequency0/1 and State0/1 are user-definable in the PLLx configuration register.
(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.
(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, high-impedance state, low, or active

Table 3. Y1 Setting(1)

Y1 SELECTION	
Y1	**FUNCTION**
0	State 0
1	State 1

(1) State0 and State1 are user definable in the generic configuration register and can be power down, high-impedance state, low, or active.

SDA/S1 and SCL/S2 pins of the CDCE925/CDCEL925 are dual-function pins. In the default configuration, they are predefined as the SDA/SCL serial programming interface. They can be programmed to control pins (S1/S2) by setting the relevant bits in the EEPROM. Note that the changes of the bits in the control register (bit [6] of byte 02h) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL).

S0 is not a multi-use pin; it is a control pin only.

DEFAULT DEVICE SETTING

The internal EEPROM of CDCE925/CDCEL925 is preconfigured as shown in Figure 6. The input frequency is passed through the output as a default. This allows the device to operate in default mode without the extra production step of programming it. The default setting appears after power is supplied or after a power-down/up sequence until it is reprogrammed by the user to a different application configuration. A new register setting is programmed via the serial SDA/SCL interface.

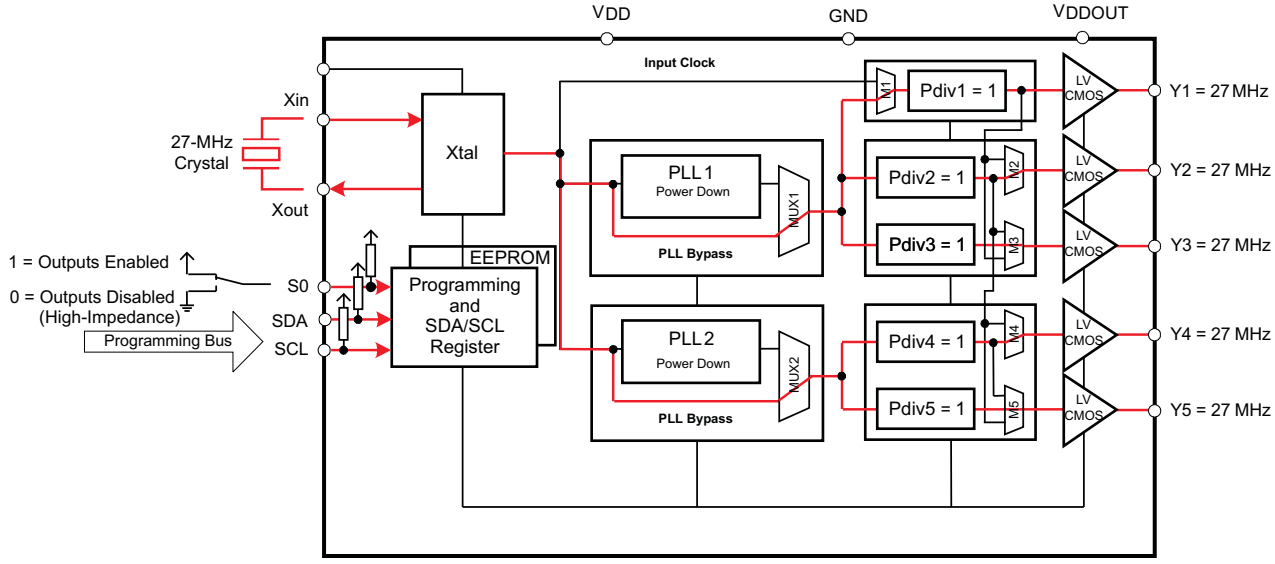


Figure 6. Preconfiguration of CDCE925/CDCEL925 Internal EEPROM

Table 4 shows the factory default setting for the control terminal register (external control pins). Note that even though eight different register settings are possible, in default configuration, only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in the default mode.

Table 4. Factory Default Settings for Control Terminal Register(1)

			Y1	PLL1 Settings			PLL2 Settings		
External Control Pins			Output Selection	Frequency Selection	SSC Selection	Output Selection	Frequency Selection	SSC Selection	Output Selection
S2	*S1*	**S0**	**Y1**	*FS1*	*SSC1*	**Y2Y3**	*FS2*	*SSC2*	**Y4Y5**
SCL (I2C)	SDA (I^2C)	**0**	**High-impedance state**	f_{VCO1_0}	Off	**High-impedance state**	f_{VCO2_0}	Off	**High-impedance state**
SCL (I2C)	SDA (I^2C)	**1**	**Enabled**	f_{VCO1_0}	Off	**Enabled**	f_{VCO2_0}	Off	**Enabled**

(1) S1 is SDA and S2 is SCL in default mode or when programmed (SPICON bit 6 of register 2 set to 0). They do not have any control-pin function but they are internally interpreted as if S1 = 0 and S2 = 0. S0, however, is a control pin which in the default mode switches all outputs ON or OFF (as previously predefined).

SDA/SCL SERIAL INTERFACE

This section describes the SDA/SCL interface of the CDCE925/CDCEL925 device. The CDCE925/CDCEL925 operates as a slave device of the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I^2C specification. It operates in the standard-mode transfer (up to 100 kbit/s) and fast-mode transfer (up to 400 kbit/s) and supports 7-bit addressing.

The SDA/S1 and SCL/S2 pins of the CDCE925/CDCEL925 are dual-function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be reprogrammed as general-purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, byte 02h, bit [6].

DATA PROTOCOL

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most-significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of bytes read out are defined by byte count in the generic configuration register. At the *Block Read* instruction, all bytes defined in the byte count must be read out to finish the read cycle correctly.

Once a byte has been sent, it is written into the internal register and is effective immediately. This applies to each transferred byte regardless of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM write cycle is initiated, the internal SDA registers are written into the EEPROM. During this write cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read out during the programming sequence (*Byte Read* or *Block Read*). The programming status can be monitored by *EEPIP*, byte 01h–bit 6.

The offset of the indexed byte is encoded in the command code, as described in Table 5.

Table 5. Slave Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1(1)	A0(1)	R/$\overline{W}$
CDCE913/CDCEL913	1	1	0	0	1	0	1	1/0
CDCE925/CDCEL925	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**1/0**
CDCE937/CDCEL937	1	1	0	1	1	0	1	1/0
CDCE949/CDCEL949	1	1	0	1	1	0	0	1/0

(1) Address bits A0 and A1 are programmable via the SDA/SCL bus (byte 01, bit [1:0]. This allows addressing up to four devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

COMMAND CODE DEFINITION

Table 6. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte offset for *Byte Read*, *Block Read*, *Byte Write* and *Block Write* operations.

Generic Programming Sequence

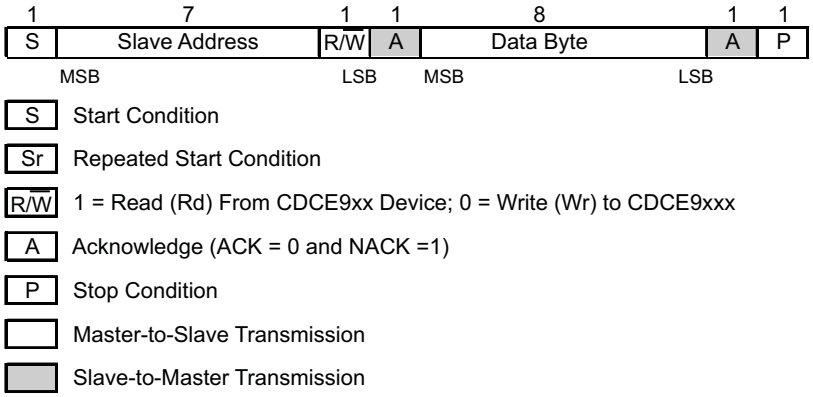


Figure 7. Generic Programming Sequence

Byte Write Programming Sequence

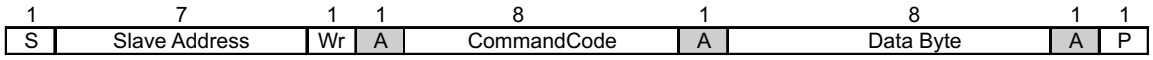


Figure 8. Byte Write Protocol

Byte Read Programming Sequence

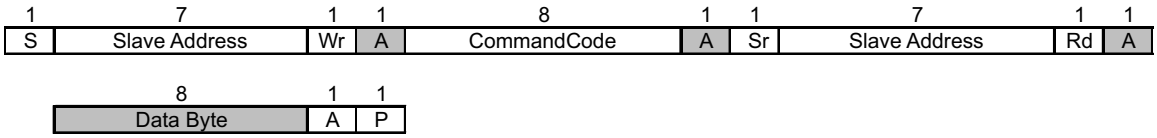
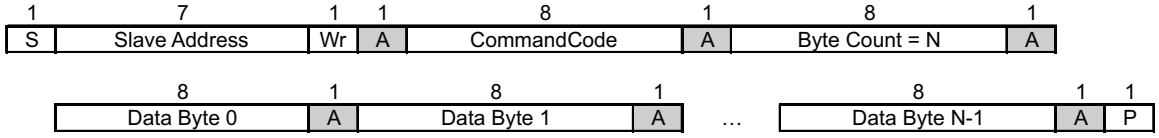


Figure 9. Byte Read Protocol

Block Write Programming Sequence



(1) Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and should not be overwritten.

Figure 10. Block Write Protocol

Block Read Programming Sequence

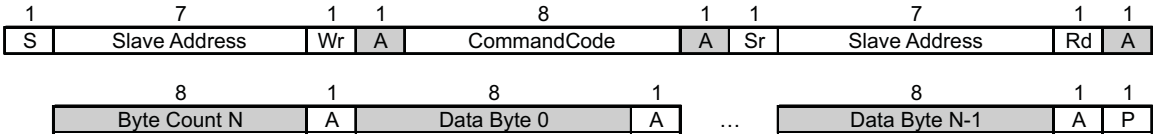


Figure 11. Block Read Protocol

Timing Diagram for the SDA/SCL Serial Control Interface

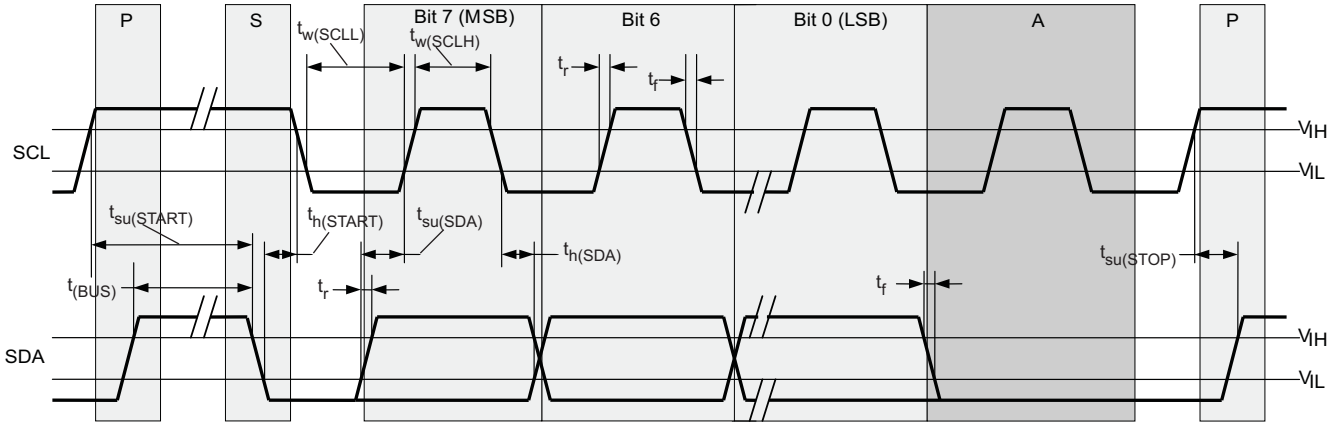


Figure 12. Timing Diagram for SDA/SCL Serial Control Interface

SDA/SCL HARDWARE INTERFACE

Figure 13 shows how the CDCE925/CDCEL925 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus, but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depend on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 kΩ. It must meet the minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages (for more details see the SMBus or I^2C Bus specification).

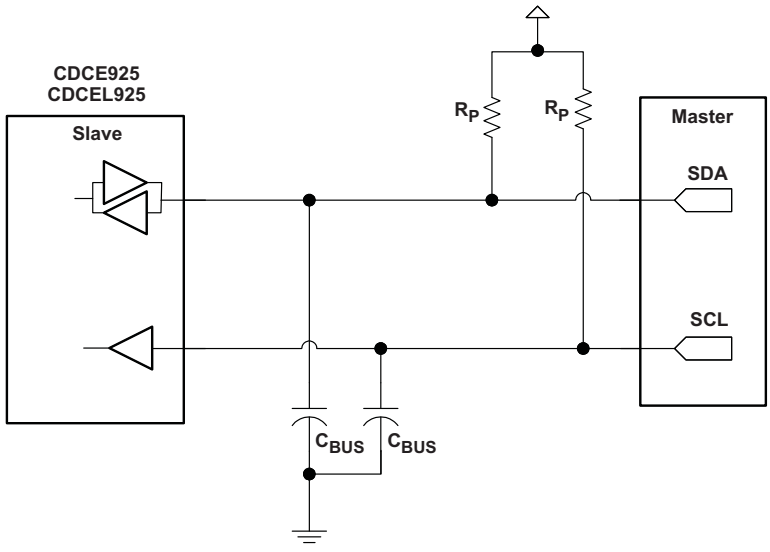


Figure 13. SDA/SCL Hardware Interface

SDA/SCL CONFIGURATION REGISTERS

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCE925/CDCEL925. All settings can be manually written into the device via the SDA/SCL bus or easily programmed by using the TI Pro-Clock™ software. TI Pro-Clock software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 7. SDA/SCL Registers

Address Offset	Register Description	Table
00h	Generic configuration register	Table 9
10h	PLL1 configuration register	Table 10
20h	PLL2 configuration register	Table 11

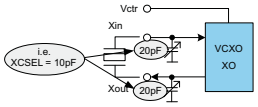
The grey-highlighted bits, described in the Configuration Registers tables in the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2. Table 8 explains the corresponding bit assignment between the Control Terminal Register and the Configuration Registers.

Table 8. Configuration Register, External Control Terminals

				Y1	PLL1 Settings			PLL2 Settings		
	External Control Pins			Output Selection	Frequency Selection	SSC Selection	Output Selection	Frequency Selection	SSC Selection	Output Selection
	S2	S1	S0	Y1	FS1	SSC1	Y2Y3	FS2	SSC2	Y4Y5
0	0	0	0	Y1_0	FS1_0	SSC1_0	Y2Y3_0	FS2_0	SSC2_0	Y4Y5_0
1	0	0	1	Y1_1	FS1_1	SSC1_1	Y2Y3_1	FS2_1	SSC2_1	Y4Y5_1
2	0	1	0	Y1_2	FS1_2	SSC1_2	Y2Y3_2	FS2_2	SSC2_2	Y4Y5_2
3	0	1	1	Y1_3	FS1_3	SSC1_3	Y2Y3_3	FS2_3	SSC2_3	Y4Y5_3
4	1	0	0	Y1_4	FS1_4	SSC1_4	Y2Y3_4	FS2_4	SSC2_4	Y4Y5_4
5	1	0	1	Y1_5	FS1_5	SSC1_5	Y2Y3_5	FS2_5	SSC2_5	Y4Y5_5
6	1	1	0	Y1_6	FS1_6	SSC1_6	Y2Y3_6	FS2_6	SSC2_6	Y4Y5_6
7	1	1	1	Y1_7	FS1_7	SSC1_7	Y2Y3_7	FS2_7	SSC2_7	Y4Y5_7
	Address offset(1)			04h	13h	10h–12h	15h	23h	20h–22h	25h

(1) Address offset refers to the byte address in the configuration register in Table 9, Table 10, and Table 11.

Table 9. Generic Configuration Register

Offset[1]	Bit[2]	Acronym	Default[3]	Description
00h	7	E_EL	Xb	Device identification (read-only): 1 is CDCE925 (3.3 V out), 0 is CDCEL925 (1.8 V out)
	6:4	RID	Xb	Revision identification number (read-only)
	3:0	VID	1h	Vendor identification number (read-only)
01h	7	–	0b	Reserved – always write 0
	6	EEPIP	0b	EEPROM programming Status4:[4] (read-only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode
	5	EELOCK	0b	Permanently lock EEPROM data[5] 0 – EEPROM is not locked 1 – EEPROM is permanently locked
	4	PWDN	0b	Device power down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – Device active (all PLLs and all outputs are enabled) 1 – Device power down (all PLLs in power down and all outputs in high-impedance state)
	3:2	INCLK	00b	Input clock selection: 00 – Xtal 01 – VCXO 10 – LVCMOS 1 – Reserved
	1:0	SLAVE_ADR	00b	Address bits A0 and A1 of the slave receiver address
02h	7	M1	1b	Clock source selection for output Y1: 0 – Input clock 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pins 14/15[6] 0 – Serial programming interface SDA (pin 15) and SCL (pin 14) 1 – Control pins S1 (pin 15) and S2 (pin 14)
	5:4	Y1_ST1	11b	Y1-State0/1 definition
	3:2	Y1_ST0	01b	00 – Device power down (all PLLs in power down and all outputs in high-impedance state) 01 – Y1 disabled to high-impedance state 10 – Y1 disabled to low 11 – Y1 enabled
	1:0	Pdiv1 [9:8]	001h	10-bit Y1-Output-Divider Pdiv1: 0 – Divider is reset and in standby 1 to 1023 – Divider value
03h	7:0	Pdiv1 [7:0]		
04h	7	Y1_7	0b	Y1_ST0/Y1_ST1 State Selection[7] 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1)
	6	Y1_6	0b	
	5	Y1_6	0b	
	4	Y1_6	0b	
	3	Y1_6	0b	
	2	Y1_6	0b	
	1	Y1_6	0b	
	0	Y1_6	0b	
05h	7:3	XCSEL	0Ah	Crystal load-capacitor selection[8] 00h – 0 pF 01h – 1 pF 02h – 2 pF : 14h to 1Fh – 20 pF 
	2:0		0b	Reserved – do not write other than 0.
06h	7:1	BCOUNT	30h	7-bit byte count (defines the number of bytes which will be sent from this device at the next *Block Read* transfer); all bytes must be read out to correctly finish the read cycle.
	0	EEWRITE	0b	Initiate EEPROM write cycle[9] 0 – No EEPROM write cycle 1 – Start EEPROM write cycle (internal registers are saved to the EEPROM)

(1) Writing data beyond 30h may affect device function.
(2) All data transferred with the MSB first
(3) Unless customer-specific setting
(4) During EEPROM programming, no data is allowed to be sent to the device via the SDA/SCL bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (*Byte Read* or *Block Read*).
(5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. No further programming is possible. Data, however can still be written via the SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM.
(6) Selection of *control pins* is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL), and the two slave receiver address bits are reset to A0 = 0 and A1 = 0.
(7) These are the bits of the control terminal register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.
(8) The internal load capacitor (C1, C2) must be used to achieve the best clock performance. External capacitors should be used only to finely adjust C_L by a few picofarads. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For CL > 20 pF, use additional external capacitors. Also, the value of the device input capacitance has to be considered which always adds 1.5 pF (6 pF/2 pF) to the selected C_L. For more information about VCXO configuration and crystal recommendation, see application report SCAA085.
(9) Note: The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level-high does not trigger an EEPROM WRITE cycle. The EEWRITE bit must be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

Table 9. Generic Configuration Register (continued)

Offset[1]	Bit[2]	Acronym	Default[3]	Description
07h-0Fh		—	0h	Reserved – do not write other than 0

Table 10. PLL1 Configuration Register

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC selection (modulation amount). [4] **Down** / **Center** 000 (Off) / 000 (Off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC1_6 [2:0]	000b	
	1:0	SSC1_5 [2:1]	000b	
11h	7	SSC1_5 [0]		
	6:4	SSC1_4 [2:0]	000b	
	3:1	SSC1_3 [2:0]	000b	
	0	SSC1_2 [2]	000b	
12h	7:6	SSC1_2 [1:0]		
	5:3	SSC1_1 [2:0]	000b	
	2:0	SSC1_0 [2:0]	000b	
13h	7	FS1_7	0b	FS1_x: PLL1 frequency selection[4] 0 – f_{VCO1_0} (predefined by PLL1_0 – multiplier/divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – multiplier/divider value)
	6	FS1_6	0b	
	5	FS1_5	0b	
	4	FS1_4	0b	
	3	FS1_3	0b	
	2	FS1_2	0b	
	1	FS1_1	0b	
	0	FS1_0	0b	
14h	7	MUX1	1b	PLL1 multiplexer: 0 – PLL1 1 – PLL1 bypass (PLL1 is in power down)
	6	M2	1b	Output Y2 multiplexer: 0 – Pdiv1 1 – Pdiv2
	5:4	M3	10b	Output Y3 multiplexer: 00 – Pdiv1-divider 01 – Pdiv2-divider 10 – Pdiv3-divider 11 – Reserved
	3:2	Y2Y3_ST1	11b	Y2, Y3-state0/1definition: 00 – Y2/Y3 disabled to high-impedance state (PLL1 is in power down) 01 – Y2/Y3 disabled to high-impedance state (PLL1 on) 10 – Y2/Y3 disabled to low (PLL1 on) 11 – Y2/Y3 enabled (normal operation, PLL1 on)
	1:0	Y2Y3_ST0	01b	
15h	7	Y2Y3_7	0b	Y2Y3_x output state selection[4] 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1)
	6	Y2Y3_6	0b	
	5	Y2Y3_5	0b	
	4	Y2Y3_4	0b	
	3	Y2Y3_3	0b	
	2	Y2Y3_2	0b	
	1	Y2Y3_1	1b	
	0	Y2Y3_0	0b	
16h	7	SSC1DC	0b	PLL1 SSC down/center selection: 0 – Down 1 – Center
	6:0	Pdiv2	01h	7-bit Y2-output-divider Pdiv2: 0 – Reset and in standby 1 to 127 – Divider value
17h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv3	01h	7-bit Y3-output-divider Pdiv3: 0 – Reset and in standby 1 to 127 – Divider value

(1) Writing data beyond 30h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 10. PLL1 Configuration Register (continued)

OFFSET[1]	Bit[2]	Acronym	Default[3]	DESCRIPTION
18h	7:0	PLL1_0N [11:4	004h	PLL1_0[5]: 30-bit multiplier/divider value for frequency f_{VCO1_0} (for more information, see the *PLL Multiplier/Divider Definition* paragraph).
19h	7:4	PLL1_0N [3:0]		
	3:0	PLL1_0R [8:5]	000h	
1Ah	7:3	PLL1_0R[4:0]		
	2:0	PLL1_0Q [5:3]	10h	
1Bh	7:5	PLL1_0Q [2:0]		
	4:2	PLL1_0P [2:0]	010b	
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection: 00 – f_{VCO1_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_0} < 175 MHz 11 – f_{VCO1_0} ≥ 175 MHz
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1[5]: 30-bit multiplier/divider value for frequency f_{VCO1_1} (for more information see the *PLL Multiplier/Divider Definition* paragraph)
1Dh	7:4	PLL1_1N [3:0]		
	3:0	PLL1_1R [8:5]	000h	
1Eh	7:3	PLL1_1R[4:0]		
	2:0	PLL1_1Q [5:3]	10h	
1Fh	7:5	PLL1_1Q [2:0]		
	4:2	PLL1_1P [2:0]	010b	
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection: 00 – f_{VCO1_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_1} < 175 MHz 11 – f_{VCO1_1} ≥ 175 MHz

(5) PLL settings limits: 16 ≤ q ≤ 63, 0 ≤ p ≤ 7, 0 ≤ r ≤ 511, 0 < N < 4096

Table 11. PLL2 Configuration Register

OFFSET(1)	Bit(2)	Acronym	Default(3)	DESCRIPTION
20h	7:5	SSC2_7 [2:0]	000b	SSC2: PLL2 SSC selection (modulation amount). (4) **Down** / **Center** 000 (Off) / 000 (Off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC2_6 [2:0]	000b	
	1:0	SSC2_5 [2:1]	000b	
21h	7	SSC2_5 [0]		
	6:4	SSC2_4 [2:0]	000b	
	3:1	SSC2_3 [2:0]	000b	
	0	SSC2_2 [2]	000b	
22h	7:6	SSC2_2 [1:0]		
	5:3	SSC2_1 [2:0]	000b	
	2:0	SSC2_0 [2:0]	000b	
23h	7	FS2_7	0b	FS2_x: PLL2 frequency selection(4) 0 – f_{VCO2_0} (predefined by PLL2_0 – multiplier/divider value) 1 – f_{VCO2_1} (predefined by PLL2_1 – multiplier/divider value)
	6	FS2_6	0b	
	5	FS2_5	0b	
	4	FS2_4	0b	
	3	FS2_3	0b	
	2	FS2_2	0b	
	1	FS2_1	0b	
	0	FS2_0	0b	
24h	7	MUX2	1b	PLL2 multiplexer: 0 – PLL2 1 – PLL2 bypass (PLL2 is in power down)
	6	M4	1b	Output Y4 multiplexer: 0 – Pdiv2 1 – Pdiv4
	5:4	M5	10b	Output Y5 multiplexer: 00 – Pdiv2-divider 01 – Pdiv4-divider 10 – Pdiv5-divider 11 – Reserved
	3:2	Y4Y5_ST1	11b	Y4, Y5-State0/1definition: 00 – Y4/Y5 disabled to high-impedance state (PLL2 is in power down) 01 – Y4/Y5 disabled to high-impedance state (PLL2 on) 10–Y4/Y5 disabled to low (PLL2 on) 11 – Y4/Y5 enabled (normal operation, PLL2 on)
	1:0	Y4Y5_ST0	01b	
25h	7	Y4Y5_7	0b	Y4Y5_x output state selection(4) 0 – state0 (predefined by Y4Y5_ST0) 1 – state1 (predefined by Y4Y5_ST1)
	6	Y4Y5_6	0b	
	5	Y4Y5_5	0b	
	4	Y4Y5_4	0b	
	3	Y4Y5_3	0b	
	2	Y4Y5_2	0b	
	1	Y4Y5_1	1b	
	0	Y4Y5_0	0b	
26h	7	SSC2DC	0b	PLL2 SSC down/center selection: 0 – Down 1 – Center
	6:0	Pdiv4	01h	7-Bit Y4-output-divider Pdiv4: 0 – Reset and in standby 1 to 127 – Divider value
27h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv5	01h	7-bit Y5-output-divider Pdiv5: 0 – Reset and in standby 1 to 127 – Divider value

(1) Writing data beyond 30h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 11. PLL2 Configuration Register (continued)

OFFSET(1)	Bit(2)	Acronym	Default(3)	DESCRIPTION
28h	7:0	PLL2_0N [11:4	004h	PLL2_0(5): 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information see the *PLL Multiplier/Divider Definition* paragraph)
29h	7:4	PLL2_0N [3:0]		
	3:0	PLL2_0R [8:5]	000h	
2Ah	7:3	PLL2_0R[4:0]		
	2:0	PLL2_0Q [5:3]	10h	
2Bh	7:5	PLL2_0Q [2:0]		
	4:2	PLL2_0P [2:0]	010b	
	1:0	VCO2_0_RANGE	00b	f_{VCO2_0} range selection: 00 – f_{VCO2_0} < 125 MHz; 01 – 125 MHz ≤ f_{VCO2_0} < 150 MHz; 10 – 150 MHz ≤ f_{VCO2_0} < 175 MHz; 11 – f_{VCO2_0} ≥ 175 MHz
2Ch	7:0	PLL2_1N [11:4]	004h	PLL2_1(5): 30-bit multiplier/divider value for frequency f_{VCO2_1} (for more information see the *PLL Multiplier/Divider Definition* paragraph)
2Dh	7:4	PLL2_1N [3:0]		
	3:0	PLL2_1R [8:5]	000h	
2Eh	7:3	PLL2_1R[4:0]		
	2:0	PLL2_1Q [5:3]	10h	
2Fh	7:5	PLL2_1Q [2:0]		
	4:2	PLL2_1P [2:0]	010b	
	1:0	VCO2_1_RANGE	00b	f_{VCO2_1} range selection: 00 – f_{VCO2_1} < 125 MHz; 01 – 125 MHz ≤ f_{VCO2_1} < 150 MHz; 10 – 150 MHz ≤ f_{VCO2_1} < 175 MHz; 11 – f_{VCO2_1} ≥ 175 MHz

(5) PLL settings limits: 16 ≤ q ≤ 63, 0 ≤ p ≤ 7, 0 ≤ r ≤ 511, 0 < N < 4096

PLL Multiplier/Divider Definition

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCE925/CDCEL925 can be calculated:

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M} \quad (1)$$

where

M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL; Pdiv (1 to 127) is the output divider.

The target VCO frequency (f_{VCO}) of each PLL can be calculated:

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and needs the following multiplier/divider settings:

$$NP = 4 - \text{int}\left(\log_2 \frac{N}{M}\right) \text{ [if } P < 0 \text{ then } P = 0] \quad Q = \text{int}\left(\frac{N'}{M}\right) \quad R = N' - M \times Q$$

where

$N' = N \times 2^P$
$N \geq M$
$80\ MHz \leq f_{VCO} \leq 230\ MHz$
$16 \leq q \leq 63$
$0 \leq p \leq 4$
$0 \leq r \leq 511$

Example:

for f_{IN} = 27 MHz; M = 1; N = 4; Pdiv = 2;

→ f_{OUT} = 54 MHz
→ f_{VCO} = 108 MHz
→ P = 4 – int($\log_2$4) = 4 – 2 = 2
→ N″ = 4 × 2^2 = 16
→ Q = int(16) = 16
→ R = 16 – 16 = 0

for f_{IN} = 27 MHz; M = 2; N = 11; Pdiv = 2;

→ f_{OUT} = 74.25 MHz
→ f_{VCO} = 148.50 MHz
→ P = 4 – int($\log_2$5.5) = 4 – 2 = 2
→ N″ = 11 × 2^2 = 44
→ Q = int(22) = 22
→ R = 44 – 44 = 0

The values for P, Q, R, and N' are automatically calculated when using TI Pro-Clock™ software.

REVISION HISTORY

Changes from Original (July 2007) to Revision A — **Page**

- Changed the data sheet status From: Product Preview To: Production data. 1

Changes from Revision A (August 2007) to Revision B — **Page**

- Changed I_{DDPD} Power-down current Typ value From: 20 To: 30 6
- Changed I_I LVCMOS Input current value From: ±5 Typ To: ±5 Max 6
- Changed I_{IH} LVCMOS Input current for S0/S1/S2 value From: 5 Typ To: 5 Max 6
- Changed I_{IL} LVCMOS Input current for S0/S1/S2 value From: -4 Typ To: -4 Max 6
- Changed text of Note 4 in the DEVICE CHARACTERISTIC table 7
- Changed Figure 2, Test Load for 50-Ω Board Environment 8
- Changed Table 2 header From: OUTPUT SELECTION (Y2 ... Y9) To: OUTPUT SELECTION (Y2 ... Y5) 10
- Changed Table 9 - 01h Bit 7 From: For interla use – always write To: Reserved – always write 16
- Changed Table 9 - PLL2_1N [11:4] description From: f_{VCO1_1} To: f_{VCO2_1} 20

Changes from Revision B (August 2007) to Revision C — **Page**

- Changed the PACKAGE THERMAL RESISTANCE for TSSOP table 3
- Changed Table 9 - RID From: 0h To: Xb 16
- Added note to the PWDN description, Table 9 16

Changes from Revision C (December 2007) to Revision D — **Page**

- Added Note 3: SDA and SCL can go up to 3.6V as stated in the Recommended Operating Conditions table. 3

Changes from Revision D (September 2009) to Revision E — **Page**

- Deleted sentence - A different default setting can be programmed on customer request. Contact Texas Instruments sales or marketing representative for more information. 11

Changes from Revision E (October 2009) to Revision F — **Page**

- Added PLL settings limits: 16 ≤ q ≤ 63, 0 ≤ p ≤ 7, 0 ≤ r ≤ 511, 0 < N < 4096 to PLL1 and PLL2 Configure Register tables 18
- Added PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<511 to PLL Multiplier/Divder Definition Section 21

Changes from Revision F (March 2010) to Revision G — **Page**

- Changed in Figure 9, second S to Sr 13
- Changed under second where page 21 from N′ = N × 2^PN ≥ M100 MHz ≤ f_{VCO} ≤ 200 MHz; TO 3 lines with last line being changed to 80 MHz ≤ f_{VCO} ≤ 230 MHz and 0 ≤ p ≤ 7 changed to 0 ≤ p ≤ 4 21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCE925PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCE925PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCE925PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCE925PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCEL925PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL925	Samples
CDCEL925PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL925	Samples
CDCEL925PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL925	Samples
CDCEL925PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL925	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

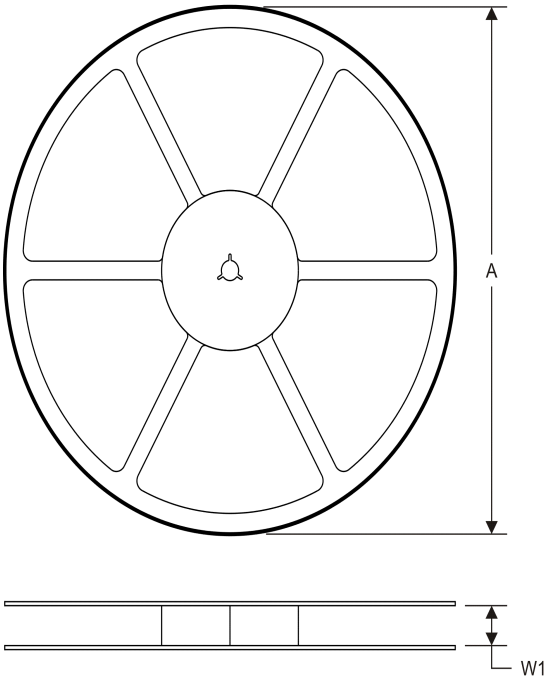
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

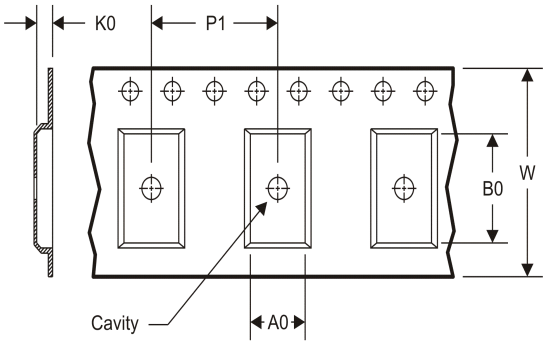
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



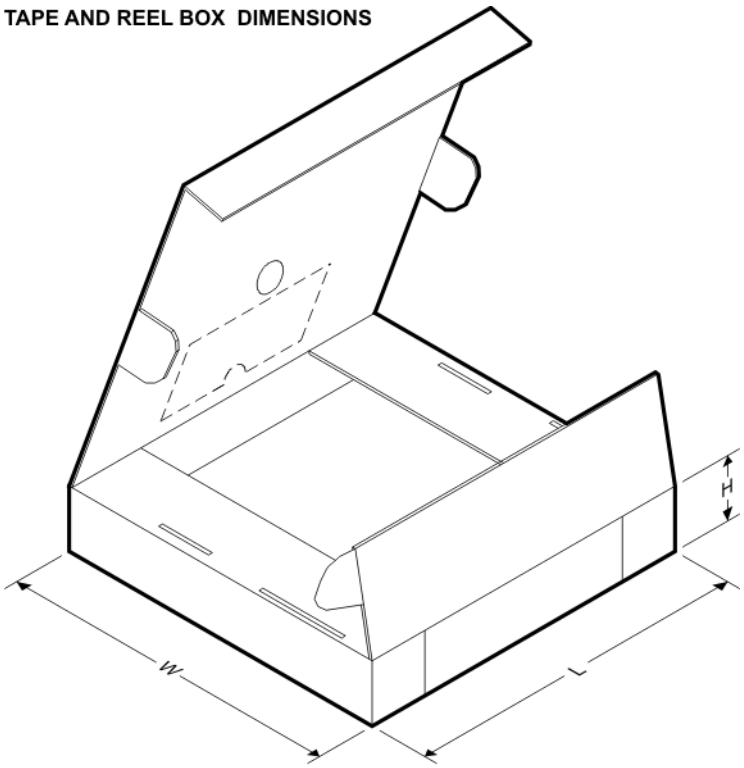
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE925PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCEL925PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

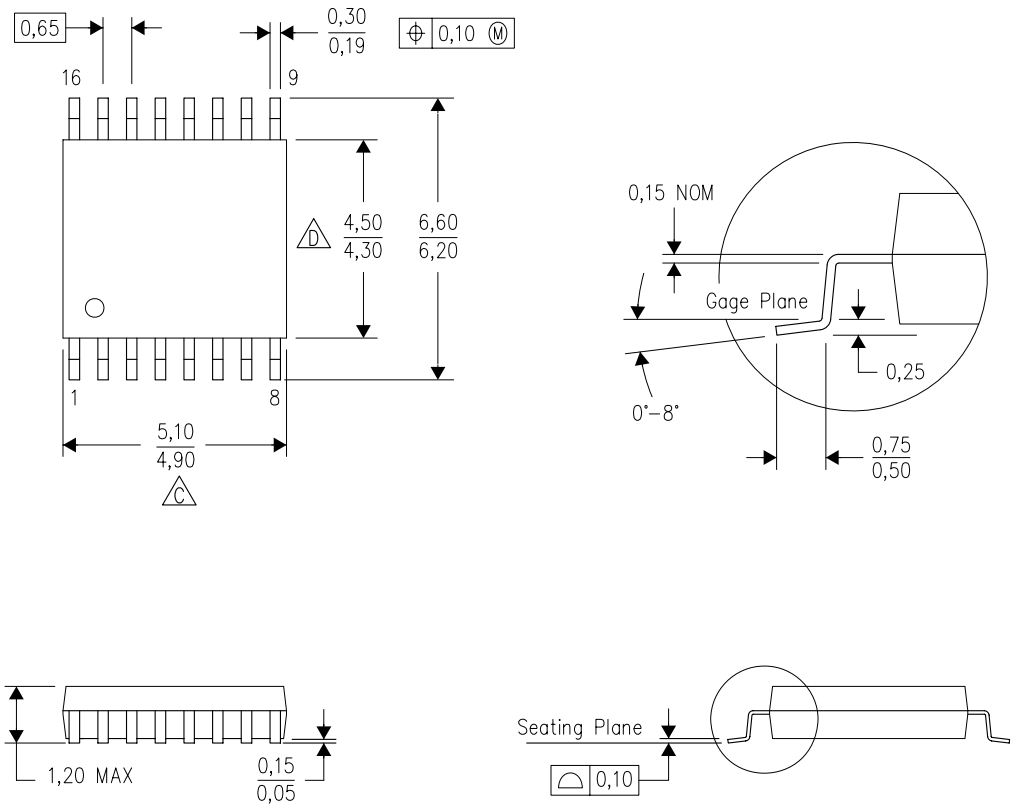
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE925PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CDCEL925PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

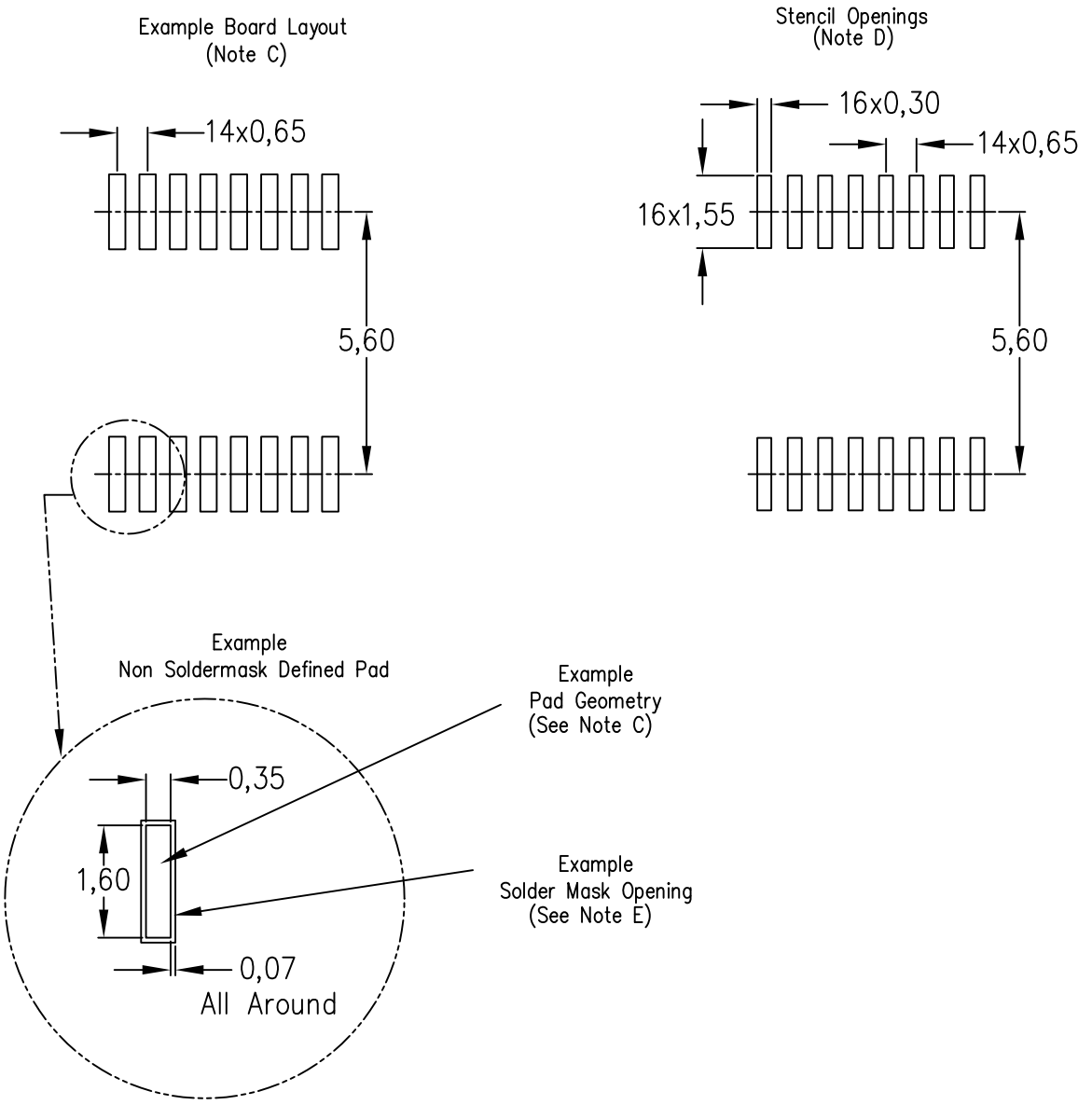
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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