

# 108 dB, 192 kHz 6-In, 8-Out TDM CODEC

## FEATURES

- ◆ Six 24-bit A/D, Eight 24-bit D/A Converters
- ◆ ADC Dynamic Range
  - 105 dB Differential
  - 102 dB Single-Ended
- ◆ DAC Dynamic Range
  - 108 dB Differential
  - 105 dB Single-Ended
- ◆ ADC/DAC THD+N
  - -98 dB Differential
  - -95 dB Single-Ended
- ◆ Compatible with Industry-Standard Time Division Multiplexed (TDM) Serial Interface
- ◆ DAC Sampling Rates up to 192 kHz
- ◆ ADC Sampling Rates up to 96 kHz
- ◆ Programmable ADC High-Pass Filter for DC Offset Calibration
- ◆ Logarithmic Digital Volume Control
- ◆ Hardware Mode or Software I<sup>2</sup>C® & SPI™
- ◆ Supports Logic Levels Between 5 V and 1.8 V

## GENERAL DESCRIPTION

The CS42438 CODEC provides six multi-bit analog-to-digital and eight multi-bit digital-to-analog delta-sigma converters. The CODEC is capable of operation with either differential or single-ended inputs and outputs, in a 52-pin MQFP package.

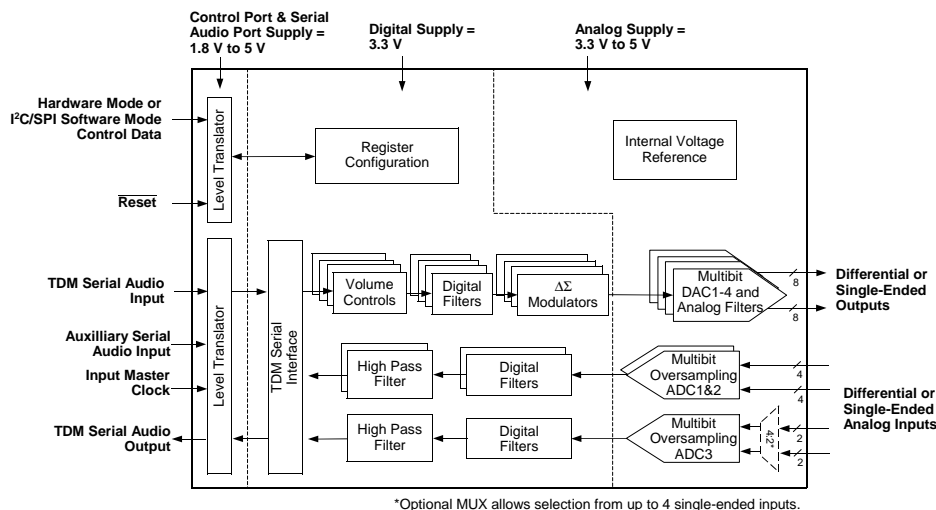
Six fully differential, or single-ended, inputs are available on stereo ADC1, ADC2, and ADC3. When operating in Single-ended Mode, an internal MUX before ADC3 allows selection from up to four single-ended inputs. Digital volume control is provided for each ADC channel, with selectable overflow detection.

All eight DAC channels provide digital volume control and can operate with differential or single-ended outputs.

An auxiliary serial input is available for an additional two channels of PCM data.

The CS42438 is available in a 52-pin MQFP package in Commercial (-10° to +70°) and Automotive (-40° to +105°) grades. The CDB42438 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to [“Ordering Information” on page 61](#) for complete ordering information.

The CS42438 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, and automotive audio systems.



\*Optional MUX allows selection from up to 4 single-ended inputs.

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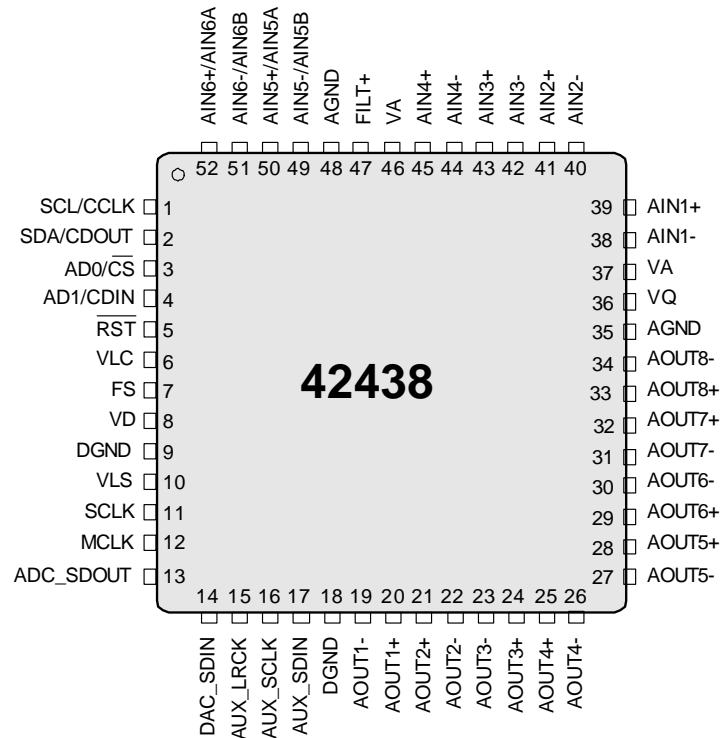
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# 1. PIN DESCRIPTIONS - SOFTWARE MODE



Pin Name	#	Pin Description
SCL/CCLK	1	<b>Serial Control Port Clock (Input)</b> - Serial clock for the control port interface.
SDA/CDOUT	2	<b>Serial Control Data I/O (Input/Output)</b> - Input/Output for I <sup>2</sup> C data. Output for SPI data.
AD0/ $\overline{CS}$	3	<b>Address Bit [0]/ Chip Select (Input)</b> - Chip address bit in I <sup>2</sup> C Mode. Control signal used to select the chip in SPI Mode.
AD1/CDIN	4	<b>Address Bit [1]/ SPI Data Input (Input)</b> - Chip address bit in I <sup>2</sup> C Mode. Input for SPI data.
$\overline{RST}$	5	<b>Reset (Input)</b> - The device enters a low-power mode and all internal registers are reset to their default settings when low.
VLC	6	<b>Control Port Power (Input)</b> - Determines the required signal level for the control port interface. See <a href="#">“Digital I/O Pin Characteristics” on page 8</a> .
FS	7	<b>Frame Sync (Input)</b> - Signals the start of a new TDM frame in the TDM digital interface format.
VD	8	<b>Digital Power (Input)</b> - Positive power supply for the digital section.
DGND	9,18	<b>Digital Ground (Input)</b> -
VLS	10	<b>Serial Port Interface Power (Input)</b> - Determines the required signal level for the serial port interfaces. See <a href="#">“Digital I/O Pin Characteristics” on page 8</a> .
SCLK	11	<b>Serial Clock (Input)</b> - Serial clock for the serial audio interface. Input frequency must be 256 x Fs.
MCLK	12	<b>Master Clock (Input)</b> - Clock source for the delta-sigma modulators and digital filters.
ADC_SDOUT	13	<b>Serial Audio Data Output (Output)</b> - TDM output for two’s complement serial audio data.
DAC_SDIN	14	<b>DAC Serial Audio Data Input (Input)</b> - TDM Input for two’s complement serial audio data.
AUX_LRCK	15	<b>Auxiliary Left/Right Clock (Output)</b> - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line.

AUX_SCLK	16	<b>Auxiliary Serial Clock (Output)</b> - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	17	<b>Auxiliary Serial Input (Input)</b> - The 42438 provides an additional serial input for two's complement serial audio data.
AOUT1 +,-	20,19	<b>Differential Analog Output (Output)</b> - The full-scale differential analog output level is specified in the Analog Characteristics specification table. Each positive leg of the differential outputs may also be used single-ended.
AOUT2 +,-	21,22	
AOUT3 +,-	24,23	
AOUT4 +,-	25,26	
AOUT5 +,-	28,27	
AOUT6 +,-	29,30	
AOUT7 +,-	31,32	
AOUT8 +,-	33,34	
AGND	35,48	<b>Analog Ground (Input)</b> - Ground reference for the analog section.
VQ	36	<b>Quiescent Voltage (Output)</b> - Filter connection for internal quiescent reference voltage.
VA	37,46	<b>Analog Power (Input)</b> - Positive power supply for the analog section.
AIN1 +,-	39,38	<b>Differential Analog Input (Input)</b> - Signals are presented differentially to the delta-sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table. Single-ended inputs may be applied to the positive terminals when the ADCx SINGLE bit is enabled. Once in Single-Ended Mode, the negative terminal of AIN1-AIN4 must be externally driven to common mode. See below for a description of AIN5-AIN6 in Single-Ended Mode.
AIN2 +,-	41,40	
AIN3 +,-	43,42	
AIN4 +,-	45,44	
AIN5 +,-	50,49	
AIN6 +,-	52,51	
AIN5 A,B	50,49	<b>Single-Ended Analog Input (Input)</b> - In Single-Ended Mode, an internal analog mux allows selection between two channels for both analog inputs AIN5 and AIN6 (see <a href="#">Sections 7.6.6-7.6.8</a> for details). The unused leg of each input is internally connected to common mode. The full-scale input level is specified in the Analog Characteristics specification table.
AIN6 A,B	52,51	
FILT+	47	<b>Positive Voltage Reference (Output)</b> - Positive reference voltage for the internal sampling circuits.

## 1.1 Digital I/O Pin Characteristics

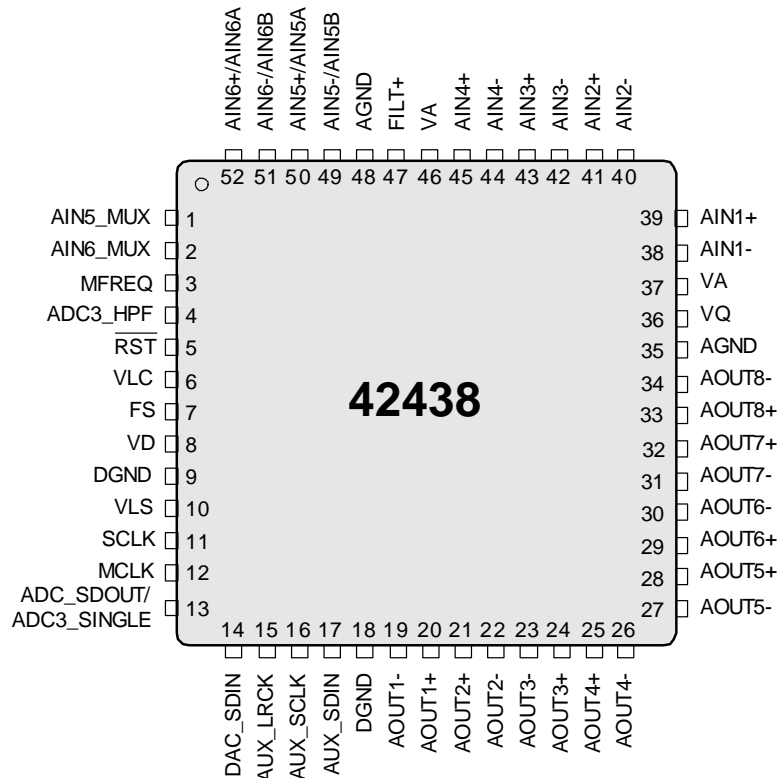
Various pins on the CS42438 are powered from separate power supply rails. The logic level for each input should adhere to the corresponding power rail and should not exceed the maximum ratings.

Power Rail	Pin Name SW/(HW)	I/O	Driver	Receiver
VLC	$\overline{\text{RST}}$	Input	-	1.8 V - 5.0 V, CMOS
	SCL/CCLK (AIN5_MUX)	Input	-	1.8 V - 5.0 V, CMOS, with Hysteresis
	SDA/CDOUT (AIN6_MUX)	Input/Output	1.8 V - 5.0 V, CMOS/Open Drain	1.8 V - 5.0 V, CMOS, with Hysteresis
	AD0/CS (MFREQ)	Input	-	1.8 V - 5.0 V, CMOS
	AD1/CDIN (ADC3_HPF)	Input	-	1.8 V - 5.0 V, CMOS
VLS	MCLK	Input	-	1.8 V - 5.0 V, CMOS
	LRCK	Input	-	1.8 V - 5.0 V, CMOS
	SCLK	Input	-	1.8 V - 5.0 V, CMOS
	ADC_SDOUT3 (ADC3_SINGLE)	Input/Output	1.8 V - 5.0 V, CMOS	-
	DAC_SDIN	Input	-	1.8 V - 5.0 V, CMOS
	AUX_LRCK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SCLK	Output	1.8 V - 5.0 V, CMOS	-
	AUX_SDIN	Input	-	1.8 V - 5.0 V, CMOS

**Table 1. I/O Power Rails**



## 2. PIN DESCRIPTIONS - HARDWARE MODE



Pin Name	#	Pin Description
AIN5_MUX	1	<b>Analog Input Multiplexer (Input)</b> - Allows selection between the A and B single-ended inputs of ADC3. See <a href="#">Section 7.6.7</a> and <a href="#">7.6.8</a> for details.
AIN6_MUX	2	
MFREQ	3	<b>MCLK Frequency (Input)</b> - Sets the required frequency range of the input Master Clock. See <a href="#">Section 5.4</a> for the appropriate settings.
ADC3_HPF	4	<b>ADC3 High-Pass Filter Freeze (Input)</b> - When this pin is driven high, the internal high-pass filter will be disabled for ADC3. The current DC offset value will be frozen and continue to be subtracted from the conversion result. See <a href="#">"ADC Digital Filter Characteristics"</a> on page 16.
RST	5	<b>Reset (Input)</b> - The device enters a low-power mode and all internal registers are reset to their default settings when low.
VLC	6	<b>Control Port Power (Input)</b> - Determines the required signal level for the control port interface. See <a href="#">"Digital I/O Pin Characteristics"</a> on page 8.
FS	7	<b>Frame Sync (Input)</b> - Signals the start of a new TDM frame in the TDM digital interface format.
VD	8	<b>Digital Power (Input)</b> - Positive power supply for the digital section.
VLS	10	<b>Serial Port Interface Power (Input)</b> - Determines the required signal level for the serial port interfaces.
SCLK	11	<b>Serial Clock (Input)</b> - Serial clock for the serial audio interface. Input frequency must be 256 x Fs.
ADC_SDOOUT/ ADC3_SINGLE	13	<b>Serial Audio Data Output (Output)</b> - TDM output for two's complement serial audio data. Start-up Option for Hardware Mode: Pull-up to VLS enables Single-Ended Mode for AIN5-AIN6.
DAC_SDIN	14	<b>DAC Serial Audio Data Input (Input)</b> - Input for two's complement serial audio data.
AUX_LRCK	15	<b>Auxiliary Left/Right Clock (Output)</b> - Determines which channel, Left or Right, is currently active on the Auxiliary serial audio data line.

AUX_SCLK	16	<b>Auxiliary Serial Clock (Output)</b> - Serial clock for the Auxiliary serial audio interface.
AUX_SDIN	17	<b>Auxiliary Serial Input (Input)</b> - The 42438 provides an additional serial input for two's complement serial audio data.
AOUT1 +,-	20,19	<b>Differential Analog Output (Output)</b> - The full-scale differential analog output level is specified in the Analog Characteristics specification table. Each positive leg of the differential outputs may also be used single-ended.
AOUT2 +,-	21,22	
AOUT3 +,-	24,23	
AOUT4 +,-	25,26	
AOUT5 +,-	28,27	
AOUT6 +,-	29,30	
AOUT7 +,-	31,32	
AOUT8 +,-	33,34	
AGND	35,48	<b>Analog Ground (Input)</b> - Ground reference for the analog section.
VQ	36	<b>Quiescent Voltage (Output)</b> - Filter connection for internal quiescent reference voltage.
VA	37,46	<b>Analog Power (Input)</b> - Positive power supply for the analog section.
AIN1 +,-	39,38	<b>Differential Analog Input (Input)</b> - Signals are presented differentially to the delta-sigma modulators. The full-scale input level is specified in the Analog Characteristics specification table. Single-ended inputs may be applied to the positive terminals when the ADCx SINGLE pin is enabled. Once in Single-Ended Mode, the negative terminal of AIN1-AIN4 must be externally driven to common mode. See below for a description of AIN5-AIN6 in Single-Ended Mode.
AIN2 +,-	41,40	
AIN3 +,-	43,42	
AIN4 +,-	45,44	
AIN5 +,-	50,49	
AIN6 +,-	52,51	
AIN7 +,-	52,53	
AIN8 +,-		
AIN5 A,B	50,49	<b>Single-Ended Analog Input (Input)</b> - In Single-Ended Mode, an internal analog mux allows selection between 2 channels for both analog inputs AIN5 and AIN6 (see <a href="#">Sections 7.6.6-7.6.8</a> for details). The unused leg of each input is internally connected to common mode. The full-scale input level is specified in the Analog Characteristics specification table.
AIN6 A,B	52,51	
FILT+	47	<b>Positive Voltage Reference (Output)</b> - Positive reference voltage for the internal sampling circuits.

### 3. TYPICAL CONNECTION DIAGRAMS

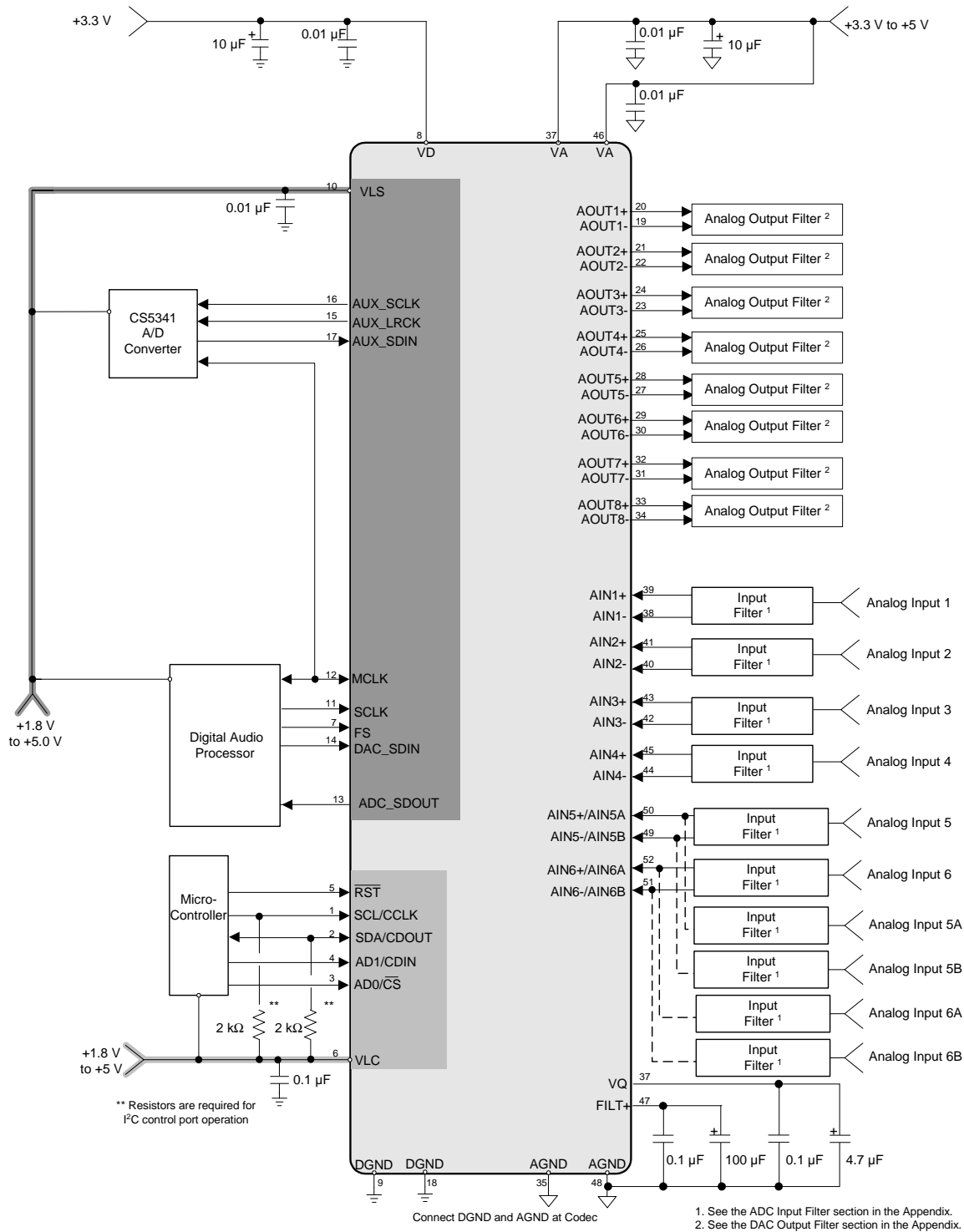


Figure 1. Typical Connection Diagram (Software Mode)

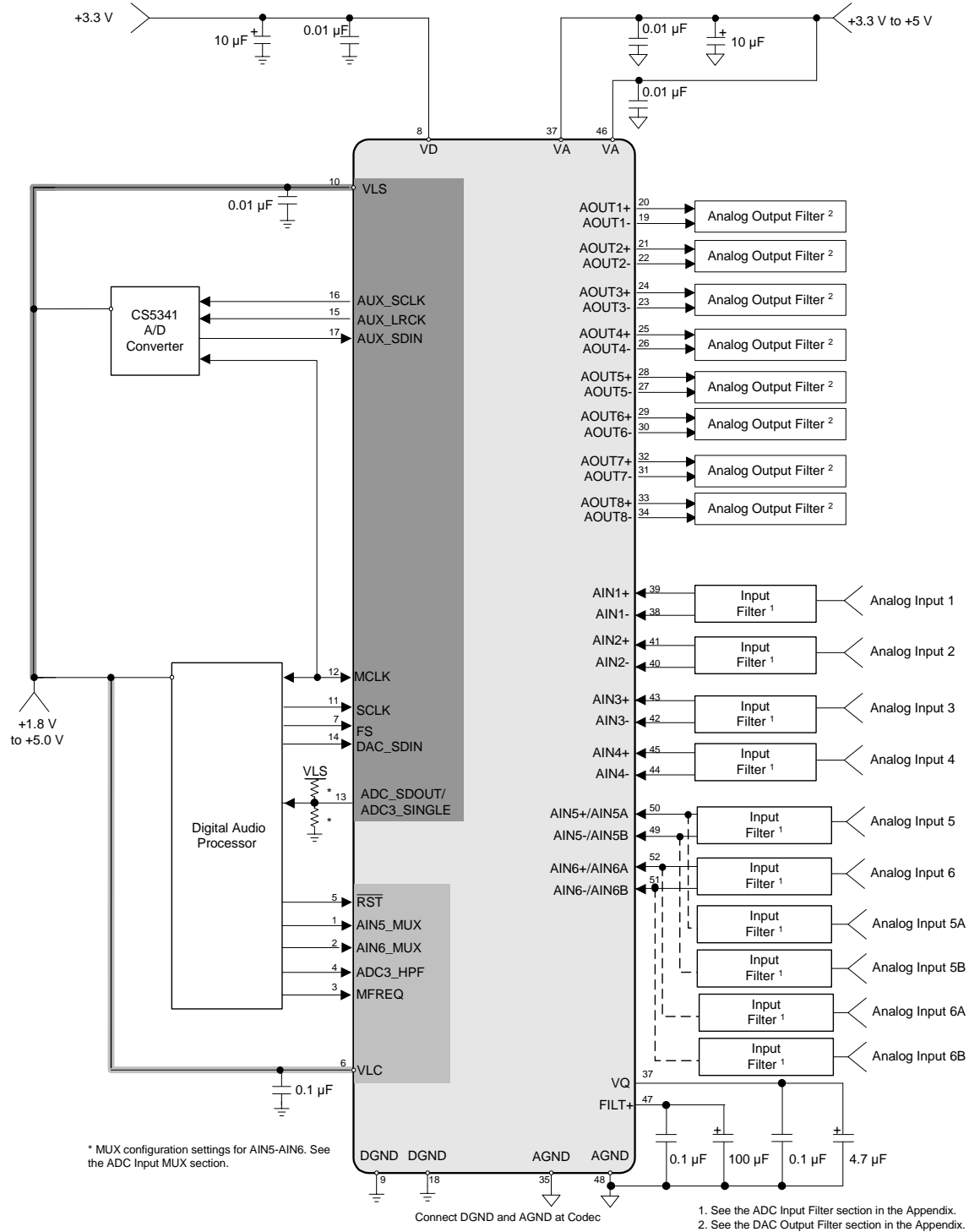


Figure 2. Typical Connection Diagram (Hardware Mode)

## 4. CHARACTERISTICS AND SPECIFICATIONS

### RECOMMENDED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply				
Analog (Note 1)	VA	3.14	5.25	V
Digital	VD	3.14	3.47	V
Serial Audio Interface (Note 2)	VLS	1.71	5.25	V
Control Port Interface	VLC	1.71	5.25	V
Ambient Temperature				
Commercial -CMZ	T <sub>A</sub>	-10	+70	°C
Automotive -DMZ		-40	+105	°C

### ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units	
DC Power Supply	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	Serial Port Interface	VLS	-0.3	6.0	V
	Control Port Interface	VLC	-0.3	6.0	V
Input Current (Note 3)	I <sub>in</sub>	-	±10	mA	
Analog Input Voltage (Note 4)	V <sub>IN</sub>	AGND-0.7	VA+0.7	V	
Digital Input Voltage (Note 4)	Serial Port Interface	V <sub>IND-S</sub>	-0.3	VLS+ 0.4	V
	Control Port Interface	V <sub>IND-C</sub>	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)	T <sub>A</sub>	-50	+125	°C	
Storage Temperature	T <sub>stg</sub>	-65	+150	°C	

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

#### Notes:

1. Typical Analog input/output performance will slightly degrade at VA = 3.3 V.
2. The ADC\_SDOOUT may not meet timing requirements in Double-Speed Mode.
3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
4. The maximum over/under voltage is limited by the input current.

**ANALOG INPUT CHARACTERISTICS (COMMERCIAL)**

(Test Conditions (unless otherwise specified):  $T_A = -10$  to  $+70^\circ\text{C}$ ;  $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$ ,  $V_A = 5\text{ V} \pm 5\%$ ;  
 Full-scale input sine wave: 1 kHz through the active input filter in [Figure 20 on page 50](#) and [Figure 21 on page 50](#);  
 Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz								
Dynamic Range	A-weighted	99	105	-	96	102	-	dB
	unweighted	96	102	-	93	99	-	dB
	40 kHz bandwidth unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 5)	-1 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
	40 kHz bandwidth -1 dB	-	-90	-	-	-90	-	dB
ADC1-3 Interchannel Isolation		-	90	-	-	90	-	dB
ADC3 MUX Interchannel Isolation		-	90	-	-	90	-	dB
<b>DC Accuracy</b>								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	$\pm 100$	-	-	$\pm 100$	-	ppm/ $^\circ\text{C}$
<b>Analog Input</b>								
Full-Scale Input Voltage		1.06*VA	1.12*VA	1.18*VA	0.53*VA	0.56*VA	0.59*VA	Vpp
Differential Input Impedance (Note 6)		18	-	-	-	-	-	k $\Omega$
Single-Ended Input Impedance (Note 7)		-	-	-	18	-	-	k $\Omega$
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

## ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified):  $T_A = -40$  to  $+85^\circ\text{C}$ ;  $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$ ,  $V_A = 5\text{ V} \pm 5\%$ ;  
Full-scale input sine wave: 1 kHz through the active input filter in [Figure 20 on page 50](#) and [Figure 21 on page 50](#);  
Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter		Differential			Single-Ended			Unit
		Min	Typ	Max	Min	Typ	Max	
Fs=48 kHz, 96 kHz								
Dynamic Range	A-weighted	97	105	-	94	102	-	dB
	unweighted	94	102	-	91	99	-	dB
	40 kHz bandwidth unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 5)	-1 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
	40 kHz bandwidth -1 dB	-	-87	-	-	-87	-	dB
ADC1-3 Interchannel Isolation		-	90	-	-	90	-	dB
ADC3 MUX Interchannel Isolation		-	85	-	-	85	-	dB
<b>DC Accuracy</b>								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	$\pm 100$	-	-	$\pm 100$	-	ppm/ $^\circ\text{C}$
<b>Analog Input</b>								
Full-Scale Input Voltage		1.04*VA	1.12*VA	1.20*VA	0.52*VA	0.56*VA	0.60*VA	Vpp
Differential Input Impedance (Note 6)		18	-	-	-	-	-	k $\Omega$
Single-Ended Input Impedance (Note 7)		-	-	-	18	-	-	k $\Omega$
Common Mode Rejection Ratio (CMRR)		-	82	-	-	-	-	dB

**Notes:**

5. Referred to the typical full-scale voltage.
6. Measured between AINx+ and AINx-.
7. Measured between AINxx and AGND.

**ADC DIGITAL FILTER CHARACTERISTICS**

Parameter (Notes 8, 9)		Min	Typ	Max	Unit
<b>Single-Speed Mode (Note 9)</b>					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.08	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	12/Fs	-	s
<b>Double-Speed Mode (Note 9)</b>					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4896	Fs
Passband Ripple		-	-	0.16	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay		-	9/Fs	-	s
<b>High-Pass Filter Characteristics</b>					
Frequency Response	-3.0 dB	-	1	-	Hz
	-0.13 dB	-	20	-	Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time		-	10 <sup>5</sup> /Fs	0	s

**Notes:**

8. Filter response is guaranteed by design.
9. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 26 to 33) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.



## ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL)

(Test Conditions (unless otherwise specified):  $T_A = -10$  to  $+70^\circ\text{C}$ ;  $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$ ,  $V_A = 5\text{ V} \pm 5\%$ ; Full-scale 997 Hz output sine wave (see [Note 11](#)) into passive filter in [Figure 26 on page 54](#) and active filter in [Figure 26 on page 54](#); Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter	Differential			Single-Ended			Unit	
	Min	Typ	Max	Min	Typ	Max		
<b><i>Fs = 48 kHz, 96 kHz, 192 kHz</i></b>								
Dynamic Range								
18 to 24-Bit	A-weighted	102	108	-	99	105	-	dB
	unweighted	99	105	-	96	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36	-	-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
<b><i>Analog Output</i></b>								
Full-Scale Output		1.235•VA	1.300•VA	1.365•VA	0.618•VA	0.650•VA	0.683•VA	Vpp
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin	( <a href="#">Note 10</a> )	-	-	10	-	-	10	μA
AC-Load Resistance ( $R_L$ )	( <a href="#">Note 12</a> )	3	-	-	3	-	-	kΩ
Load Capacitance ( $C_L$ )	( <a href="#">Note 12</a> )	-	-	100	-	-	100	pF

## ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE)

(Test Conditions (unless otherwise specified):  $T_A = -40$  to  $+85^\circ\text{C}$ ;  $V_D = V_{LS} = V_{LC} = 3.3\text{ V} \pm 5\%$ ,  $V_A = 5\text{ V} \pm 5\%$ ; Full-scale 997 Hz output sine wave (see [Note 11](#)) in [Figure 26 on page 54](#) and [Figure 26 on page 54](#); Measurement Bandwidth is 10 Hz to 20 kHz.)

Parameter	Differential			Single-Ended			Unit	
	Min	Typ	Max	Min	Typ	Max		
<b><i>F<sub>s</sub> = 48 kHz, 96 kHz, 192 kHz</i></b>								
Dynamic Range								
18 to 24-Bit	A-weighted	100	108	-	97	105	-	dB
	unweighted	97	105	-	94	102	-	dB
16-Bit	A-weighted	-	99	-	-	96	-	dB
	unweighted	-	96	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-98	-90	-	-95	-87	dB
	-20 dB	-	-85	-	-	-82	-	dB
	-60 dB	-	-45	-	-	-42	-	dB
16-Bit	0 dB	-	-93	-	-	-90	-	dB
	-20 dB	-	-76	-	-	-73	-	dB
	-60 dB	-	-36	-	-	-33	-	dB
Interchannel Isolation	(1 kHz)	-	100	-	-	100	-	dB
<b><i>Analog Output</i></b>								
Full-Scale Output		1.210•V <sub>A</sub>	1.300•V <sub>A</sub>	1.392•V <sub>A</sub>	0.605•V <sub>A</sub>	0.650•V <sub>A</sub>	0.696•V <sub>A</sub>	V <sub>pp</sub>
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Output Impedance		-	100	-	-	100	-	Ω
DC Current draw from an AOUT pin		-	-	10	-	-	10	μA
	( <a href="#">Note 10</a> )							
AC-Load Resistance (R <sub>L</sub> )	( <a href="#">Note 12</a> )	3	-	-	3	-	-	kΩ
Load Capacitance (C <sub>L</sub> )	( <a href="#">Note 12</a> )	-	-	100	-	-	100	pF

### Notes:

- Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC-blocking capacitors.
- One-half LSB of triangular PDF dither is added to data.
- Guaranteed by design. See [Figure 3](#). R<sub>L</sub> and C<sub>L</sub> reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C<sub>L</sub> will effectively move the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable. See "[External Filters](#)" on [page 50](#) for a recommended output filter.

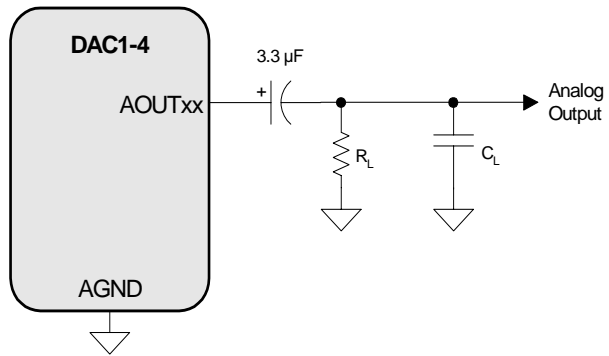


Figure 3. Output Test Circuit for Maximum Load

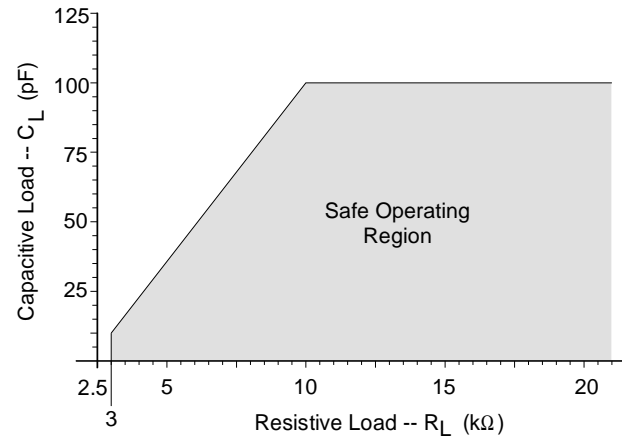


Figure 4. Maximum Loading

**COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE**

Parameter (Notes 8, 13)	Min	Typ	Max	Unit	
<b>Single-Speed Mode</b>					
Passband (Frequency Response)	to -0.05 dB corner	0	-	0.4780	Fs
	to -3 dB corner	0	-	0.4996	Fs
Frequency Response 10 Hz to 20 kHz	-0.2	-	+0.08	dB	
StopBand	0.5465	-	-	Fs	
StopBand Attenuation (Note 14)	50	-	-	dB	
Group Delay	-	10/Fs	-	s	
De-emphasis Error (Note 15)	Fs = 32 kHz	-	-	+1.5/+0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.25	dB
	Fs = 48 kHz	-	-	-0.2/-0.4	dB
<b>Double-Speed Mode</b>					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4650	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz	-0.2	-	+0.7	dB	
StopBand	0.5770	-	-	Fs	
StopBand Attenuation (Note 14)	55	-	-	dB	
Group Delay	-	5/Fs	-	s	
<b>Quad-Speed Mode</b>					
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.397	Fs
	to -3 dB corner	0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz	-0.2	-	+0.05	dB	
StopBand	0.7	-	-	Fs	
StopBand Attenuation (Note 14)	51	-	-	dB	
Group Delay	-	2.5/Fs	-	s	

**Notes:**

13. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 34 to 45) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
14. Single- and Double-Speed Mode Measurement Bandwidth is from Stopband to 3 Fs.  
Quad-Speed Mode Measurement Bandwidth is from Stopband to 1.34 Fs.
15. De-emphasis is only available in Single-Speed Mode.

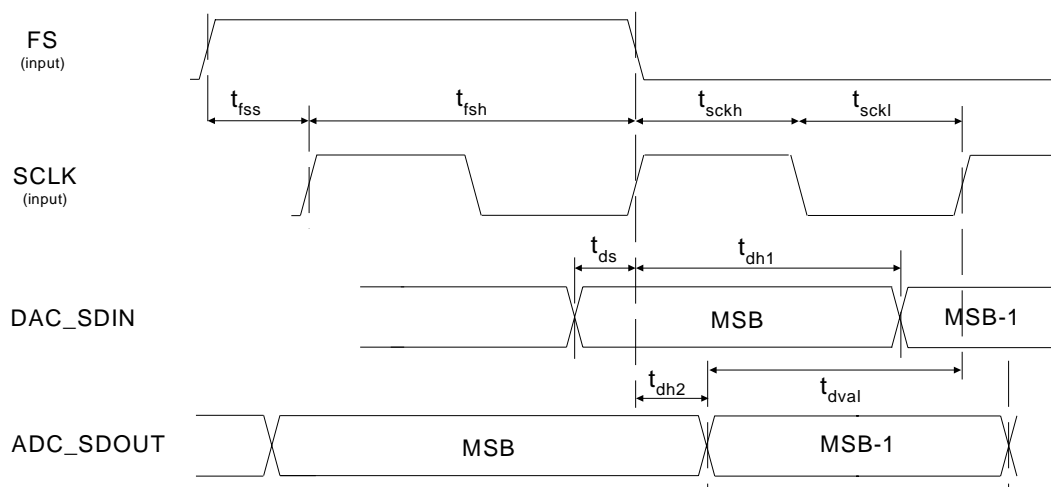
## SWITCHING SPECIFICATIONS - ADC/DAC PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS, ADC\_SDOOUT  $C_{LOAD}$  = 15 pF.)

Parameters	Symbol	Min	Max	Units	
<b>Slave Mode</b>					
RST pin Low Pulse Width (Note 16)		1	-	ms	
MCLK Frequency		0.512	50	MHz	
MCLK Duty Cycle (Note 17)		45	55	%	
Input Sample Rate (FS pin)	Single-Speed Mode	$F_s$	4	50	kHz
	Double-Speed Mode (Note 18)	$F_s$	50	100	kHz
	Quad-Speed Mode (Note 19)	$F_s$	100	200	kHz
SCLK Duty Cycle		45	55	%	
SCLK High Time	$t_{sckh}$	8	-	ns	
SCLK Low Time	$t_{sckl}$	8	-	ns	
FS Rising Edge to SCLK Rising Edge	$t_{fss}$	5	-	ns	
SCLK Rising Edge to FS Falling Edge	$t_{fsh}$	16	-	ns	
DAC_SDIN Setup Time Before SCLK Rising Edge	$t_{ds}$	3	-	ns	
DAC_SDIN Hold Time After SCLK Rising Edge	$t_{dh}$	5	-	ns	
DAC_SDIN Hold Time After SCLK Rising Edge	$t_{dh1}$	5	-	ns	
ADC_SDOOUT Hold Time After SCLK Rising Edge	$t_{dh2}$	10	-	ns	
ADC_SDOOUT Valid Before SCLK Rising Edge	$t_{dval}$	15	-	ns	

### Notes:

16. After powering up the CS42438,  $\overline{RST}$  should be held low after the power supplies and clocks are settled.
17. See [Table 7 on page 43](#) for suggested MCLK frequencies.
18. VLS is limited to nominal 2.5 V to 5.0 V operation only.
19. ADC does not meet timing specification for Quad-Speed Mode.

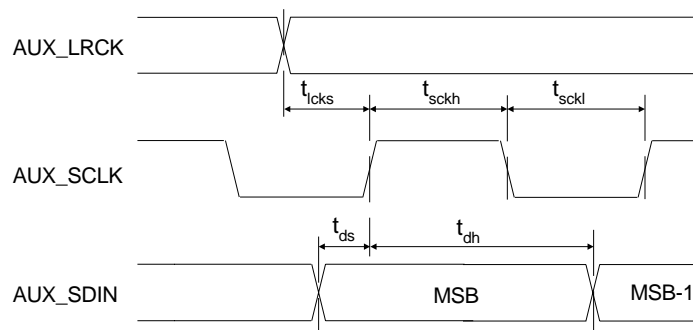


**Figure 5. TDM Serial Audio Interface Timing**

## SWITCHING CHARACTERISTICS - AUX PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLS.)

Parameters	Symbol	Min	Max	Units
<b>Master Mode</b>				
Output Sample Rate (AUX_LRCK) All Speed Modes	$F_s$	-	LRCK	kHz
AUX_SCLK Frequency		-	64•LRCK	kHz
AUX_SCLK Duty Cycle		45	55	%
AUX_LRCK Edge to SCLK Rising Edge	$t_{icks}$	-	5	ns
AUX_SDIN Setup Time Before SCLK Rising Edge	$t_{ds}$	3	-	ns
AUX_SDIN Hold Time After SCLK Rising Edge	$t_{dh}$	5	-	ns



**Figure 6. Serial Audio Interface Slave Mode Timing**

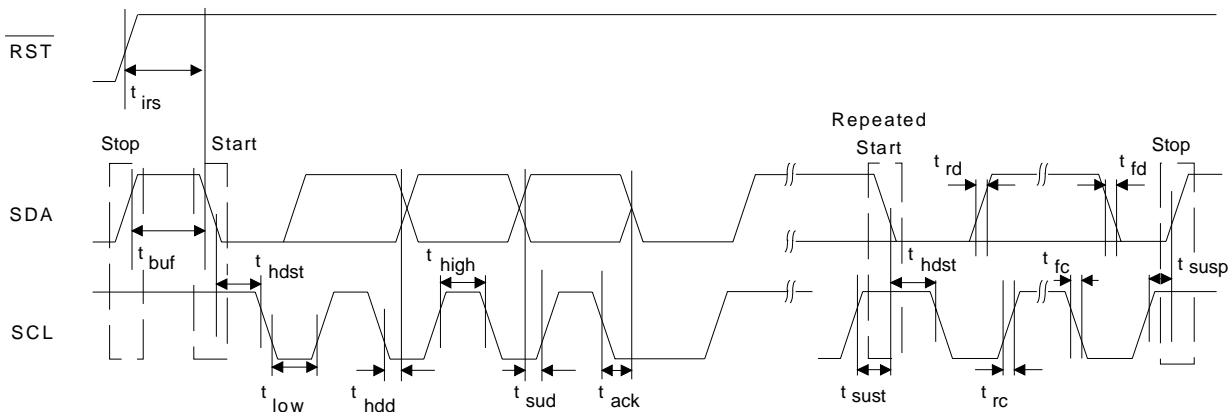
**SWITCHING SPECIFICATIONS - CONTROL PORT - I<sup>2</sup>C MODE**

 (VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, SDA C<sub>L</sub> = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f <sub>scl</sub>	-	100	kHz
RST Rising Edge to Start	t <sub>irs</sub>	500	-	ns
Bus Free Time Between Transmissions	t <sub>buf</sub>	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t <sub>hdst</sub>	4.0	-	μs
Clock Low time	t <sub>low</sub>	4.7	-	μs
Clock High Time	t <sub>high</sub>	4.0	-	μs
Setup Time for Repeated Start Condition	t <sub>sust</sub>	4.7	-	μs
SDA Hold Time from SCL Falling (Note 20)	t <sub>hdd</sub>	0	-	μs
SDA Setup time to SCL Rising	t <sub>sud</sub>	250	-	ns
Rise Time of SCL and SDA (Note 21)	t <sub>rc</sub>	-	1	μs
Fall Time SCL and SDA (Note 21)	t <sub>fc</sub>	-	300	ns
Setup Time for Stop Condition	t <sub>susp</sub>	4.7	-	μs
Acknowledge Delay from SCL Falling	t <sub>ack</sub>	300	1000	ns

**Notes:**

- 20. Data must be held for sufficient time to bridge the transition time, t<sub>fc</sub>, of SCL.
- 21. Guaranteed by design.


**Figure 7. Control Port Timing - I<sup>2</sup>C Format**

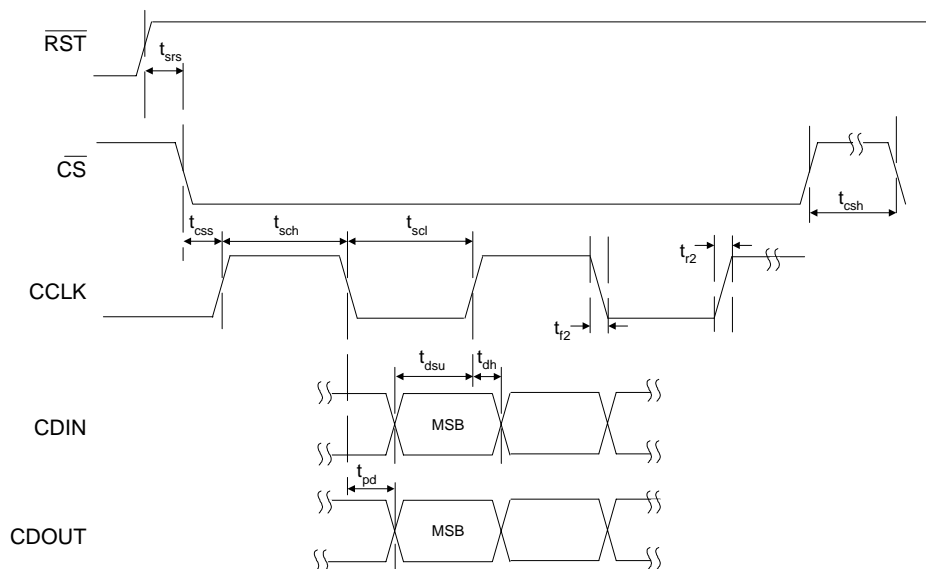
## SWITCHING SPECIFICATIONS - CONTROL PORT - SPI FORMAT

(VLC = 1.8 V - 5.0 V, VLS = VD = 3.3 V, VA = 5.0 V; Inputs: Logic 0 = DGND, Logic 1 = VLC, CDOUT C<sub>L</sub> = 30 pF)

Parameter	Symbol	Min	Max	Units
CCLK Clock Frequency	$f_{sck}$	0	6.0	MHz
RST Rising Edge to CS Falling	$t_{srs}$	20	-	ns
CS Falling to CCLK Edge	$t_{css}$	20	-	ns
CS High Time Between Transmissions	$t_{csh}$	1.0	-	μs
CCLK Low Time	$t_{scl}$	66	-	ns
CCLK High Time	$t_{sch}$	66	-	ns
CDIN to CCLK Rising Setup Time	$t_{dsu}$	40	-	ns
CCLK Rising to DATA Hold Time	$t_{dh}$	15	-	ns
CCLK Falling to CDOUT Stable	$t_{pd}$	-	50	ns
Rise Time of CDOUT	$t_{r1}$	-	25	ns
Fall Time of CDOUT	$t_{f1}$	-	25	ns
Rise Time of CCLK and CDIN	$t_{r2}$	-	100	ns
Fall Time of CCLK and CDIN	$t_{f2}$	-	100	ns

### Notes:

22. Data must be held for sufficient time to bridge the transition time of CCLK.
23. For  $f_{sck} < 1$  MHz.



**Figure 8. Control Port Timing - SPI Format**



## DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units
<b>Normal Operation (Note 24)</b>					
Power Supply Current VA = 5.0 V VLS = VLC = VD = 3.3 V (Note 25)	I <sub>A</sub>	-	80	-	mA
	I <sub>DT</sub>	-	60.6	-	mA
Power Dissipation VLS = VLC = VD = 3.3 V, VA = 5 V		-	600	850	mW
Power Supply Rejection Ratio (Note 26)	PSRR	1 kHz	60	-	dB
		60 Hz	40	-	dB
<b>Power-Down Mode (Note 27)</b>					
Power Dissipation VLS = VLC = VD = 3.3 V, VA = 5 V		-	1.25	-	mW
<b>VQ Characteristics</b>					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 28)		-	-	10	μA
FILT+ Nominal Voltage		-	VA	-	V

### Notes:

24. Normal operation is defined as  $\overline{RST} = HI$  with a 997 Hz, 0 dBFS input to the DAC and AUX port, and a 1 kHz, -1 dB analog input to the ADC port sampled at the highest  $F_s$  for each speed mode. DAC outputs are open, unless otherwise specified.
25. I<sub>DT</sub> measured with no external loading on pin 2 (SDA).
26. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.
27. Power-Down Mode is defined as  $\overline{RST} = LO$  with all clocks and data lines held static and no analog input.
28. Guaranteed by design. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.

## DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 29)	Symbol	Min	Typ	Max	Units
High-Level Output Voltage at I <sub>o</sub> =2 mA	Serial Port	VLS-1.0	-	-	V
	Control Port	VLC-1.0	-	-	V
Low-Level Output Voltage at I <sub>o</sub> =2 mA	Serial Port	-	-	0.4	V
	Control Port	-	-	0.4	V
High-Level Input Voltage	Serial Port	0.7xVLS	-	-	V
	Control Port	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	-	-	0.2xVLS	V
	Control Port	-	-	0.2xVLC	V
Leakage Current	I <sub>in</sub>	-	-	±10	μA
Input Capacitance (Note 21)		-	-	10	pF

### Notes:

29. See “Digital I/O Pin Characteristics” on page 8 for serial and control port power rails.

## 5. APPLICATIONS

### 5.1 Overview

The CS42438 is a highly integrated mixed signal 24-bit audio CODEC comprised of 6 analog-to-digital converters (ADC) implemented using multi-bit delta-sigma techniques and 8 digital-to-analog converters (DAC) also implemented using multi-bit delta-sigma techniques.

Other functions integrated within the CODEC include independent digital volume controls for each DAC, digital de-emphasis filters for the DAC, digital volume control with gain on each ADC channel, ADC high-pass filters, and an on-chip voltage reference,.

The serial audio interface ports allow up to 8 DAC channels and 8 ADC channels in a Time-Division Multiplexed (TDM) interface format. The CS42438 features an Auxiliary Port used to accommodate an additional two channels of PCM data on the ADC\_SDOOUT data line in the TDM digital interface format. See [“AUX Port Digital Interface Formats” on page 34](#) for details.

The CS42438 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined automatically based on the MCLK frequency setting. Single-Speed Mode (SSM) supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed Mode (DSM) supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed Mode (QSM) supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x (**Note:** QSM for the ADC is only supported in the I<sup>2</sup>S, Left-Justified, Right-Justified interface formats. QSM is not supported for the ADC). **Note:** QSM is only available in Software Mode (see [“System Clocking” on page 33](#) for details).

All functions can be configured through software via a serial control port operable in SPI Mode or in I<sup>2</sup>C Mode. A Hardware, Stand-Alone Mode is also available, allowing configuration of the CODEC on a more limited basis. See Table 2 for the default configuration in Hardware Mode.

[Figure 1 on page 11](#) and [Figure 2 on page 12](#) show the recommended connections for the CS42438 in Software and Hardware Mode, respectively. See [“Register Description” on page 41](#) for the default register settings and options in Software Mode.

Hardware Mode Feature Summary			
Function	Default Configuration	Hardware Control	Note
Power Down ADC	All ADC's are enabled	-	-
Power Down DAC	All DAC's are enabled	-	-
Power Down Device	Device is powered up	-	-
MCLK Frequency Select	Selectable between 256Fs and 512Fs	“MFREQ” pin 3	see <a href="#">Section 5.4</a>
Freeze Control	N/A	-	-
AUX Serial Port Interface Format	Left-Justified	-	-
ADC1/ADC2 High Pass Filter Freeze	High Pass Filter is always enabled	-	-
ADC3 High Pass Filter Freeze	High Pass Filter can be enabled/disabled	“ADC3_HPF” pin 4	see <a href="#">Section 5.2.5</a>
DAC De-Emphasis	No De-Emphasis applied	-	-
ADC1/ADC2 Single-Ended Mode	Disabled	-	-
ADC3 Single-Ended Mode	Selectable between Differential and Single-Ended	“ADC_SDOOUT/ADC3_SINGLE” pin 13	see <a href="#">Section 5.2.2</a>
AIN5 Multiplexer	Selects between AIN5A and AIN5B when ADC3 in Single-Ended Mode	“AIN5_MUX” pin 1	see <a href="#">Section 5.2.2</a>

**Table 2. Hardware Configurable Settings**

<b>Hardware Mode Feature Summary</b>			
<b>Function</b>	<b>Default Configuration</b>	<b>Hardware Control</b>	<b>Note</b>
AIN6 Multiplexer	Selects between AIN6A and AIN6B when ADC3 in Single-Ended Mode	"AIN6_MUX" pin 2	see <a href="#">Section 5.2.2</a>
DAC Volume Control/Mute/Invert	All DAC Volume = 0 dB, un-muted, not inverted	-	-
ADC Volume Control	All ADC Volume = 0 dB	-	-
DAC Soft Ramp/Zero Cross	Immediate Change	-	-
ADC Soft Ramp/Zero Cross	Immediate Change	-	-
DAC Auto-Mute	Enabled	-	-
Status Interrupt	N/A	-	-

**Table 2. Hardware Configurable Settings (Continued)**

## 5.2 Analog Inputs

### 5.2.1 Line-Level Inputs

AINx+ and AINx- are the line-level differential analog inputs internally biased to VQ, approximately VA/2. [Figure 9 on page 28](#) shows the full-scale analog input levels. The CS42438 also accommodates single-ended signals on all inputs, AIN1-AIN6. See ["ADC Input Filter" on page 50](#) for the recommended input filters.

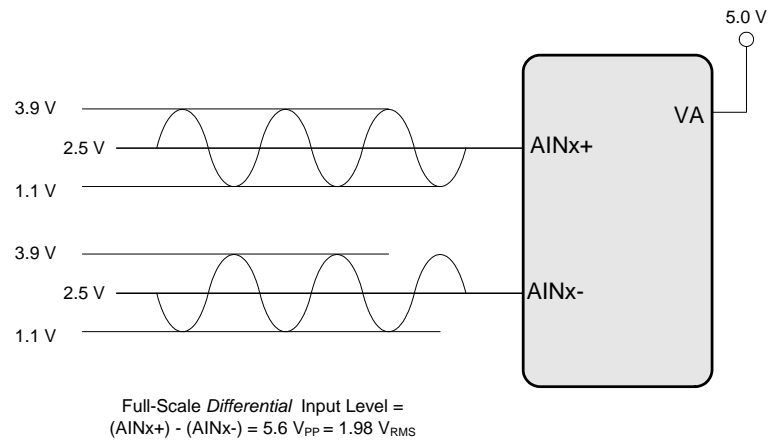
#### 5.2.1.1 Hardware Mode

AIN Volume Control and ADC Overflow status are not accessible in Hardware Mode. Single-ended operation is only supported for ADC3. See [Section 5.2.2](#).

#### 5.2.1.2 Software Mode

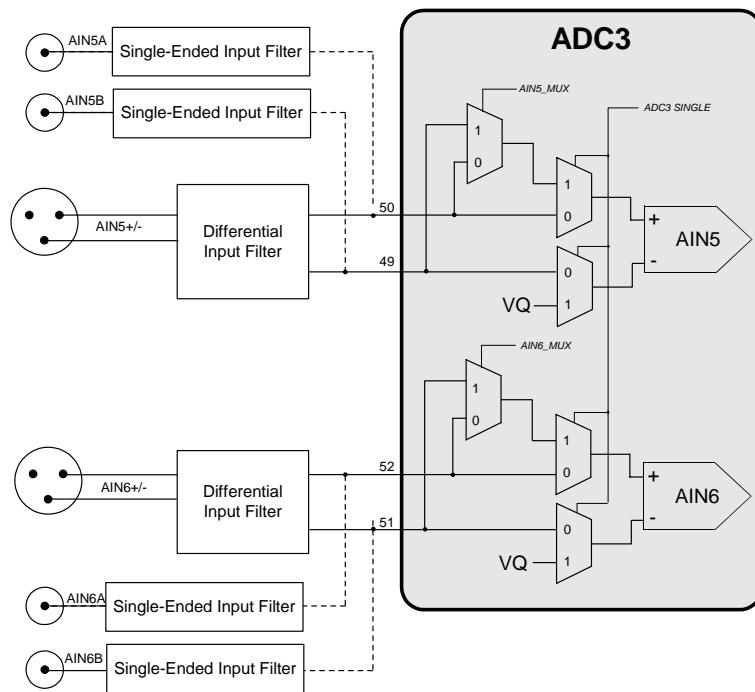
For single-ended operation on ADC1-ADC3 (AIN1 to AIN6), the ADCx\_SINGLE bit in the register ["ADC Control & DAC De-Emphasis \(Address 05h\)" on page 44](#) must be set appropriately (see [Figure 21 on page 50](#) for required external components).

The gain/attenuation of the signal can be adjusted for each AINx independently through the ["AINX Volume Control \(Address 11h-16h\)" on page 48](#). The ADC output data is in 2's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFFH or 800000H, respectively, and cause the ADC Overflow bit in the register ["Status \(Address 19h\) \(Read Only\)" on page 49](#) to be set to a '1'.


**Figure 9. Full-Scale Input**

### 5.2.2 ADC3 Analog Input

ADC3 accommodates differential as well as single-ended inputs. In Single-Ended Mode, an internal MUX selects from up to four single-ended inputs.


**Figure 10. ADC3 Input Topology**

### 5.2.3 Hardware Mode

Single-Ended Mode is selected using a pull-up on the ADC\_SDOUT/ADC3\_SINGLE pin during startup. Analog input selection is then made via the AINx\_MUX pins. See [Tables 3-4](#) for ADC3 set-up options. Refer to [Figure 10 on page 28](#) for the internal ADC3 analog input topology.

Configuration Setting		AIN5 Input Selection
ADC_SDOUT (pin 13)	AIN5_MUX (pin 1)	
47 kΩ Pull-down	X	Differential Input (pins 50 & 49)
47 kΩ Pull-up	Low	AIN5A Input (pin 50)
47 kΩ Pull-up	High	AIN5B Input (pin 49)

**Table 3. AIN5 Analog Input Selection**

Configuration Setting		AIN6 Input Selection
ADC_SDOUT (pin 13)	AIN6_MUX (pin 2)	
47 kΩ Pull-down	X	Differential Input (pins 52 & 51)
47 kΩ Pull-up	Low	AIN5A Input (pin 52)
47 kΩ Pull-up	High	AIN5B Input (pin 51)

**Table 4. AIN6 Analog Input Selection**

### 5.2.4 Software Mode

Single-Ended Mode is selected using the ADC3\_SINGLE bit. Analog input selection is then made via the AINx\_MUX bits. See register “[ADC Control & DAC De-Emphasis \(Address 05h\)](#)” on [page 44](#) for all bit selections. Refer to [Figure 11 on page 31](#) for the internal ADC3 analog input topology.

### 5.2.5 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is disabled during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS42438 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

#### 5.2.5.1 Hardware Mode

The high pass filters for ADC1 and ADC2 are permanently enabled in Hardware Mode. The high pass filter for ADC3 is enabled by driving the ADC3\_HPF (pin 4) high.

#### 5.2.5.2 Software Mode

The high-pass filter for ADC1/ADC2 can be enabled and disabled. The high pass filter for ADC3 can be independently enabled and disabled. The high-pass filters are controlled using the HPF\_FREEZE bit in the register “[ADC Control & DAC De-Emphasis \(Address 05h\)](#)” on [page 44](#).

## 5.3 Analog Outputs

### 5.3.1 Initialization

The initialization and Power-Down sequence flow chart is shown in [Figure 11 on page 31](#). The CS42438 enters a power-down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, multi-bit digital-to-analog and analog-to-digital converters and switched-capacitor low-pass filters are powered down.

The device remains in the power-down state until the  $\overline{\text{RST}}$  pin is brought high. The control port is accessible once  $\overline{\text{RST}}$  is high, and the desired register settings can be loaded per the interface descriptions in the [“Control Port Description and Timing” on page 35](#). In Hardware Mode operation, the Hardware Mode pins must be set up before  $\overline{\text{RST}}$  is brought high. All features will default to the Hardware Mode defaults as listed in [Table 2](#).

Once MCLK is valid, VQ will quickly charge to  $V_A/2$ , and the internal voltage reference, FILT+, will begin powering up to normal operation. Power is applied to the D/A converters and switched-capacitor filters, and the analog outputs are clamped to the quiescent voltage, VQ. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. After an approximate 2000 sample period delay, normal operation begins.

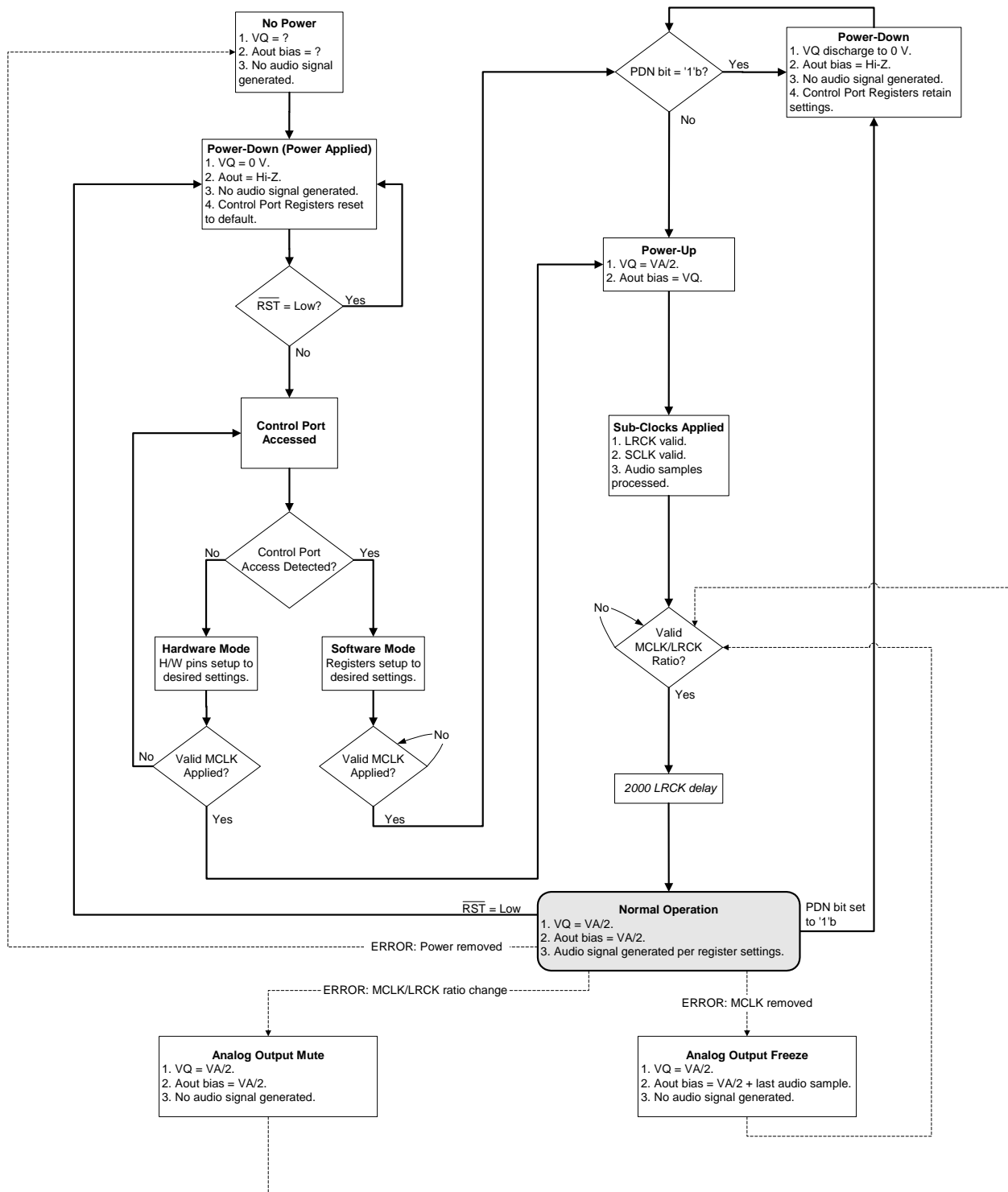
### 5.3.2 Line-Level Outputs and Filtering

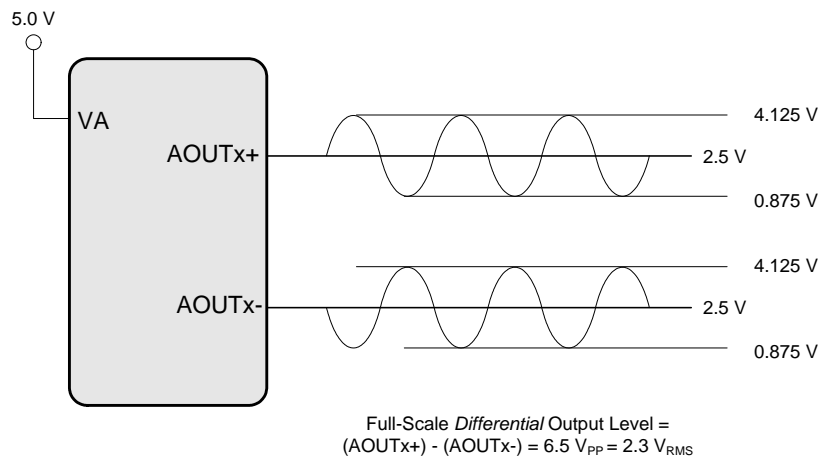
The CS42438 contains on-chip buffer amplifiers capable of producing line-level differential as well as single-ended outputs on AOUT1-AOUT8. These amplifiers are biased to a quiescent DC level of approximately VQ.

The delta-sigma conversion process produces high-frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low-pass filter.

See [“DAC Output Filter” on page 53](#) for recommended output filter. The active filter configuration accounts for the normally differing AC loads on the AOUTx+ and AOUTx- differential output pins. Also shown is a passive filter configuration which minimizes costs and the number of components.

[Figure 12](#) shows the full-scale analog output levels. All outputs are internally biased to VQ, approximately  $V_A/2$ .


**Figure 11. Audio Output Initialization Flow Chart**



**Figure 12. Full-Scale Output**

### 5.3.3 Digital Volume Control

#### 5.3.3.1 Hardware Mode

DAC Volume Control and Mute are not accessible in Hardware Mode.

#### 5.3.3.2 Software Mode

Each DAC's output level is controlled via the Volume Control registers operating over the range of 0 to -127.5 dB attenuation with 0.5 dB resolution. See [“AOUTX Volume Control \(Addresses 08h- 0Fh\)” on page 47](#). Volume control changes are programmable to ramp in increments of 0.125 dB at the rate controlled by the SZC[1:0] bits in the Digital Volume Control register. See [“Transition Control \(Address 06h\)” on page 46](#).

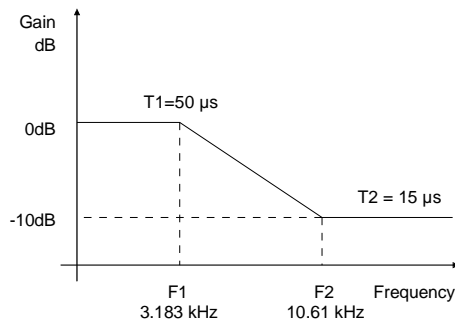
Each output can be independently muted via mute control bits in the register [“DAC Channel Mute \(Address 07h\)” on page 47](#). When enabled, each AOUTx\_MUTE bit attenuates the corresponding DAC to its maximum value (-127.5 dB). When the AOUTx\_MUTE bit is disabled, the corresponding DAC returns to the attenuation level set in the Volume Control register. The attenuation is ramped up and down at the rate specified by the SZC[1:0] bits.

### 5.3.4 De-Emphasis Filter

The CS42438 includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in [Figure 13](#). The de-emphasis feature is included to accommodate audio recordings that utilize 50/15  $\mu$ s pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single-Speed Mode. Please see [“DAC De-Emphasis Control \(DAC\\_DEM\)” on page 44](#) for de-emphasis control.





**Figure 13. De-Emphasis Curve**

## 5.4 System Clocking

The CODEC serial audio interface ports operate as a slave and accept externally generated clocks.

The CODEC requires external generation of the master clock (MCLK). The frequency of this clock must be an integer multiple of, and synchronous with, the system sample rate,  $F_s$ .

### 5.4.1 Hardware Mode

The allowable ratios include 256 $F_s$  and 512 $F_s$  in Single-Speed Mode and 256 $F_s$  in Double-Speed Mode. The frequency of MCLK must be specified using the MFREQ (pin 3). See [Table 5](#) for the required frequency range.

MFREQ	Description	Ratio (x $F_s$ )		
		SSM	DSM	QSM
0	1.5360 MHz to 12.8000 MHz	256	N/A	N/A
1	2.0480 MHz to 25.6000 MHz	512	256	N/A

**Table 5. MCLK Frequency Settings**

### 5.4.2 Software Mode

The frequency range of MCLK must be specified using the MFREQ bits in register “MCLK Frequency (MFREQ[2:0])” on [page 43](#).

## 5.5 CODEC Digital Interface

The ADC and DAC serial ports operate as a slave and support the TDM digital interface formats with varying bit depths from 16 to 32 as shown in . Data is clocked out of the ADC on the falling edge of SCLK and clocked into the DAC on the rising edge.

TDM is the only interface supported in Hardware and Software Mode.

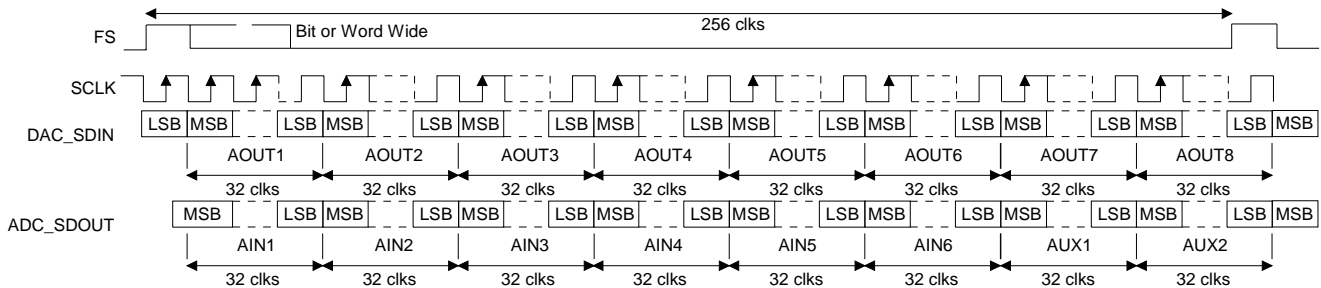
### 5.5.1 TDM

TDM data is received most significant bit (MSB) first, on the second rising edge of the SCLK occurring after a an FS rising edge. All data is valid on the rising edge of SCLK. The AIN1 MSB is transmitted early, but is guaranteed valid for a specified time after SCLK rises. All other bits are transmitted on the falling edge of SCLK. Each time slot is 32 bits wide, with the valid data sample left ‘justified within the time slot. Valid data lengths are 16, 18, 20, or 24.

SCLK must operate at 256 $F_s$ . FS identifies the start of a new frame and is equal to the sample rate,  $F_s$ .

FS is sampled as valid on the rising SCLK edge preceding the most significant bit of the first data sample and must be held valid for at least 1 SCLK period.

**Note:** The ADC does not meet the timing requirements for proper operation in Quad-Speed Mode.



**Figure 14. TDM Serial Audio Format**

### 5.5.2 I/O Channel Allocation

Digital Input/Output	Interface Format	Analog Output/Input Channel Allocation from/to Digital I/O
DAC_SDIN	TDM	AOUT 1,2,3,4,5,6,7,8
ADC_SDOUT	TDM	,5,6AIN 1,2,3,4,5,6; (2 additional channels from AUX_SDIN)

**Table 6. Serial Audio Interface Channel Allocations**

## 5.6 AUX Port Digital Interface Formats

These serial data lines are used when supporting the TDM Mode of operation with an external ADC or S/PDIF receiver attached. The AUX serial port operates only as a clock master. The AUX\_SCLK will operate at  $64 \times F_s$ , where  $F_s$  is equal to the ADC sample rate (FS on the TDM interface). If the AUX\_SDIN signal is not being used, it should be tied to AGND via a pull-down resistor.

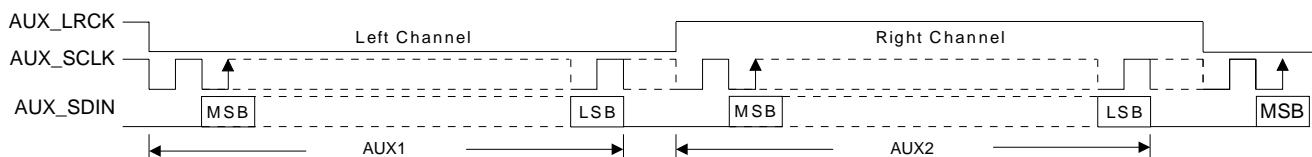
### 5.6.1 Hardware Mode

The AUX port will only operate in the Left-Justified digital interface format and supports bit depths ranging from 16 to 24 bits (see [Figure 18 on page 36](#) for timing relationship between AUX\_LRCK and AUX\_SCLK).

### 5.6.2 Software Mode

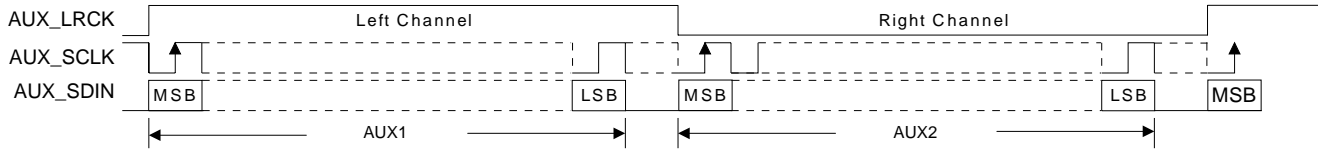
The AUX port will operate in either the Left-Justified or I<sup>2</sup>S digital interface format with bit depths ranging from 16 to 24 bits. Settings for the AUX port are made through the register “Miscellaneous Control (Address 04h)” on [page 43](#).

### 5.6.3 I<sup>2</sup>S



**Figure 15. AUX I<sup>2</sup>S Format**

### 5.6.4 Left-Justified



**Figure 16. AUX Left-Justified Format**

## 5.7 Control Port Description and Timing

The control port is used to access the registers, in Software Mode, allowing the CS42438 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I<sup>2</sup>C, with the CS42438 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/ $\overline{\text{CS}}$  pin, after the RST pin has been brought high. I<sup>2</sup>C Mode is selected by connecting the AD0/ $\overline{\text{CS}}$  pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

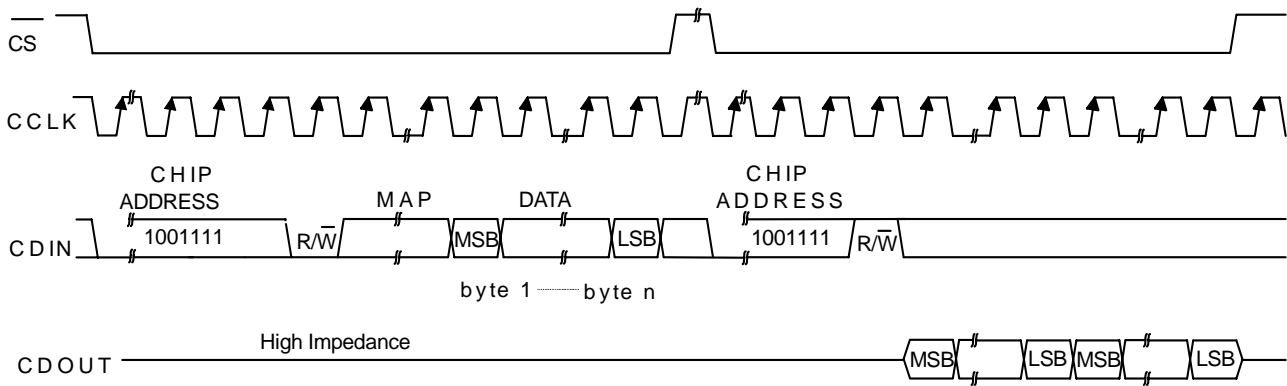
### 5.7.1 SPI Mode

In SPI Mode,  $\overline{\text{CS}}$  is the CS42438 chip-select signal, CCLK is the control port bit clock (input into the CS42438 from the microcontroller), CDIN is the input data line from the microcontroller, CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 17 shows the operation of the control port in SPI Mode. To write to a register, bring  $\overline{\text{CS}}$  low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/W), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 k $\Omega$  resistor, if desired.

There is a MAP auto-increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ( $\overline{\text{CS}}$  high) immediately after the MAP byte. The MAP auto-increment bit (INCR) may be set or not, as desired. To begin a read, bring  $\overline{\text{CS}}$  low, send out the chip address and set the read/write bit (R/W) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto-increment bit is set to 1, the data for successive registers will appear consecutively.



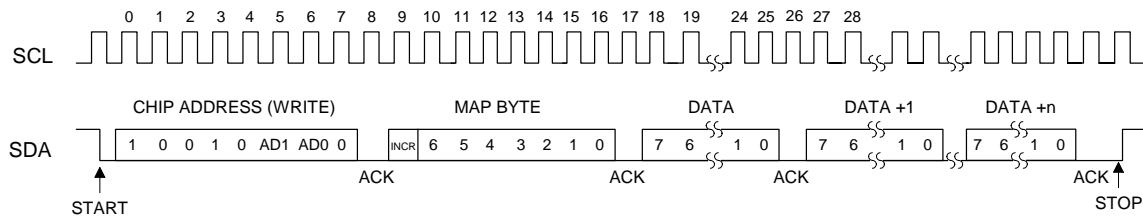
MAP = Memory Address Pointer, 8 bits, MSB first

**Figure 17. Control Port Timing in SPI Mode**

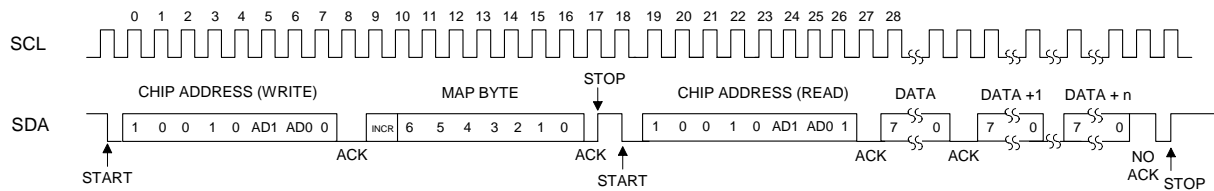
### 5.7.2 I<sup>2</sup>C Mode

In I<sup>2</sup>C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no CS pin. Pins AD0 and AD1 form the two least-significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS42438 is being reset.

The signal timings for a read and write cycle are shown in Figure 18 and Figure 19. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42438 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10010. To communicate with a CS42438, the chip address field, which is the first byte sent to the CS42438, should match 10010 followed by the settings of the AD1 and AD0. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42438 after each input byte is read, and is input to the CS42438 from the microcontroller after each transmitted byte.



**Figure 18. Control Port Timing, I<sup>2</sup>C Write**



**Figure 19. Control Port Timing, I<sup>2</sup>C Read**

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in [Figure 19](#), the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 10010xx0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 10010xx1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

## 5.8 Recommended Power-Up Sequence

### 5.8.1 Hardware Mode

1. Hold  $\overline{\text{RST}}$  low until the power supply, clocks and hardware control pins are stable. In this state, the control port is reset to its default settings and VQ will remain low.
2. Bring  $\overline{\text{RST}}$  high. The device will initially be in a low power state with VQ low.
3. The device will initiate the Hardware Mode power up sequence. All features will default to the Hardware Mode defaults as listed in [Table 2 on page 26](#) according to the Hardware Mode control pins. VQ will quick-charge to approximately VA/2 and the analog output bias will clamp to VQ.
4. Following approximately 2000 sample periods, the device is initialized and ready for normal operation.

**Note:** During the Hardware Mode power-up sequence, there must be no transitions on any of the hardware control pins.

### 5.8.2 Software Mode

1. Hold  $\overline{\text{RST}}$  low until the power supply and clocks are stable. In this state, the control port is reset to its default settings and VQ will remain low.
2. Bring  $\overline{\text{RST}}$  high. The device will initially be in a low power state with VQ low. All features will default as described in the [“Register Quick Reference” on page 39](#).
3. Perform a write operation to the Power Control register ([“Power Control \(Address 02h\)” on page 42](#)) to set bit 0 to a ‘1’b. This will place the device in a power down state.
4. Load the desired register settings while keeping the PDN bit set to ‘1’b.
5. Mute all DACs. Muting the DACs suppresses any noise associated with the CODEC's first initialization after power is applied.
6. Set the PDN bit in the power control register to ‘0’b. Following approximately 2000 LRCK cycles, the device is initialized and ready for normal operation.
7. After the CODEC is initialized, wait ~90 LRCK cycles (~1.9 ms @48 kHz) and then unmute the DACs.
8. Normal operation begins.

### 5.9 Reset and Power-Up

It is recommended that reset be activated if the analog or digital supplies drop below the recommended operating condition to prevent power-glitch-related issues.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the  $\overline{\text{RST}}$  pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the FILT+ pin. A time delay of approximately 400 ms is required after applying power to the device or after exiting a reset state. During this voltage reference ramp delay, all serial ports and DAC outputs will be automatically muted.

### 5.10 Power Supply, Grounding, and PCB Layout

As with any high-resolution converter, the CS42438 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Figures 1 and 2](#) show the recommended power arrangements, with VA connected to clean supplies. VD, which powers the digital circuitry, may be run from the system logic supply.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS42438 as possible. The low value ceramic capacitor should be the nearest to the pin and should be mounted on the same side of the board as the CS42438 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+, VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1  $\mu\text{F}$ , must be positioned to minimize the electrical path from FILT+ and AGND. The CDB42438 evaluation board demonstrates the optimum layout and power supply arrangements.

For optimal heat dissipation from the package, it is recommended that the area directly under the part be filled with copper and tied to the ground plane. The use of vias connecting the topside ground to the backside ground is also recommended.

## 6. REGISTER QUICK REFERENCE

Software Mode register defaults are as shown. **Note:** The default value in all “Reserved” registers must be preserved.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID p 41 default	Chip_ID3 0	Chip_ID2 0	Chip_ID1 0	Chip_ID0 0	Rev_ID3 0	Rev_ID2 0	Rev_ID1 0	Rev_ID0 1
02h	Power Control p 42 default	PDN_ADC3 0	PDN_ADC2 0	PDN_ADC1 0	PDN_DAC4 0	PDN_DAC3 0	PDN_DAC2 0	PDN_DAC1 0	PDN 0
03h	Functional Mode p 43 default	Reserved 1	Reserved 1	Reserved 1	Reserved 1	MFreq2 0	MFreq1 0	MFreq0 0	Reserved 0
04h	Misc Control p 43 default	FREEZE 0	AUX_DIF 0	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 1	Reserved 0
05h	ADC Control (w/DAC_DEM) p 44 default	ADC1-2_HPF FREEZE 0	ADC3_HPF FREEZE 0	DAC_DEM 0	ADC1 SINGLE 0	ADC2 SINGLE 0	ADC3 SINGLE 0	AIN5_MUX 0	AIN6_MUX 0
06h	Transition Control p 46 default	DAC_SNG VOL 0	DAC_SZC1 0	DAC_SZC0 0	AMUTE 1	MUTE ADC_SP 0	ADC_SNG VOL 0	ADC_SZC1 0	ADC_SZC0 0
07h	Channel Mute p 47 default	AOUT8 MUTE 0	AOUT7 MUTE 0	AOUT6 MUTE 0	AOUT5 MUTE 0	AOUT4 MUTE 0	AOUT3 MUTE 0	AOUT2 MUTE 0	AOUT1 MUTE 0
08h	Vol. Control AOUT1 p 47 default	AOUT1 VOL7 0	AOUT1 VOL6 0	AOUT1 VOL5 0	AOUT1 VOL4 0	AOUT1 VOL3 0	AOUT1 VOL2 0	AOUT1 VOL1 0	AOUT1 VOL0 0
09h	Vol. Control AOUT2 p 47 default	AOUT2 VOL7 0	AOUT2 VOL6 0	AOUT2 VOL5 0	AOUT2 VOL4 0	AOUT2 VOL3 0	AOUT2 VOL2 0	AOUT2 VOL1 0	AOUT2 VOL0 0
0Ah	Vol. Control AOUT3 p 47 default	AOUT3 VOL7 0	AOUT3 VOL6 0	AOUT3 VOL5 0	AOUT3 VOL4 0	AOUT3 VOL3 0	AOUT3 VOL2 0	AOUT3 VOL1 0	AOUT3 VOL0 0
0Bh	Vol. Control AOUT4 p 47 default	AOUT4 VOL7 0	AOUT4 VOL6 0	AOUT4 VOL5 0	AOUT4 VOL4 0	AOUT4 VOL3 0	AOUT4 VOL2 0	AOUT4 VOL1 0	AOUT4 VOL0 0
0Ch	Vol. Control AOUT5 p 47 default	AOUT5 VOL7 0	AOUT5 VOL6 0	AOUT5 VOL5 0	AOUT5 VOL4 0	AOUT5 VOL3 0	AOUT5 VOL2 0	AOUT5 VOL1 0	AOUT5 VOL0 0
0Dh	Vol. Control AOUT6 p 47 default	AOUT6 VOL7 0	AOUT6 VOL6 0	AOUT6 VOL5 0	AOUT6 VOL4 0	AOUT6 VOL3 0	AOUT6 VOL2 0	AOUT6 VOL1 0	AOUT6 VOL0 0
0Eh	Vol. Control AOUT7 p 47 default	AOUT7 VOL7 0	AOUT7 VOL6 0	AOUT7 VOL5 0	AOUT7 VOL4 0	AOUT7 VOL3 0	AOUT7 VOL2 0	AOUT7 VOL1 0	AOUT7 VOL0 0
0Fh	Vol. Control AOUT8 p 47 default	AOUT8 VOL7 0	AOUT8 VOL6 0	AOUT8 VOL5 0	AOUT8 VOL4 0	AOUT8 VOL3 0	AOUT8 VOL2 0	AOUT8 VOL1 0	AOUT8 VOL0 0
10h	DAC Channel Invert p 48 default	INV_AOUT8 0	INV_AOUT7 0	INV_AOUT6 0	INV_AOUT5 0	INV_AOUT4 0	INV_AOUT3 0	INV_AOUT2 0	INV_AOUT1 0

Addr	Function	7	6	5	4	3	2	1	0
11h	Vol. Control AIN1 <a href="#">p 47</a> default	AIN1 VOL7 0	AIN1 VOL6 0	AIN1 VOL5 0	AIN1 VOL4 0	AIN1 VOL3 0	AIN1 VOL2 0	AIN1 VOL1 0	AIN1 VOL0 0
12h	Vol. Control AIN2 <a href="#">p 48</a> default	AIN2 VOL7 0	AIN2 VOL6 0	AIN2 VOL5 0	AIN2 VOL4 0	AIN2 VOL3 0	AIN2 VOL2 0	AIN2 VOL1 0	AIN2 VOL0 0
13h	Vol. Control AIN3 <a href="#">p 47</a> default	AIN3 VOL7 0	AIN3 VOL6 0	AIN3 VOL5 0	AIN3 VOL4 0	AIN3 VOL3 0	AIN3 VOL2 0	AIN3 VOL1 0	AIN3 VOL0 0
14h	Vol. Control AIN4 <a href="#">p 48</a> default	AIN4 VOL7 0	AIN4 VOL6 0	AIN4 VOL5 0	AIN4 VOL4 0	AIN4 VOL3 0	AIN4 VOL2 0	AIN4 VOL1 0	AIN4 VOL0 0
15h	Vol. Control AIN5 <a href="#">p 47</a> default	AIN5 VOL7 0	AIN5 VOL6 0	AIN5 VOL5 0	AIN5 VOL4 0	AIN5 VOL3 0	AIN5 VOL2 0	AIN5 VOL1 0	AIN5 VOL0 0
16h	Vol. Control AIN6 <a href="#">p 48</a> default	AIN6 VOL7 0	AIN6 VOL6 0	AIN6 VOL5 0	AIN6 VOL4 0	AIN6 VOL3 0	AIN6 VOL2 0	AIN6 VOL1 0	AIN6 VOL0 0
17h	ADC Chan- nel Invert <a href="#">p 48</a> default	Reserved 0	Reserved 0	INV_A6 0	INV_A5 0	INV_A4 0	INV_A3 0	INV_A2 0	INV_A1 0
18h	Reserved default	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
19h	Status <a href="#">p 49</a> default	Reserved 0	Reserved 0	Reserved 0	Reserved X	CLK Error X	ADC3 OVFL X	ADC2 OVFL X	ADC1 OVFL X
1Ah	Status Mask <a href="#">p 49</a> default	Reserved 0	Reserved 0	Reserved 0	Reserved 0	CLK Error_M 0	ADC3 OVFL_M 0	ADC2 OVFL_M 0	ADC1 OVFL_M 0



## 7. REGISTER DESCRIPTION

All registers are read/write except for the I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit-definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.

### 7.1 Memory Address Pointer (MAP)

Not a register

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

#### 7.1.1 Increment (INCR)

Default = 1

Function:

Memory address pointer auto increment control

0 - MAP is not incremented automatically.

1 - Internal MAP is automatically incremented after each read or write.

#### 7.1.2 Memory Address Pointer (MAP[6:0])

Default = 0000001

Function:

Memory address pointer (MAP). Sets the register address that will be read or written by the control port.

## 7.2 Chip I.D. and Revision Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID3	Rev_ID2	Rev_ID1	Rev_ID0

#### 7.2.1 Chip I.D. (CHIP\_ID[3:0])

Default = 0000

Function:

I.D. code for the CS42438. Permanently set to 0000.

#### 7.2.2 Chip Revision (REV\_ID[3:0])

Default = 0001

Function:

CS42438 revision level. Revision A is coded as 0001.

### 7.3 Power Control (Address 02h)

7	6	5	4	3	2	1	0
PDN_ADC3	PDN_ADC2	PDN_ADC1	PDN_DAC4	PDN_DAC3	PDN_DAC2	PDN_DAC1	PDN

#### 7.3.1 Power Down ADC Pairs (PDN\_ADCX)

Default = 0

0 - Disable

1 - Enable

Function:

When enabled, the respective ADC channel pair (ADC1 - AIN1/AIN2; ADC2 - AIN3/AIN4; and ADC3 - AIN5/AIN6) will remain in a reset state.

#### 7.3.2 Power Down DAC Pairs (PDN\_DACX)

Default = 0

0 - Disable

1 - Enable

Function:

When enabled, the respective DAC channel pair (DAC1 - AOUT1/AOUT2; DAC2 - AOUT3/AOUT4; DAC3 - AOUT5/AOUT6; and DAC4 - AOUT7/AOUT8) will remain in a reset state. It is advised that any change of these bits be made while the DACs are muted or the power down bit (PDN) is enabled to eliminate the possibility of audible artifacts.

#### 7.3.3 Power Down (PDN)

Default = 0

0 - Disable

1 - Enable

Function:

The entire device will enter a low-power state when this function is enabled. The contents of the control registers are retained in this mode.

## 7.4 Functional Mode (Address 03h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	MFreq2	MFreq1	MFreq0	Reserved

### 7.4.1 MCLK Frequency (MFREQ[2:0])

Default = 000

Function:

Sets the appropriate frequency for the supplied MCLK. For TDM operation, SCLK must equal 256Fs. MCLK can be equal to or greater than SCLK.

				Ratio (xFs)		
MFreq2	MFreq1	MFreq0	Description	SSM	DSM	QSM
0	0	0	1.0290 MHz to 12.8000 MHz	256	N/A	N/A
0	0	1	1.5360 MHz to 19.2000 MHz	384	N/A	N/A
0	1	0	2.0480 MHz to 25.6000 MHz	512	256	N/A
0	1	1	3.0720 MHz to 38.4000 MHz	768	384	N/A
1	X	X	4.0960 MHz to 51.2000 MHz	1024	512	256

Table 7. MCLK Frequency Settings

## 7.5 MISCELLANEOUS CONTROL (Address 04h)

7	6	5	4	3	2	1	0
FREEZE	AUX_DIF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

### 7.5.1 Freeze Controls (FREEZE)

Default = 0

Function:

This function will freeze the previous settings of, and allow modifications to be made to the channel mutes, the DAC and ADC Volume Control/Channel Invert registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in these control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

### 7.5.2 Auxiliary Digital Interface Format (AUX\_DIF)

Default = 0

0 - Left Justified

1 - I<sup>2</sup>S

Function:

This bit selects the digital interface format used for the AUX Serial Port. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in [Figures 17-18](#).

## 7.6 ADC Control & DAC De-Emphasis (Address 05h)

7	6	5	4	3	2	1	0
ADC1-2_HPF FREEZE	ADC3_HPF FREEZE	DAC_DEM	ADC1 SINGLE	ADC2 SINGLE	ADC3 SINGLE	AIN5_MUX	AIN6_MUX

### 7.6.1 ADC1-2 High-Pass Filter Freeze (ADC1-2\_HPF FREEZE)

Default = 0

Function:

When this bit is set, the internal high-pass filter will be disabled for ADC1 and ADC2. The current DC offset value will be frozen and continue to be subtracted from the conversion result. See [“ADC Digital Filter Characteristics” on page 16](#).

### 7.6.2 ADC3 High Pass Filter Freeze (ADC3\_HPF FREEZE)

Default = 0

Function:

When this bit is set, the internal high-pass filter will be disabled for ADC3. The current DC offset value will be frozen and continue to be subtracted from the conversion result. See [“ADC Digital Filter Characteristics” on page 16](#).

### 7.6.3 DAC De-Emphasis Control (DAC\_DEM)

Default = 0

- 0 - No De-Emphasis
- 1 - De-Emphasis Enabled (Auto-Detect Fs)

Function:

Enables the digital filter to maintain the standard 15 $\mu$ s/50 $\mu$ s digital de-emphasis filter response at the auto-detected sample rate of either 32, 44.1, or 48 kHz. De-emphasis will not be enabled, regardless of this register setting, at any other sample rate.

### 7.6.4 ADC1 Single-Ended Mode (ADC1 SINGLE)

Default = 0

- 0 - Disabled; Differential input to ADC1
- 1 - Enabled; Single-Ended input to ADC1

Function:

When enabled, this bit allows the user to apply a single-ended input to the positive terminal of ADC1. A +6 dB digital gain is automatically applied to the serial audio data of ADC1. The negative leg must be driven to the common mode of the ADC. See [Figure 21 on page 50](#) for a graphical description.

### 7.6.5 **ADC2 Single-Ended Mode (ADC2 SINGLE)**

Default = 0

- 0 - Disabled; Differential input to ADC2
- 1 - Enabled; Single-Ended input to ADC2

Function:

When enabled, this bit allows the user to apply a single-ended input to the positive terminal of ADC2. A +6 dB digital gain is automatically applied to the serial audio data of ADC2. The negative leg must be driven to the common mode of the ADC. See [Figure 21 on page 50](#) for a graphical description.

### 7.6.6 **ADC3 Single-Ended Mode (ADC3 SINGLE)**

Default = 0

- 0 - Disabled; Differential input to ADC
- 1 - Enabled; Single-Ended input to ADC

Function:

When disabled, this bit removes the 4:2 multiplexer from the signal path of ADC3 allowing a differential input. When enabled, this bit allows the user to choose between four single-ended inputs to ADC3, using the AIN5\_MUX and AIN6\_MUX bits. See [Figure 11 on page 31](#) and [Figure 21 on page 50](#) for graphical descriptions.

### 7.6.7 **Analog Input Ch. 5 Multiplexer (AIN5\_MUX)**

Default = 0

- 0 - Single-Ended Input AIN5A
- 1 - Single-Ended Input AIN5B

Function:

ADC3 can accept single-ended input signals when the ADC3 SINGLE bit is enabled. The AIN5\_MUX bit selects between two input channels (AIN5A or AIN5B) to be sent to ADC3 in Single-Ended Mode. This bit is ignored when the ADC3\_SINGLE bit is disabled. See [Figure 11 on page 31](#) for a graphical description.

### 7.6.8 **Analog Input Ch. 6 Multiplexer (AIN6\_MUX)**

Default = 0

- 0 - Single-Ended Input AIN6A
- 1 - Single-Ended Input AIN6B

Function:

ADC3 can accept a single-ended input signal when the ADC3 SINGLE bit is enabled. The AIN6\_MUX bit selects between two input channels (AIN6A or AIN6B) to be sent to ADC3 in Single-Ended Mode. This bit is ignored when the ADC3\_SINGLE bit is disabled. See [Figure 11 on page 31](#) for a graphical description.

## 7.7 Transition Control (Address 06h)

7	6	5	4	3	2	1	0
DAC_SNGVOL	DAC_SZC1	DAC_SZC0	AMUTE	MUTE_ADC_SP	ADC_SNGVOL	ADC_SZC1	ADC_SZC0

### 7.7.1 Single Volume Control (DAC\_SNGVOL, ADC\_SNGVOL)

Default = 0

Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the AOUT1 and AIN1 Volume Control register and the other Volume Control registers are ignored.

### 7.7.2 Soft Ramp and Zero Cross Control (ADC\_SZC[1:0], DAC\_SZC[1:0])

Default = 00

00 - Immediate Change

01 - Zero Cross

10 - Soft Ramp

11 - Soft Ramp on Zero Crossings

Function:

#### Immediate Change

When Immediate Change is selected, all volume-level changes will take effect immediately in one step.

#### Zero Cross

Zero Cross Enable dictates that signal level changes, either by gain changes, attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

#### Soft Ramp

Soft Ramp allows level changes, either by gain changes, attenuation changes or muting, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

#### Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by gain changes, attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

### 7.7.3 Auto-Mute (AMUTE)

Default = 1

0 - Disabled

1 - Enabled

Function:

The Digital-to-Analog converters of the CS42438 will mute the output following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits (SZC[1:0]).

### 7.7.4 Mute ADC Serial Port (MUTE\_ADC\_SP)

Default = 0

0 - Disabled

1 - Enabled

Function:

When enabled, the ADC Serial Port will be muted.

## 7.8 DAC Channel Mute (Address 07h)

7	6	5	4	3	2	1	0
AOUT8_MUTE	AOUT7_MUTE	AOUT6_MUTE	AOUT5_MUTE	AOUT4_MUTE	AOUT3_MUTE	AOUT2_MUTE	AOUT1_MUTE

### 7.8.1 Independent Channel Mute (AOUTX\_MUTE)

Default = 0

0 - Disabled

1 - Enabled

Function:

The respective Digital-to-Analog converter outputs of the CS42438 will mute when enabled. The quiescent voltage on the outputs will be retained. The muting function is affected by the DAC Soft and Zero Cross bits (DAC\_SZC[1:0]).

## 7.9 AOUTX Volume Control (Addresses 08h- 0Fh)

7	6	5	4	3	2	1	0
AOUTx_VOL7	AOUTx_VOL6	AOUTx_VOL5	AOUTx_VOL4	AOUTx_VOL3	AOUTx_VOL2	AOUTx_VOL1	AOUTx_VOL0

### 7.9.1 Volume Control (AOUTX\_VOL[7:0])

Default = 00h

Function:

The AOUTx Volume Control registers allow independent setting of the signal levels in 0.5 dB increments from 0 dB to -127.5 dB. Volume settings are decoded as shown in [Table 8](#). The volume changes are im-

plemented as dictated by the Soft and Zero Cross bits (DAC\_SZC[1:0]). All volume settings less than -127.5 dB are equivalent to enabling the AOUTx\_MUTE bit for the given channel.

Binary Code	Volume Setting
00000000	0 dB
00101000	-20 dB
01010000	-40 dB
01111000	-60 dB
10110100	-90 dB

**Table 8. Example AOUT Volume Settings**

## 7.10 DAC Channel Invert (Address 10h)

7	6	5	4	3	2	1	0
INV_AOUT8	INV_AOUT7	INV_AOUT6	INV_AOUT5	INV_AOUT4	INV_AOUT3	INV_AOUT2	INV_AOUT1

### 7.10.1 Invert Signal Polarity (INV\_AOUTX)

Default = 0

- 0 - Disabled
- 1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

## 7.11 AINX Volume Control (Address 11h-16h)

7	6	5	4	3	2	1	0
AINx_VOL7	AINx_VOL6	AINx_VOL5	AINx_VOL4	AINx_VOL3	AINx_VOL2	AINx_VOL1	AINx_VOL0

### 7.11.1 AINX Volume Control (AINX\_VOL[7:0])

Default = 00h

Function:

The level of AIN1 - AIN6 can be adjusted in 0.5 dB increments as dictated by the ADC Soft and Zero Cross bits (ADC\_SZC[1:0]) from +24 to -64 dB. Levels are decoded in two's complement, as shown in [Table 9](#).

Binary Code	Volume Setting
0111 1111	+24 dB
...	...
0011 0000	+24 dB
...	...
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1 dB
...	...
1000 0000	-64 dB

**Table 9. Example AIN Volume Settings**



## 7.12 ADC Channel Invert (Address 17h)

7	6	5	4	3	2	1	0
Reserved	Reserved	INV_AIN6	INV_AIN5	INV_AIN4	INV_AIN3	INV_AIN2	INV_AIN1

### 7.12.1 Invert Signal Polarity (INV\_AINX)

Default = 0

0 - Disabled  
1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

## 7.13 Status (Address 19h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	CLK Error	ADC3_OVFL	ADC2_OVFL	ADC1_OVFL

For all bits in this register, a “1” means the associated error condition has occurred at least once since the register was last read. A “0” means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0. Status bits that are masked off in the associated mask register will always be “0” in this register.

### 7.13.1 CLOCK ERROR (CLK ERROR)

Default = x

Function:

Indicates an invalid MCLK to FS ratio. This status flag is set to “Level Active Mode” and becomes active *during* the error condition. See [“System Clocking” on page 33](#) for valid clock ratios.

### 7.13.2 ADC Overflow (ADCX\_OVFL)

Default = x

Function:

Indicates that there is an over-range condition anywhere in the CS42438 ADC signal path of each of the associated ADC’s.

## 7.14 Status Mask (Address 1Ah)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	CLK Error_M	ADC3_OV FL_M	ADC2_OVFL_M	ADC1_OVFL_M

Default = 0000

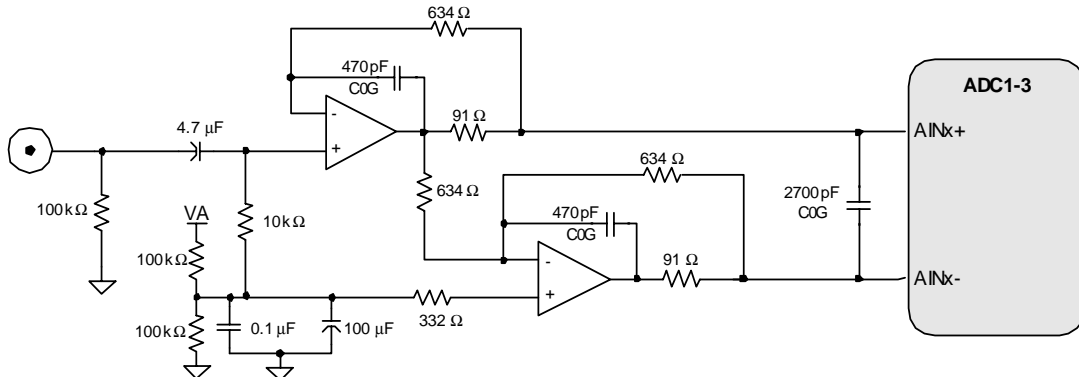
Function:

The bits of this register serve as a mask for the error sources found in the register [“Status \(Address 19h\) \(Read Only\)” on page 49](#). If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect status register. The bit positions align with the corresponding bits in the Status register.

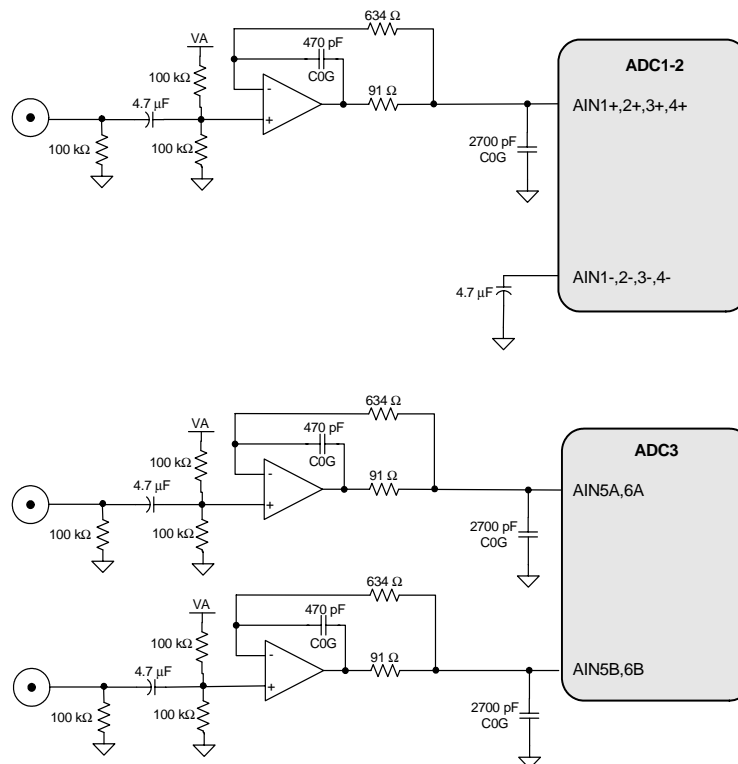
## 8. EXTERNAL FILTERS

### 8.1 ADC Input Filter

The analog modulator samples the input at 6.144 MHz (internal MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the digital passband frequency ( $n \times 6.144$  MHz), where  $n=0,1,2,\dots$ . Refer to [Figures 20](#) and [21](#) for a recommended analog input filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. Refer to [Figures 22](#) and [23](#) for low-cost, low-component-count passive input filters. The use of capacitors that have a large voltage coefficient (such as general-purpose ceramics) must be avoided since these can degrade signal linearity



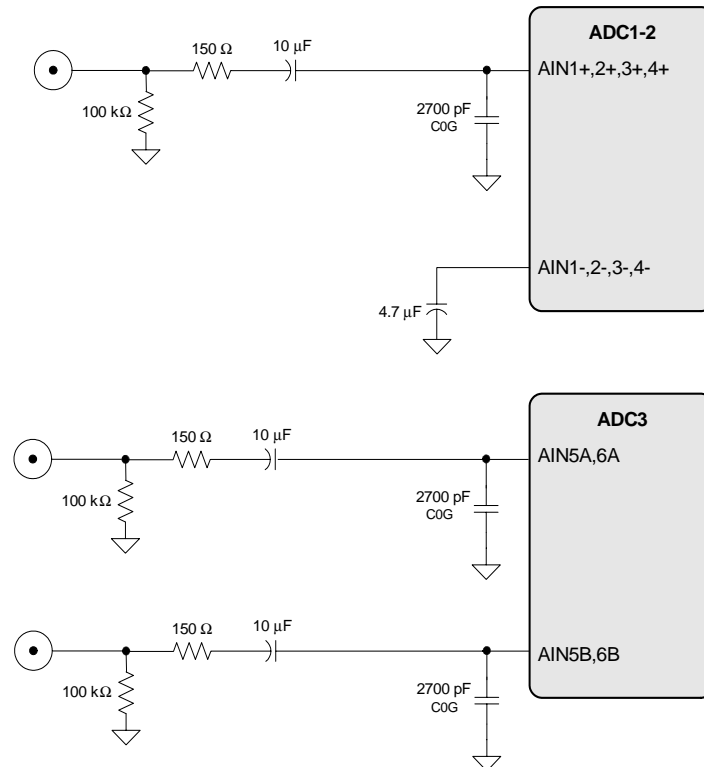
**Figure 20. Single to Differential Active Input Filter**



**Figure 21. Single-Ended Active Input Filter**

### 8.1.1 Passive Input Filter

The passive filter implementation shown in Figure 22 will attenuate any noise energy at 6.144 MHz but will not provide optimum source impedance for the ADC modulators. Full analog performance will therefore not be realized using a passive filter. Figure 22 illustrates the unity gain, passive input filter solution. In this topology the distortion performance is affected, but the dynamic range performance is not limited.

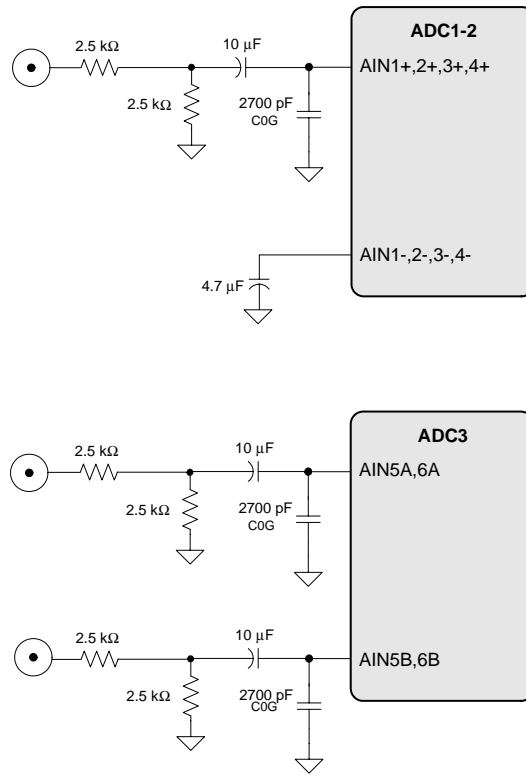


**Figure 22. Passive Input Filter**

### 8.1.2 Passive Input Filter w/Attenuation

Some applications may require signal attenuation prior to the ADC. The full-scale input voltage will scale with the analog power supply voltage. For  $V_A = 5.0\text{ V}$ , the full-scale input voltage is approximately 2.8 V<sub>pp</sub>, or 1 V<sub>rms</sub> (most consumer audio line-level outputs range from 1.5 to 2 V<sub>rms</sub>).

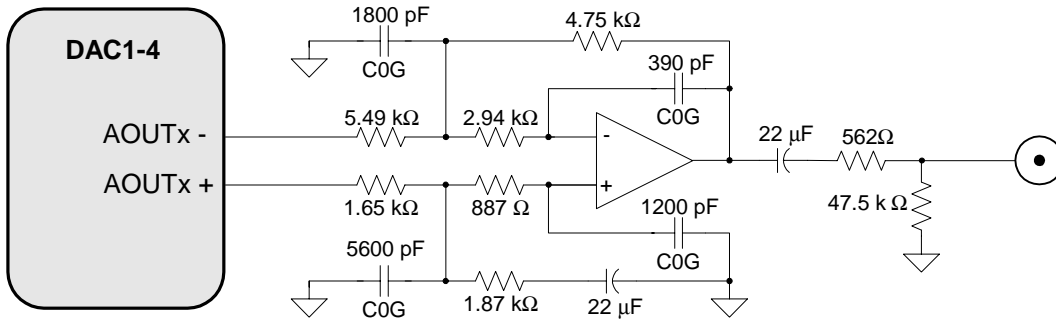
Figure 23 shows a passive input filter with 6 dB of signal attenuation. Due to the relatively high input impedance on the analog inputs, the full distortion performance cannot be realized. Also, the resistor divider circuit will determine the input impedance into the input filter. In the circuit shown in Figure 23, the input impedance is approximately 5 kΩ. By doubling the resistor values, the input impedance will increase to 10 kΩ. However, in this case the distortion performance will drop due to the increase in series resistance on the analog inputs.



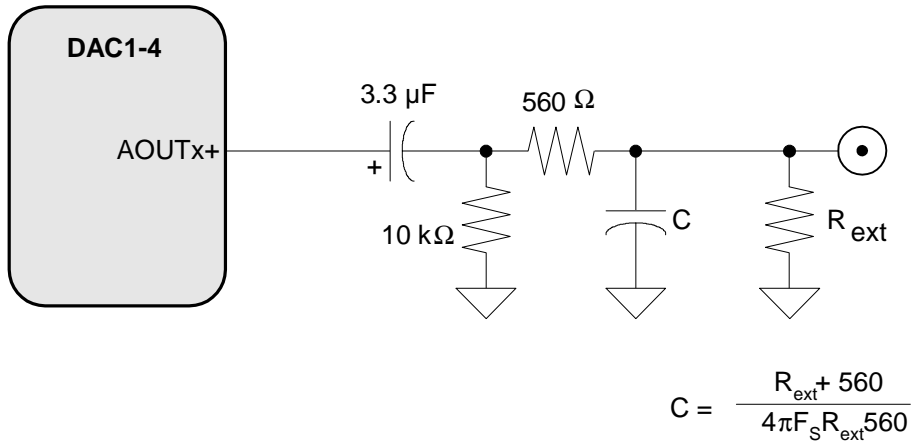
**Figure 23. Passive Input Filter w/Attenuation**

## 8.2 DAC Output Filter

The CS42438 is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry. Shown below is the recommended active and passive output filters.

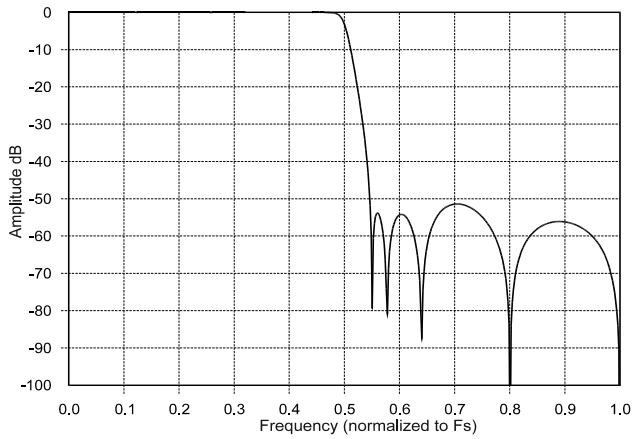


**Figure 24. Active Analog Output Filter**

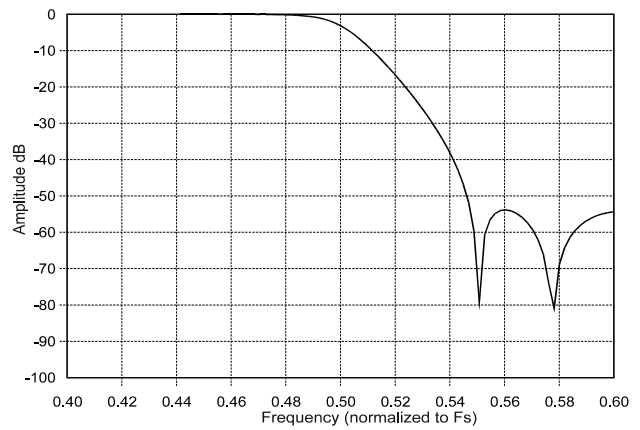


**Figure 25. Passive Analog Output Filter**

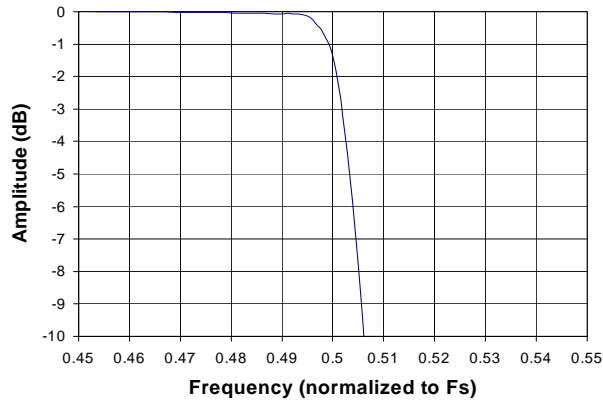
## 9. ADC FILTER PLOTS



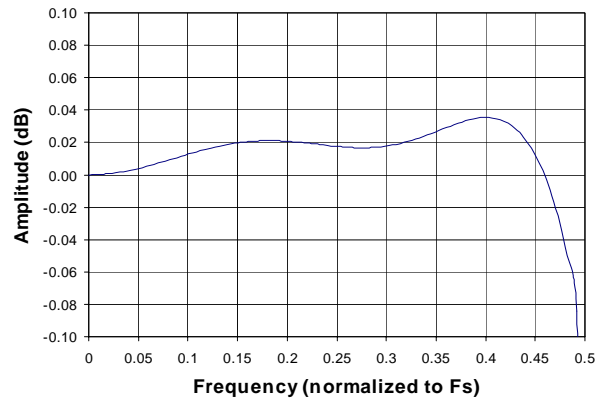
**Figure 26. SSM Stopband Rejection**



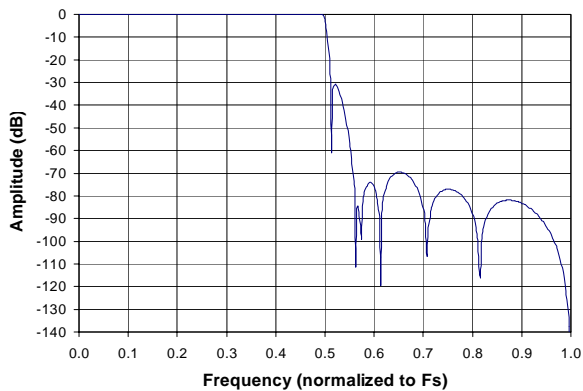
**Figure 27. SSM Transition Band**



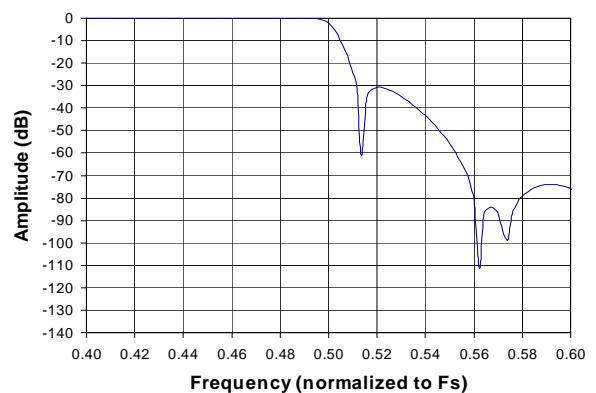
**Figure 28. SSM Transition Band (Detail)**



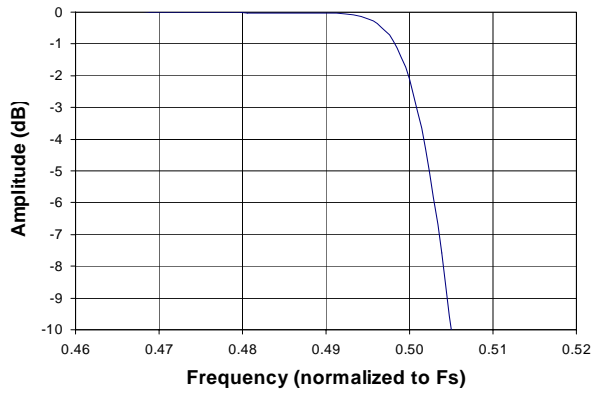
**Figure 29. SSM Passband Ripple**



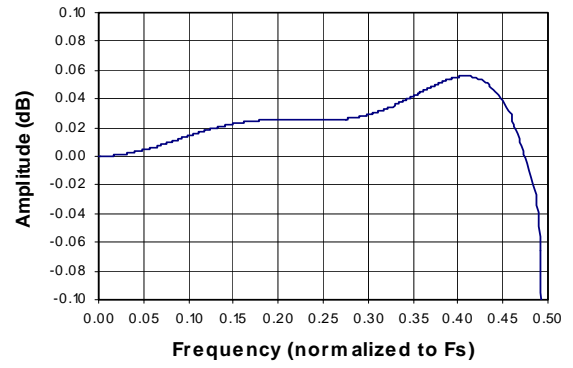
**Figure 30. DSM Stopband Rejection**



**Figure 31. DSM Transition Band**

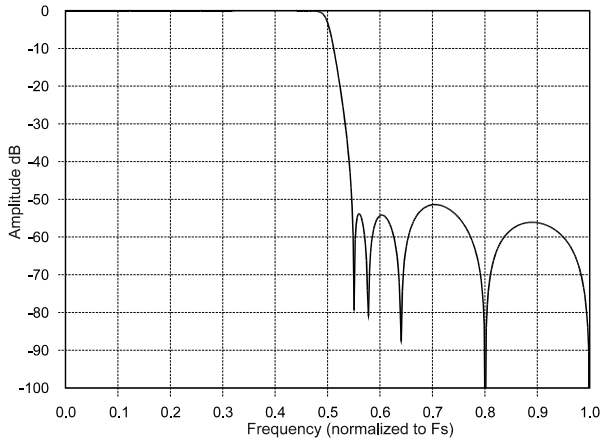


**Figure 32. DSM Transition Band (Detail)**

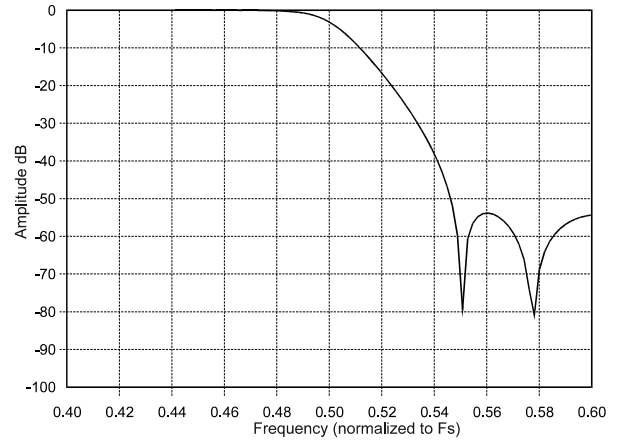


**Figure 33. DSM Passband Ripple**

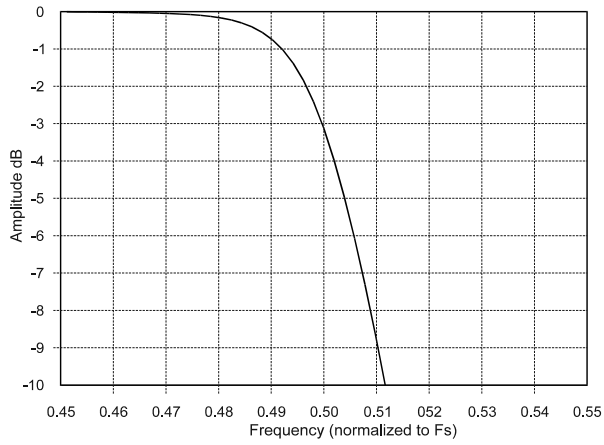
## 10.DAC FILTER PLOTS



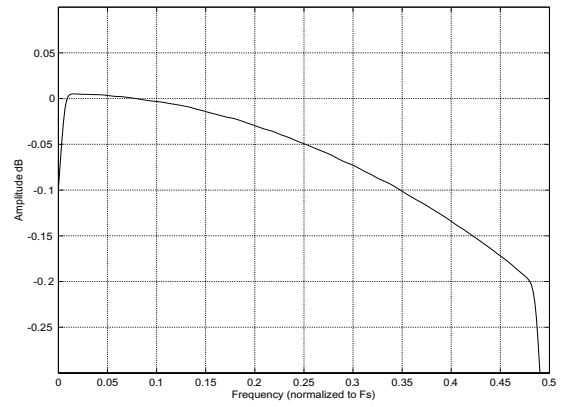
**Figure 34. SSM Stopband Rejection**



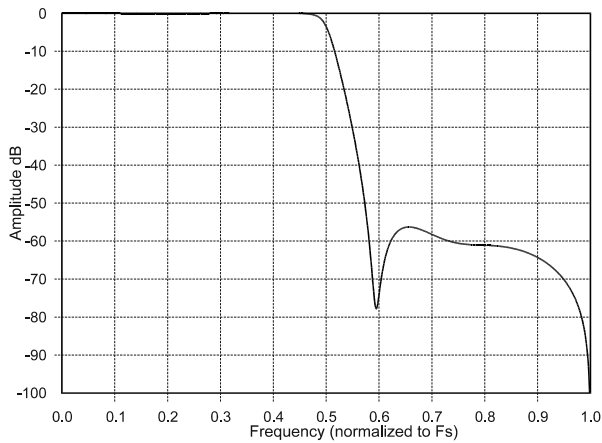
**Figure 35. SSM Transition Band**



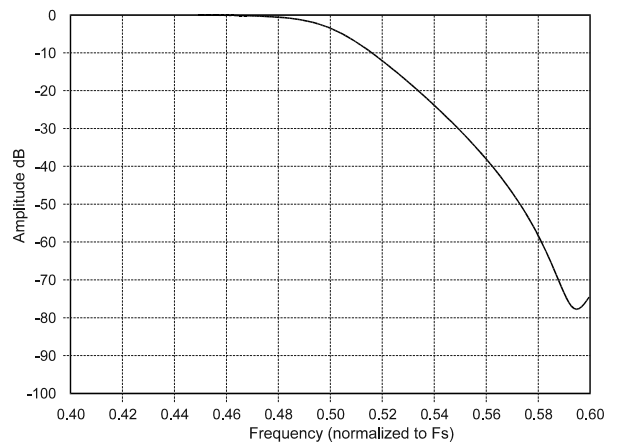
**Figure 36. SSM Transition Band (detail)**



**Figure 37. SSM Passband Ripple**

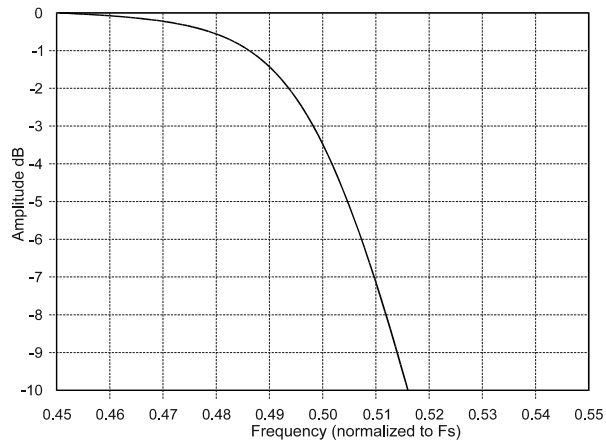
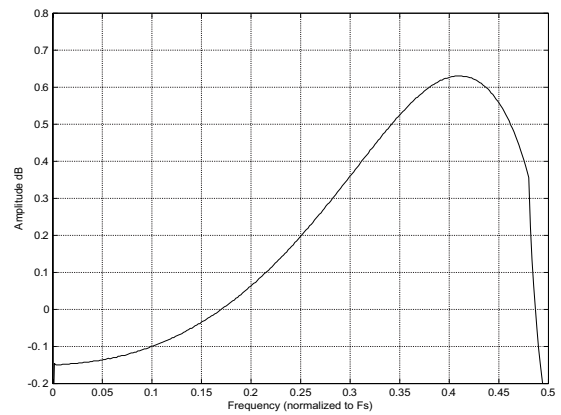
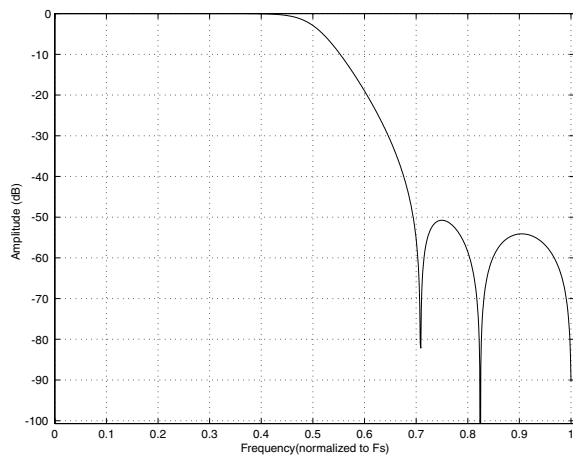
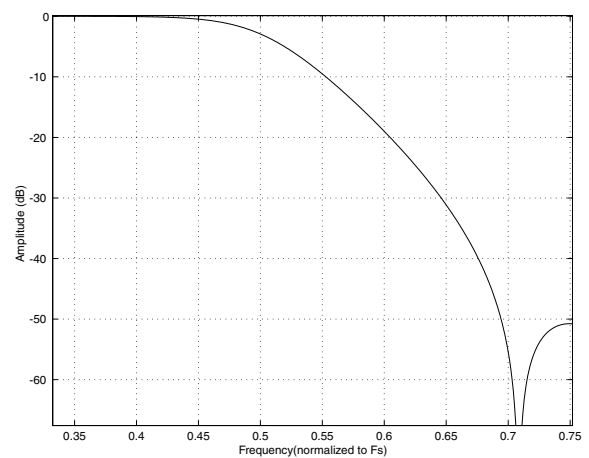
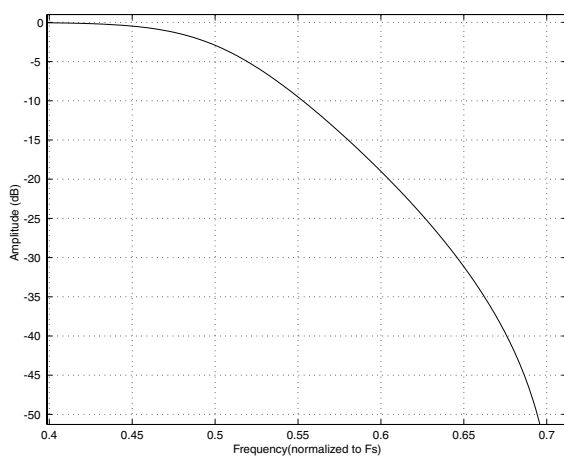
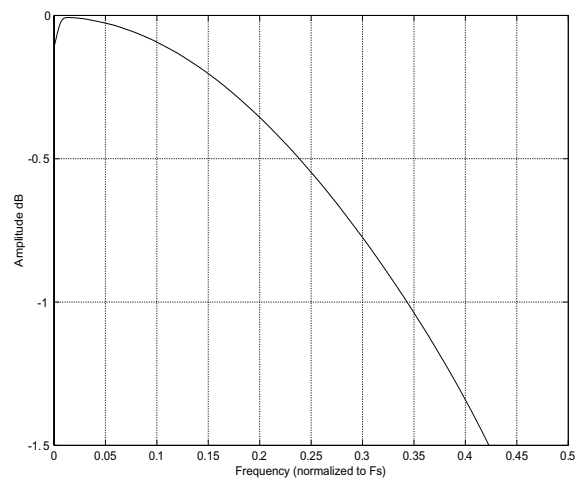


**Figure 38. DSM Stopband Rejection**



**Figure 39. DSM Transition Band**




**Figure 40. DSM Transition Band (detail)**

**Figure 41. DSM Passband Ripple**

**Figure 42. QSM Stopband Rejection**

**Figure 43. QSM Transition Band**

**Figure 44. QSM Transition Band (detail)**

**Figure 45. QSM Passband Ripple**

## 11. PARAMETER DEFINITIONS

### Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

### Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

### Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

### Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

### Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

### Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

### Gain Drift

The change in gain value with temperature. Units in ppm/°C.

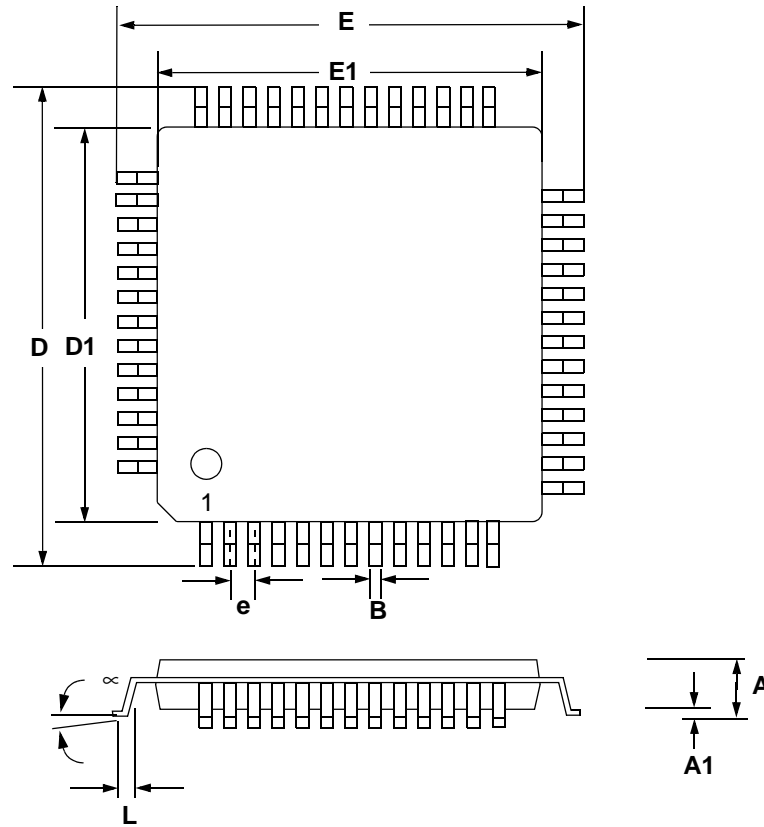
### Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

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## 12. REFERENCES

1. Cirrus Logic, *AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices*, Version 6.0, February 1998.
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7. Cirrus Logic, *A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range*, by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
8. Philips Semiconductor, *The I<sup>2</sup>C-Bus Specification: Version 2.1*, January 2000.  
<http://www.semiconductors.philips.com>

**13.PACKAGE INFORMATION**
**52L MQFP PACKAGE DRAWING**


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.096	---	---	2.45
A1	0.000	---	0.010	0.00	---	0.25
B	0.009	---	0.016	0.22	---	0.40
D	---	0.519	---	---	13.20 BSC	---
D1	---	0.394	---	---	10.00 BSC	---
E	---	0.519	---	---	13.20 BSC	---
E1	---	0.394	---	---	10.00 BSC	---
e*	---	0.026	---	---	0.65 BSC	---
L	0.029	0.035	0.041	0.73	0.88	1.03
$\infty$	0.00°	4°	7.00°	0.00°	4°	7.00°

\* Nominal pin pitch is 0.65 mm  
 Controlling dimension is mm.  
 JEDEC Designation: MS022

**13.1 Thermal Characteristics**

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	$\theta_{JA}$	-	47	-	°C/Watt
	4 Layer Board	$\theta_{JA}$	-	38	-	°C/Watt

## 14.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42438	6-in, 8-out, TDM CODEC for Surround Sound Apps	52L-MQFP	YES	Commercial	-10° to +70° C	Rail	CS42438-CMZ
						Tape & Reel	CS42438-CMZR
				Automotive	-40° to +105° C	Rail	CS42438-DMZ
						Tape & Reel	CS42438-DMZR
CDB42438	CS42438 Evaluation Board	-	-	-	-	-	CDB42438

## 15.REVISION HISTORY

Revision	Changes
A1	Initial Release
A2	Corrected I <sup>2</sup> C Address in Section 5.7.2 on page 36. Corrected Chip I.D. in Section 7.2.1 on page 41.
PP1	Initial Preliminary Product (PP) Release subject to <a href="#">legal notice</a> below. Added pin numbers to “ <a href="#">Typical Connection Diagram (Software Mode)</a> ” on page 11 and “ <a href="#">Typical Connection Diagram (Hardware Mode)</a> ” on page 12. Changed ADC Double-Speed Mode parameters. See <a href="#">Note 2 on page 13</a> and <a href="#">Note 18 on page 21</a> . Added <a href="#">ADC3 MUX Interchannel Isolation</a> characteristic in “Characteristics and Specifications” beginning on page 13. Changed <a href="#">ADC Passband Ripple</a> maximum specifications for SSM, DSM & QSM in section “Characteristics and Specifications” beginning on page 13. Changed <a href="#">DAC Frequency Response</a> specifications for SSM, DSM & QSM in “Characteristics and Specifications” beginning on page 13. Removed ADC Quad-Speed Mode feature. See <a href="#">Note 19 on page 21</a> . Added section “ <a href="#">De-Emphasis Filter</a> ” on page 32. Corrected section “ <a href="#">TDM data is received most significant bit (MSB) first, on the second rising edge of the SCLK occurring after a an FS rising edge. All data is valid on the rising edge of SCLK. The AIN1 MSB is transmitted early, but is guaranteed valid for a specified time after SCLK rises. All other bits are transmitted on the falling edge of SCLK. Each time slot is 32 bits wide, with the valid data sample left justified within the time slot. Valid data lengths are 16, 18, 20, or 24.</a> ” on page 33. Changed AIN1-6 Volume Control range from (+12 dB to -115.5 dB) to (+24 dB to -64 dB) in register “ <a href="#">AINX Volume Control (AINX_VOL[7:0])</a> ” on page 48. Removed the register “ <a href="#">Status Control (address 18h)</a> ”. See “ <a href="#">CLOCK ERROR (CLK ERROR)</a> ” on page 49 and “ <a href="#">ADC Overflow (ADCX_OVFL)</a> ” on page 49 for the Active Mode setting.
PP2	Corrected <a href="#">Figures 21-23</a> . Added “ <a href="#">Ordering Information</a> ” on page 61.
F1	Updated temperature and voltage specifications in the “ <a href="#">Recommended Operating Conditions</a> ” on page 13. Added test conditions to the Analog Input and Analog Output Characteristics tables.

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## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest to you, go to [www.cirrus.com](http://www.cirrus.com).

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