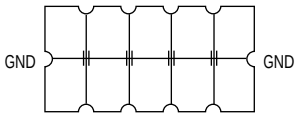
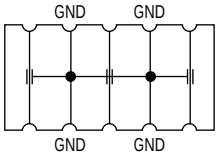
Chip 3-Terminal Capacitor Array

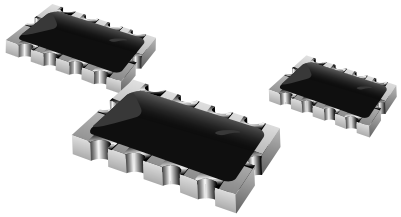
EZANC Terminal pitch 1.27mm
EZASC Terminal pitch 0.8mm



Chip Feed Through Capacitor Array

EZANF Terminal pitch 1.27mm





■ Features

Suitable for EMI suppression filtering

- The low residual inductance at high frequency range provides effective reduction of noise
- Equivalent noise reduction to the EMI filters with low cost design
- Chip Feed Through Capacitor Array with grounding terminal between capacitor elements reduces crosstalk between signal lines and is suitable for high frequency noise protection

Compact design for high density PWB assembly

- EZANC: 6.4 x 3.1 x 0.75mm
  EZASC: 4.0 x 2.1 x 0.65mm
  EZANF: 6.4 x 3.1 x 0.65
- Flat and square packages suitable for high speed automatic placement machine

Superior mountability with concave terminals

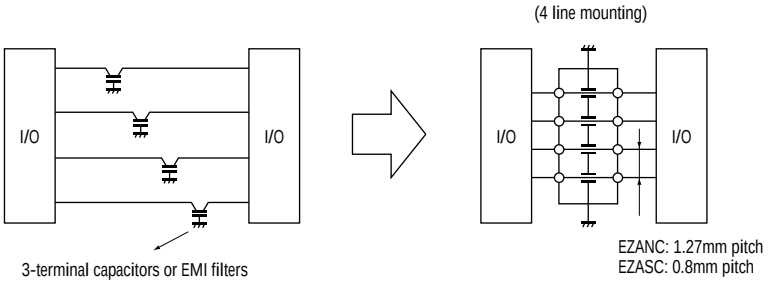
- Firm solder joint (two times of convex terminal)
- Self-alignment of placement at reflow process

ISO-9001 approved

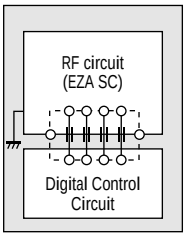
■ Recommended Applications

- Digital equipment such as personal computers, PCMIA cards, PDA and word processors
- Communications equipment, digital cordless phones, cellular phones, GSM, PHS, DECT
- Digital audio and video equipment
- Electrical musical instruments and digital devices

Effect of high density placing, PWB space saving



Digital cordless phone



Prevent high frequency harmonic noise to RF circuits

■ Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11
E	Z	A	N	C	E	1	0	1	M	
Product Code			Dimensions and Circuit Configuration		Temperature Characteristics	Size			Capacitance Tolerance	Suffix for Special Requirements

Product Code
Thick Film Noise Suppression and FIltering Components

Dimensions and Circuit Configuration

NC	6.4 x 3.1mm	Four 3-Terminal Capacitors
SC	4.0 x 2.1mm	
NF	6.4 x 3.1mm	Three Feed Through Capacitors

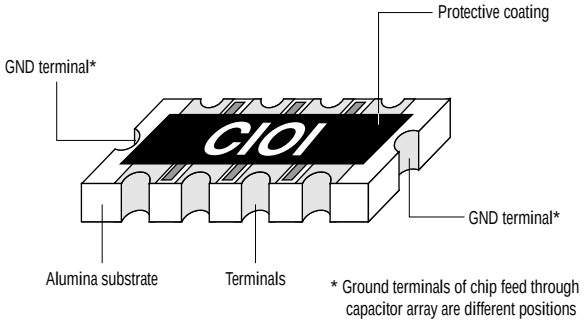
Temperature Characteristics
E +20/–55% (–25 to +85 °C)

Size
The first two digits are significant figures of capacitance value, and the third one denotes the number of zeros following.
Ex. 101 → 100 pF

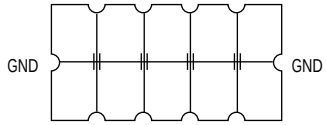
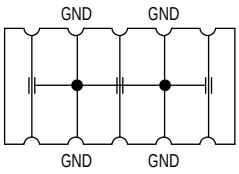
Capacitance Tolerance
M ±20%
+30/–20 in the case of 22 pF

Suffix for Special Requirements

■ Construction

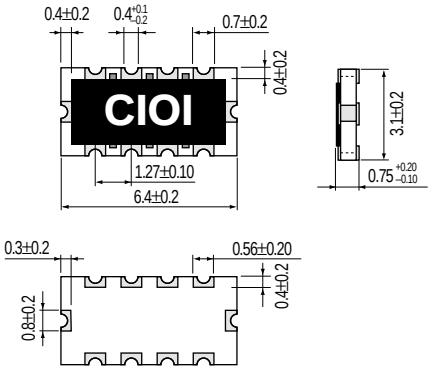


■ Circuit Configuration

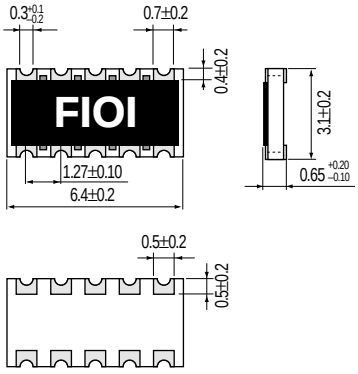
Circuit Code	Circuit Configuration
NC **SC** (EZANC, EZASC)	
NF (EZANF)	

■ Dimensions in mm (not to scale)

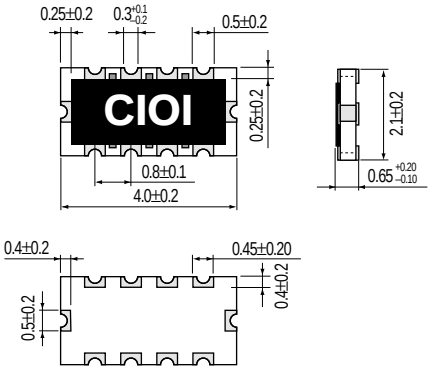
EZANC



EZANF



EZASC

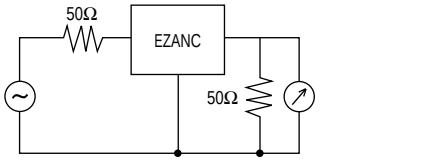


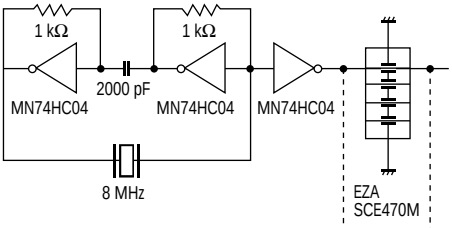
■ Ratings

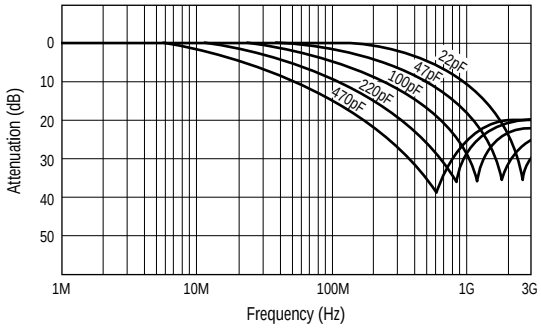
Capacitance values*	**EZANC**	22, 47, 100, 220, 470 pF	Rated voltage	25V	
	EZASC	22, 47, 100 pF	Rated current**	**EZANC**	300 mA
	EZANF	22, 47, 100, 220, 470, 1000 pF		**EZASC**	200 mA
Capacitance tolerance	±20% ($^{+30}_{-20}$% in the case of 22 pF)			**EZANF**	300 mA
Temperature characteristic	E characteristic: +20%/–55% (–25°C to +85°C)		Resistance***	Less than 1.0Ω	
Dissipation factor	Less than 2.0% (25°C, 1 kHz*, 1 Vrms)		Operating temperature range	–25° to +85°C	

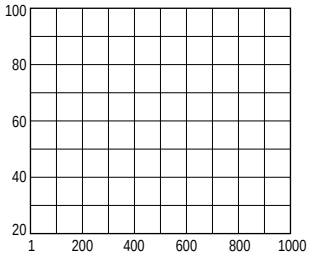
* In measuring at 1 MHz, capacitance value and dissipation factor are different.
** Rated current between input terminal and output terminal.
*** Resistance value between input terminal and output terminal.

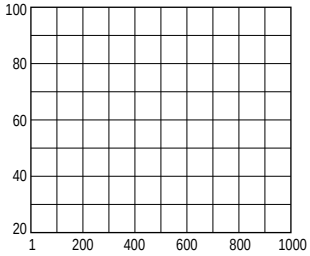
■ Attenuation Characteristics







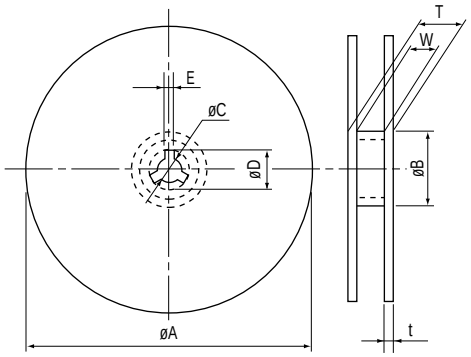




■ Standard Packaging

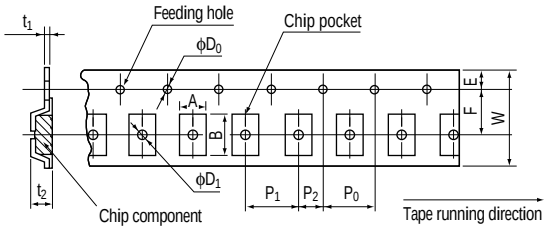
Type	Thickness	Weight/pcs.	Standard Quantity	Style
EZANC	0.75 $^{+0.20}_{-0.10}$ mm	52 mg.	4,000 pcs./reel	Embossed taping
EZASC	0.65 $^{+0.20}_{-0.10}$ mm	17 mg.		
EZANF	0.65 $^{+0.20}_{-0.10}$ mm	40 mg.		

Standard Reel Dimensions in mm (not to scale)



Dimensions							
øA	**øB**	**øC**	**øD**	**E**	**W**	**T**	**t**
$178^{\pm2}$	$60.0^{\pm0.5}$	$13.0^{\pm0.5}$	$21.0^{\pm0.8}$	$2.0^{\pm0.5}$	$13.0^{\pm0.3}$	$15.4^{\pm1.0}$	$1.2^{\pm0.2}$

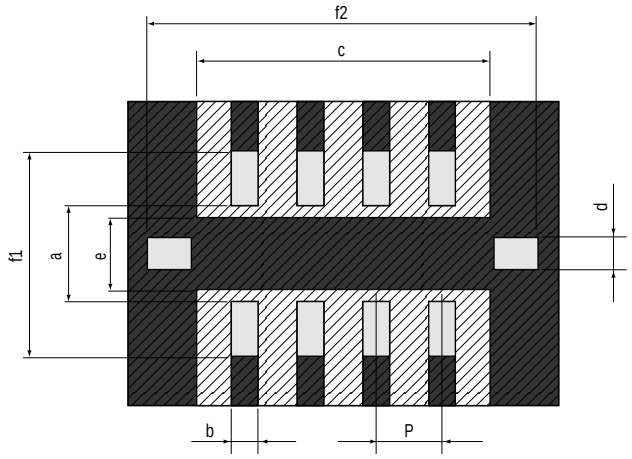
Embossed Carrier Dimensions in mm (not to scale)



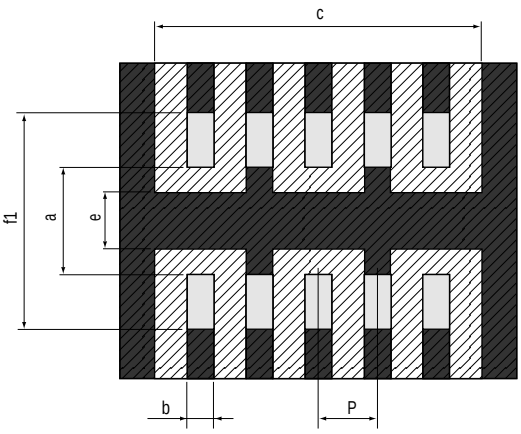
	Dimensions					
	A	**B**	**W**	**F**	**E**	**P_0**
EZASC	$2.50^{\pm0.20}$	$4.40^{\pm0.20}$	$12.00^{\pm0.20}$	$5.50^{\pm0.10}$	$1.75^{\pm0.10}$	$4.00^{\pm0.10}$
EZANC/NF	$3.40^{\pm0.20}$	$6.70^{\pm0.20}$				
	P_1	**P_2**	**$øD_0$**	**t_1**	**t_2**	**$øD_1$**
EZASC	$4.00^{\pm0.10}$	$2.00^{\pm0.10}$	$1.50^{+0.1}_{0}$	$0.25^{\pm0.05}$	$1.15^{\pm0.20}$	$1.50^{-0.10}_{0}$
EZANC/NF					$1.30^{\pm0.20}$	

■ Recommended Land Pattern Design

EZANC/EZASC
Chip 3-Terminal Capacitor Array



EZANF
Chip Feed-Through Capacitor Array



Solder resist Land pattern

	Dimensions (mm)							
	a	**b**	**c**	**d**	**e**	**f1**	**f2**	**P**
EXANC	2.1 to 2.5	0.4 to 0.6	5.6 to 5.8	0.4 to 0.8	1.8	4.3 to 4.7	7.6 to 8.0	1.27
EZASC	1.6 to 1.7	0.4	3.4 to 3.6	0.4 to 0.5	1.2	2.7 to 3.5	4.8 to 5.4	0.8
EZANF	2.1 to 2.5	0.4 to 0.6	5.6 to 5.8	—	1.8	4.3 to 4.7	—	1.27

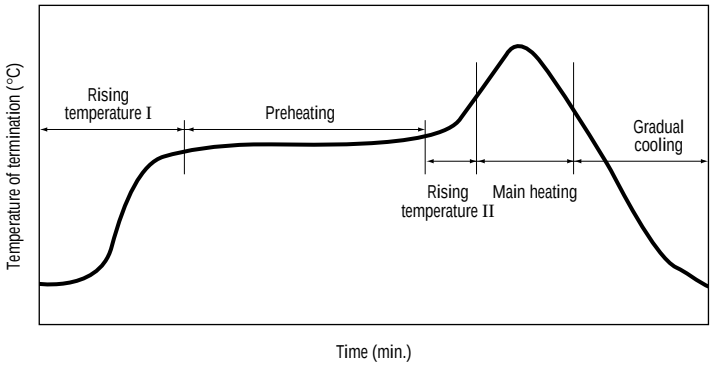
■ Safety Precautions

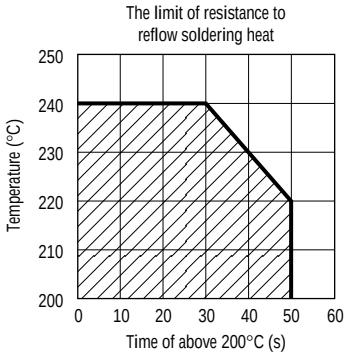
1. Soldering

- Reflow soldering. Please consult us when you use different conditions. Please measure the temperature of terminations and study the solderability of every type of board before actual use.

  (Reflow soldering shall be within two times.)

Rising temperature I	The normal to preheating temp.	30 to 60 s
Preheating	140° to 160°C	60 to 120 s
Rising temperature II	Preheating to 200°C	20 to 40 s
Main heating	*(cf. The limits of resistance to reflow soldering heat)*	
Gradual cooling	200 to 100°C	1 to 4 °C/s





- Flow soldering. We cannot recommend the flow soldering to Chip 3-Terminal Capacitor Array: EZASC, because we are afraid that solder bridge happens owing to narrow 0.8mm pitch of EZASC. Ask the flow soldering of EZANC/EZANF type to us.
- Iron soldering. Solder at 280°C max. and 3 seconds max. with the soldering iron tip. The soldering iron tip should not touch the protective coating of the part.
- Use rosin type flux. Do not use high-activity flux (the chlorine content is 0.2 wt% or more).
- Allow enough preheating so that the difference of soldering temperature and the temperature of the surface of the part is 100°C or less. This temperature difference should be kept in rapid cooling by immersion into solvent.
- More amount of solder gives more mechanical stress to the part, resulting in crack of impaired characteristics. Avoid excessive amount of solder.

2. Cleaning

- Residual flux after board washing may cause solder migration. Carefully check the status of board washing. Study type of water-soluble flux, cleaning agent, and drying condition when water washing is done. Confirm they will not cause any trouble.

3. Miscellaneous

- Take necessary precaution to avoid any abnormal stress caused by bend of board.
- Do not use the product in dewy atmospheres.
- Peculiar characteristic of dielectric materials of high dielectric constant may reduce static capacitance by a few percents relative to that at shipment.