# MAX9860

# 16-Bit Mono Audio Voice Codec

## General Description

The MAX9860 is a low-power, voiceband, mono audio codec designed to provide a complete audio solution for wireless voice headsets and other mono voice audio devices. Using an on-chip bridge-tied load mono headphone amplifier, the MAX9860 can output 30mW into a 32Ω earpiece while operating from a single 1.8V power supply. Very low power consumption makes it an ideal choice for battery-powered applications.

The MAX9860's flexible clocking circuitry utilizes common system clock frequencies ranging from 10MHz to 60MHz, eliminating the need for an external PLL and multiple crystal oscillators. Both the ADC and DAC support sample rates of 8kHz to 48kHz in either synchronous or asynchronous operation. Both master and slave timing modes are supported.

Two differential microphone inputs are available with a user-programmable preamplifier and programmable gain amplifier. Automatic gain control with selectable attack/release times and signal threshold allows maximum dynamic range. A noise gate with selectable threshold provides a means to quiet the channel when no signal is present. Both the DAC and ADC digital filters provide full attenuation for out-of-band signals as well as a 5th order GSM-compliant digital highpass filter. A digital side tone mixer provides loopback of the microphones/ADC signal to the DAC/headphone output.

Serial DAC and ADC data is transferred over a flexible digital I²S-compatible interface that also supports TDM mode. Mode settings, volume control, and shutdown are programmed through a 2-wire, I²C-compatible interface.

The MAX9860 is fully specified over the -40°C to +85°C extended temperature range and is available in a low-profile, 4mm x 4mm, 24-pin thin QFN package.

## Applications

Audio Headsets

Portable Navigation Device

Mobile Phones

Smart Phones

VoIP Phones

Audio Accessories

***Pin Configuration and Typical Operating Circuit appear at end of data sheet.***

## Features

- **1.8V Single-Supply Operation**
- **Digital Highpass Elliptical Filters with Notch for 217Hz (GSM)**
- **Mono 30mW BTL Headphone Amplifier**
- **Dual Low-Noise Microphone Inputs**
- **Automatic Microphone Gain Control and Noise Gate**
- **90dB DAC DR ($f_S$ = 48kHz)**
- **81dB ADC DR ($f_S$ = 48kHz)**
- **Supports Master Clock Frequencies from 10MHz to 60MHz**
- **Supports Sample Rates from 8kHz to 48kHz**
- **Flexible Digital Audio Interface**
- **Clickless/Popless Operation**
- **2-Wire, I²C-Compatible Control Interface**
- **Available in 24-Pin, Thin QFN, 4mm x 4mm x 0.8mm Package**

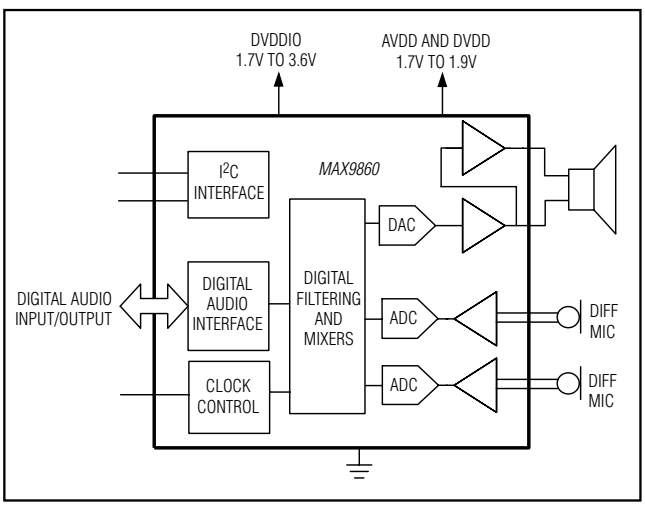
## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX9860ETG+ | -40°C to +85°C | 24 TQFN-EP* |

*+Denotes a lead-free/RoHS-compliant package.*

**EP = Exposed pad.*

## Simplified Block Diagram




***For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.***

*19-4349; Rev 2; 2/12*

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to AGND.)
DVDDIO, SDA, SCL, $\overline{IRQ}$.....-0.3V to +3.6V
AVDD, DVDD.....-0.3V to +2V
AGND, DGND, MICGND.....-0.3V to +0.3V
OUTP, OUTN, PREG, REF, MICBIAS.....-0.3V to ($V_{AVDD}$ + 0.3V)
MICLP, MICLN, MICRP, MICRN, REG....-0.3V to ($V_{PREG}$ + 0.3V)
MCLK, LRCLK, BCLK,
SDOUT, SDIN.....-0.3V to ($V_{DVDDIO}$ + 0.3V)

Continuous Power Dissipation ($T_A$ = +70°C)
24-Pin TQFN (derate 27.8mW/°C above +70°C, multilayer board).....2222mW
Operating Temperature Range.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$).....36°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$).....3°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## ELECTRICAL CHARACTERISTICS

($V_{AVDD}$ = $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{MICBIAS}$ = $C_{PREG}$ = $C_{REG}$ = 1µF, $A_{VPRE}$ = +20dB, $A_{VMICPGA}$ = 0dB, $f_{MCLK}$ = 13MHz, $f_{LRCLK}$ = 8kHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage Range | | AVDD (inferred from HP output PSRR) | | 1.7 | 1.8 | 1.9 | V |
| | | DVDD (inferred from codec performance tests) | | 1.7 | 1.8 | 1.9 | |
| | | DVDDIO | | 1.7 | 1.8 | 3.6 | |
| Total Supply Current (Note 3) | $I_{AVDD+DVDD}$ | DAC playback mode (48kHz) | AVDD | | 1.46 | 2.2 | mA |
| | | | DVDD | | 1.05 | 1.6 | |
| | | Full operation 8kHz mono ADC + DAC | AVDD | | 4.08 | 5.7 | |
| | | | DVDD | | 0.78 | 1.0 | |
| | | Full operation 8kHz stereo ADC + DAC | AVDD | | 6.17 | 9.0 | |
| | | | DVDD | | 0.8 | 1.2 | |
| | | Stereo ADC only (48kHz) | AVDD | | 5.38 | 8.0 | |
| | | | DVDD | | 1.68 | 2.2 | |
| Shutdown Supply Current | $I_{\overline{SHDN}}$ | $T_A$ = +25°C | AVDD | | 0.56 | 5 | µA |
| | | | DVDD + DVDDIO | | 1.65 | 5 | |
| Shutdown to Full Operation | | | | | 10 | | ms |
| **DAC (Note 4)** | | | | | | | |
| Gain Error | | | | | ±1 | ±5 | % |
| Dynamic Range (Note 5) | DR | +0dB volume setting, $f_S$ = 8kHz, measured at headphone output, $T_A$ = +25°C | | 84 | 90 | | dB |
| DAC Full-Scale Output | | | | | 1 | | $V_{RMS}$ |
| DAC Path Phase Delay | | f = 1kHz, 0dBFS, HP filter disabled, digital input to analog output | $f_S$ = 8kHz | | 1.2 | | ms |
| | | | $f_S$ = 16kHz | | 0.59 | | |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz | | | -87 | | dB |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{MICBIAS}$ = $C_{PREG}$ = $C_{REG}$ = 1µF, $A_{VPRE}$ = +20dB, $A_{VMICPGA}$ = 0dB, $f_{MCLK}$ = 13MHz, $f_{LRCLK}$ = 8kHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Power-Supply Rejection Ratio | PSRR | f = 1kHz, $V_{RIPPLE}$ = 100m$V_{P-P}$, $A_{VPGA}$ = 0dB | | 94 | | dB |
| | | f = 10kHz, $V_{RIPPLE}$ = 100m$V_{P-P}$, $A_{VPGA}$ = 0dB | | 71 | | |
| **DAC LOWPASS DIGITAL FILTER** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | With respect to $f_S$ within ripple; $f_S$ = 8kHz to 48kHz | | 0.448 x $f_S$ | | Hz |
| | | -3dB cutoff | | 0.451 | | $f_S$ |
| Passband Ripple | | $f < f_{PLP}$ | | ±0.1 | | dB |
| Stopband Cutoff | $f_{SLP}$ | With respect to $f_S$; $f_S$ = 8kHz to 48kHz | | 0.476 x $f_S$ | | Hz |
| Stopband Attenuation | | $f > f_{SLP}$, f = 20Hz to 20kHz | | 75 | | dB |
| **DAC HIGHPASS DIGITAL FILTER** | | | | | | |
| 5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable) (Note 6) | $f_{DHPPB}$ | DVFLT = 0x1 (elliptical for 16kHz GSM) | | 0.0161 x $f_S$ | | Hz |
| | | DVFLT = 0x2 (500Hz Butterworth for 16kHz) | | 0.0312 x $f_S$ | | |
| | | DVFLT = 0x3 (elliptical for 8kHz GSM) | | 0.0321 x $f_S$ | | |
| | | DVFLT = 0x4 (500Hz Butterworth for 8kHz) | | 0.0625 x $f_S$ | | |
| | | DVFLT = 0x5 (200Hz Butterworth for 48kHz) | | 0.0042 x $f_S$ | | |
| 5th Order Stopband Cutoff (-30dB from Peak, I²C Register Programmable) (Note 6) | $f_{DHPSB}$ | DVFLT = 0x1 (elliptical for 16kHz GSM) | | 0.0139 x $f_S$ | | Hz |
| | | DVFLT = 0x2 (500Hz Butterworth for 16kHz) | | 0.0156 x $f_S$ | | |
| | | DVFLT = 0x3 (elliptical for 8kHz GSM) | | 0.0279 x $f_S$ | | |
| | | DVFLT = 0x4 (500Hz Butterworth for 8kHz) | | 0.0312 x $f_S$ | | |
| | | DVFLT = 0x5 (200Hz Butterworth for 48kHz) | | 0.0021 x $f_S$ | | |
| DC Blocking | $DC_{Atten}$ | DVFLT ≠ 0x0 | | 90 | | dB |
| **ADC** | | | | | | |
| Full-Scale Input Voltage | 0dBFS | Differential MIC Input, $A_{VPRE}$ = 0dB, $A_{VPGA}$ = 0dB | | 1 | | $V_{P-P}$ |
| Channel Gain Mismatch | | | | ±0.3 | | % |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{MICBIAS}$ = $C_{PREG}$ = $C_{REG}$ = 1µF, $A_{VPRE}$ = +20dB, $A_{VMICPGA}$ = 0dB, $f_{MCLK}$ = 13MHz, $f_{LRCLK}$ = 8kHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Dynamic Range (Note 5) | DR | $f_S$ = 8kHz, $A_{VPRE}$ = 0dB, A-weighted from 20Hz to $f_S$/2 | | | 81 | | dB |
| | | $f_S$ = 48kHz, $A_{VPRE}$ = 0dB, $T_A$ = +25°C | | 75 | 83 | | |
| ADC Phase Delay | | f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output | $f_S$ = 8kHz | | 1.2 | | ms |
| | | | $f_S$ = 16kHz | | 0.61 | | |
| Total Harmonic Distortion | THD | f = 1kHz, $f_S$ = 48kHz, $T_A$ = +25°C | | -70 | -75 | | dB |
| Power-Supply Rejection Ratio | PSRR | f = 1kHz, $V_{RIPPLE}$ = 100m$V_{P-P}$, $A_{VPGA}$ = 0dB | | | 82 | | dB |
| | | f = 10kHz, $V_{RIPPLE}$ = 100m$V_{P-P}$, $A_{VPGA}$ = 0dB | | | 76 | | |
| Channel Crosstalk | | Driven channel at -1dBFS, f = 1kHz | | | -92 | | dB |
| **ADC LOWPASS DIGITAL FILTER** | | | | | | | |
| Passband Cutoff | $f_{PLP}$ | With respect to $f_S$ within ripple; $f_S$ = 8kHz to 48kHz | | | 0.445 x $f_S$ | | Hz |
| | | -3dB cutoff | | | 0.449 | | $f_S$ |
| Passband Ripple | | f < $f_{PLP}$ | | | ±0.1 | | dB |
| Stopband Cutoff | $f_{SLP}$ | With respect to $f_S$; $f_S$ = 8kHz to 48kHz | | | 0.469 x $f_S$ | | Hz |
| Stopband Attenuation | | f > $f_{SLP}$ | | | 74 | | dB |
| **ADC HIGHPASS DIGITAL FILTER** | | | | | | | |
| 5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable) (Note 6) | $f_{AHPPB}$ | AVFLT = 0x1 (elliptical for 16kHz GSM) | | | 0.0161 x $f_S$ | | Hz |
| | | AVFLT = 0x2 (500Hz Butterworth for 16kHz) | | | 0.0312 x $f_S$ | | |
| | | AVFLT = 0x3 (elliptical for 8kHz GSM) | | | 0.0321 x $f_S$ | | |
| | | AVFLT = 0x4 (500Hz Butterworth for 8kHz) | | | 0.0625 x $f_S$ | | |
| | | AVFLT = 0x5 (200Hz Butterworth for 48kHz) | | | 0.0042 x $f_S$ | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{MICBIAS}$ = $C_{PREG}$ = $C_{REG}$ = 1µF, $A_{VPRE}$ = +20dB, $A_{VMICPGA}$ = 0dB, $f_{MCLK}$ = 13MHz, $f_{LRCLK}$ = 8kHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| 5th Order Stopband Cutoff (-30dB from peak, I²C Register Programmable) (Note 6) | $f_{AHPSB}$ | AVFLT = 0x1 (elliptical for 16kHz GSM) | | 0.0139 x $f_S$ | | Hz |
| | | AVFLT = 0x2 (500Hz Butterworth for 16kHz) | | 0.0156 x $f_S$ | | |
| | | AVFLT = 0x3 (elliptical for 8kHz GSM) | | 0.0279 x $f_S$ | | |
| | | AVFLT = 0x4 (500Hz Butterworth for 8kHz) | | 0.0312 x $f_S$ | | |
| | | AVFLT = 0x5 (200Hz Butterworth for 48kHz) | | 0.0021 x $f_S$ | | |
| DC Blocking | $DC_{ATTEN}$ | AVFLT ≠ 0x0 | | 90 | | dB |
| **CLOCKING** | | | | | | |
| MCLK Input Frequency | | MCLK is not required to be synchronous or related to the desired LRCLK data rate | 10 | | 60 | MHz |
| MCLK Duty Cycle | | | 40 | 50 | 60 | % |
| Maximum MCLK Input Jitter | | For guaranteed performance limits | | 100 | | $ps_{RMS}$ |
| LRCLK Data Rate Frequency | | | 8 | | 48 | kHz |
| LRCLK PLL Lock Time | | | | 12 | 25 | ms |
| LRCLK Acceptable Jitter for Maintaining PLL Lock | | | | ±20 | | ns |
| **MONO HEADPHONE AMPLIFIER** | | | | | | |
| Output Power | $P_{OUT}$ | f = 1kHz, THD+N ≤ 1%, $T_A$ = +25°C, $R_L$ = 16Ω | 30 | 50 | | mW |
| | | f = 1kHz, THD+N ≤ 1%, $T_A$ = +25°C, $R_L$ = 32Ω | | 33 | | |
| Total Harmonic Distortion + Noise | THD+N | $R_L$ = 32Ω, $P_{OUT}$ = 25mW, f = 1kHz | | 0.05 | | % |
| | | $R_L$ = 16Ω, $P_{OUT}$ = 25mW, f = 1kHz | | 0.08 | | |
| Dynamic Range (Note 5) | DR | +0dB volume setting, DAC input at $f_S$ = 8kHz to 48kHz | | 90 | | dB |
| Power-Supply Rejection Ratio | PSRR | $V_{AVDD}$ = 1.7V to 1.9V | 60 | 84 | | dB |
| | | $V_{RIPPLE}$ = 100m$V_{P-P}$, f = 217Hz | | 86 | | |
| | | $V_{RIPPLE}$ = 100m$V_{P-P}$, f = 20kHz | | 71 | | |
| Output Offset Voltage | $V_{OS}$ | $V_{OUTP}$ - $V_{OUTN}$, $T_A$ =+25°C | | | ± 3.5 | mV |
| Capacitive Drive Capability | | No sustained oscillations, $R_L$ = 32Ω | | 500 | | pF |
| | | No sustained oscillations, $R_L$ = ∞ | | 100 | | |
| Click-and-Pop Level | | Peak voltage into/out of shutdown, 32sps, A-weighted | | -70 | | dBV |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD}$ = $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{MICBIAS}$ = $C_{PREG}$ = $C_{REG}$ = 1µF, $A_{VPRE}$ = +20dB, $A_{VMICPGA}$ = 0dB, $f_{MCLK}$ = 13MHz, $f_{LRCLK}$ = 8kHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **MICROPHONE AMPLIFIER** | | | | | | | |
| Preamplifier Gain | $A_{VPRE}$ | $T_A$ = +25°C | PAM = 00 | | Off | | dB |
| | | | PAM = 01 | -0.5 | 0 | +0.5 | |
| | | | PAM = 10 | 19 | 20 | 21 | |
| | | | PAM = 11 | 29 | 30 | 31 | |
| MIC PGA Gain | $A_{VMICPGA}$ | PGAM = 0x14–0x1F | | | 0 | | dB |
| | | PGAM = 0x00 | | | +20 | | |
| MIC PGA Gain Step Size | | | | | 1 | | dB |
| Common-Mode Rejection Ratio | CMRR | $V_{IN}$ = 100m$V_{P-P}$ at 217Hz | | | 50 | | dB |
| MIC Input Resistance | $R_{IN\_MIC}$ | All gain settings, measured at MICLN/MICRN | | 30 | 50 | | kΩ |
| MIC Input Bias Voltage | | | | 0.7 | 0.8 | 0.9 | V |
| Total Harmonic Distortion + Noise | THD+N | $A_{VPRE}$ = 0dB, $A_{VMICPGA}$ = 0dB, $V_{IN}$ = 1$V_{P-P}$, f = 1kHz | | | -75 | | dB |
| | | $A_{VPRE}$ = +30dB, $A_{VMICPGA}$ = 0dB, $V_{IN}$ = 31m$V_{P-P}$, f = 1kHz | | | -66 | | dB |
| MIC Power-Supply Rejection Ratio | PSRR | $V_{AVDD}$ = 1.7V to 1.9V | | 60 | 95 | | dB |
| | | $V_{RIPPLE}$ = 100mV at 1kHz, input referred | | | 82 | | dB |
| | | $V_{RIPPLE}$ = 100mV at 10kHz, input referred | | | 76 | | dB |
| **MICROPHONE BIAS** | | | | | | | |
| MICBIAS Output Voltage | $V_{MICBIAS}$ | $I_{LOAD}$ = 1mA, $T_A$ = +25°C | | 1.5 | 1.55 | 1.6 | V |
| Load Regulation | | $I_{LOAD}$ = 1mA to 2mA | | | 0.2 | 10 | mV |
| MICBIAS Line Ripple Rejection | LRR | $V_{RIPPLE}$ = 100m$V_{P-P}$ at 217Hz | | | 82 | | dB |
| | | $V_{RIPPLE}$ = 100m$V_{P-P}$ at 10kHz | | | 81 | | dB |
| MICBIAS Noise Voltage | | A-weighted | | | 9.5 | | $\mu V_{RMS}$ |
| **AUTOMATIC GAIN CONTROL** | | | | | | | |
| AGC Hold Duration | | AGCHLD[1:0] setting range, FREQ ≠ 0 | | 50 | | 400 | ms |
| AGC Attack Time | | AGCATK[1:0] setting range, FREQ ≠ 0 | | 3 | | 200 | ms |
| AGC Release Time | | AGCRLS[2:0] setting range, FREQ ≠ 0 | | 0.078 | | 10 | s |
| AGC Threshold Level | | AGCSTH[3:0] setting range, FREQ ≠ 0 | | -3 | | -18 | dB |
| **NOISE GATE** | | | | | | | |
| NG Attack and Release Time | | | | | 0.5 | | s |
| NG Threshold Level | | | | -72 | | -16 | dB |
| Noise Gate Threshold Step Size | | | | | 4 | | dB |
| NG Attenuation | | | | 0 | | 12 | dB |
| **DIGITAL SIDETONE** | | | | | | | |
| Sidetone Gain Adjust | DVST | 2dB steps | | -60 | | 0 | dB |
| Sidetone Phase Delay | PDLY | MIC input to headphone output, f = 1kHz, HP filter disabled | 8kHz | | 2.2 | | ms |
| | | | 16kHz | | 1.1 | | |

## DIGITAL AUDIO INTERFACE ELECTRICAL CHARACTERISTICS

($V_{DVDD}$ = $V_{DVDDIO}$ = 1.8V, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| BCLK Cycle Time | $t_{BCLKS}$ | Slave operation | 75 | | | ns |
| BCLK High Time | $t_{BCLKH}$ | Slave operation | 30 | | | ns |
| BCLK Low Time | $t_{BCLKL}$ | Slave operation | 30 | | | ns |
| BCLK or LRCLK Rise and Fall Time | $t_R$, $t_F$ | Master operation | | 7 | | ns |
| SDIN or LRCLK to BCLK Rising Setup Time | $t_{SU}$ | ABCI = DBCI = 0 | 25 | | | ns |
| SDIN or LRCLK to BCLK Falling Setup Time | $t_{SU}$ | ABCI = DBCI = 1 | 25 | | | ns |
| SDIN or LRCLK to BCLK Rising Hold Time | $t_{HD}$ | ABCI = DBCI = 0 | 0 | | | ns |
| SDIN or LRCLK to BCLK Falling Hold Time | $t_{HD}$ | ABCI = DBCI = 1 | 0 | | | ns |
| SDOUT Delay Time from BCLK Rising Edge | $t_{DLY}$ | ABCI = DBCI = 0, $C_L$ = 30pF | 0 | | 40 | ns |

## I²C INTERFACE ELECTRICAL CHARACTERISTICS

($V_{DVDD}$ = $V_{DVDDIO}$ = 1.8V, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial-Clock Frequency | $f_{SCL}$ | | 0 | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Hold Time (Repeated) START Condition | $t_{HD,STA}$ | | 0.6 | | | µs |
| SCL Pulse Width Low | $t_{LOW}$ | | 1.3 | | | µs |
| SCL Pulse Width High | $t_{HIGH}$ | | 0.6 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU,STA}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{HD,DAT}$ | | 0 | | 900 | ns |
| Data Setup Time | $t_{SU,DAT}$ | | 100 | | | ns |
| SDA and SCL Receiving Rise Time | $t_R$ | $C_B$ is in pF | 20 + 0.1$C_B$ | | 300 | ns |
| SDA and SCL Receiving Fall Time | $t_F$ | $C_B$ is in pF | 20 + 0.1$C_B$ | | 300 | ns |

## I²C INTERFACE ELECTRICAL CHARACTERISTICS (continued)

($V_{DVDD}$ = $V_{DVDDIO}$ = 1.8V, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SDA Transmitting Fall Time | $t_F$ | $C_B$ is in pF | 20 + 0.1$C_B$ | | 250 | ns |
| Setup Time for STOP Condition | $t_{SU,STO}$ | | 0.6 | | | µs |
| Bus Capacitance | $C_B$ | | | | 400 | pF |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | 0 | | 50 | ns |
| **DIGITAL INPUTS (LRCLK, BCLK, SDIN, MCLK)** | | | | | | |
| Input Voltage High | $V_{IH}$ | | 0.7 x $V_{DVDDIO}$ | | | V |
| Input Voltage Low | $V_{IL}$ | | | | 0.3 x $V_{DVDDIO}$ | V |
| MCLK Input Voltage High | | | 1.4 | | | V |
| MCLK Input Voltage Low | | | | | 0.4 | V |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $T_A$ = +25°C | -1 | | +1 | µA |
| Input Capacitance | | | | 3 | | pF |
| **DIGITAL INPUTS (SCL, SDA)** | | | | | | |
| Input Voltage High | $V_{IH}$ | | 0.7 x $V_{DVDD}$ | | | V |
| Input Voltage Low | $V_{IL}$ | | | | 0.3 x $V_{DVDD}$ | V |
| Input Hysteresis | | | | 200 | | mV |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $T_A$ = +25°C | -1 | | +1 | µA |
| Input Capacitance | | | | 3 | | pF |
| **CMOS DIGITAL OUTPUTS (BCLK, LRCLK, SDOUT)** | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 3mA | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OL}$ = 3mA | $V_{DVDDIO}$ - 0.4 | | | V |
| **OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)** | | | | | | |
| Output High Leakage Current | $I_{OH}$ | $V_{OUT}$ = $V_{DVDDIO}$, $T_A$ = +25°C | -1 | | +1 | µA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 3mA | | | 0.4 | V |

**Note 2:** All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.

**Note 3:** Supply current measurements taken with no applied signal at microphone inputs. A digital zero audio signal used for all digital serial audio inputs. Headphone outputs are loaded as stated in the global conditions.

**Note 4:** DAC performance is measured at headphone outputs.

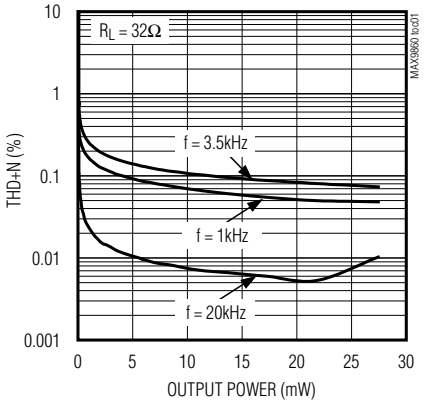
**Note 5:** ADC, DAC, and headphone amplifier dynamic ranges are measured using the EIAJ method. -60dBV 1kHz input signal, A-weighted and normalized to 0dBFS.

**Note 6:** Notch for GSM filters occurs at 217Hz.

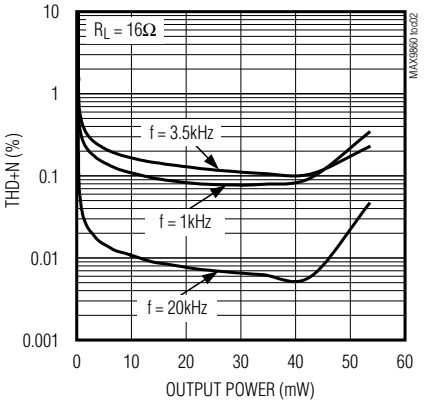
## Typical Operating Characteristics

($V_{AVDD}$ = +1.8V, $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{PREG}$ = $C_{REG}$ = 1µF, $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, $A_{VPRE}$ = +20dB, $f_{MCLK}$ = 13MHz, $T_A$ = +25°C, unless otherwise noted.)

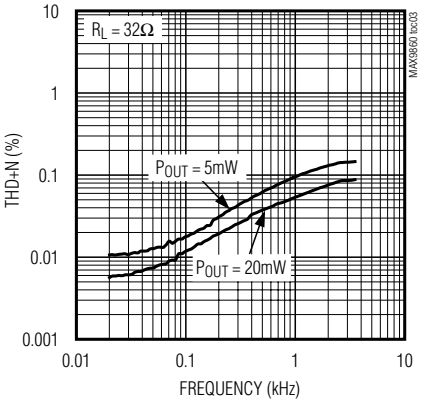
**TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER (DAC TO HP)**



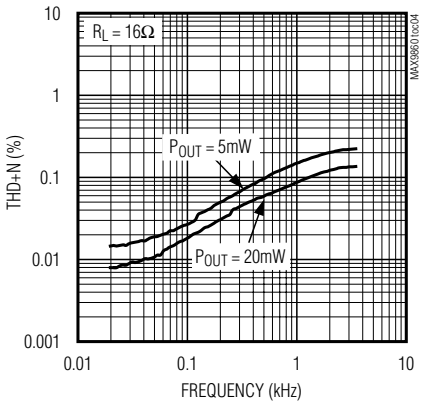

**TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER (DAC TO HP)**



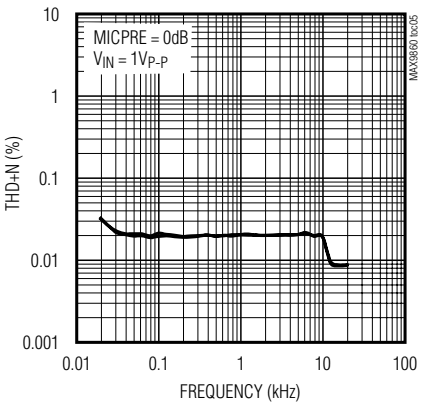

**TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HP)**



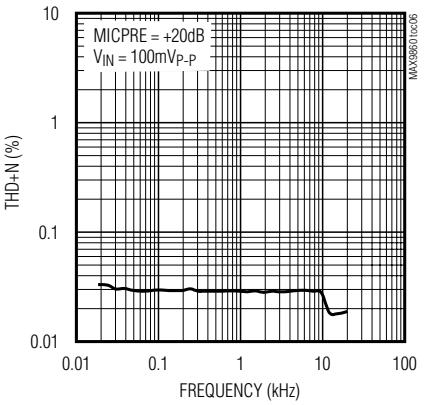

**TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HP)**



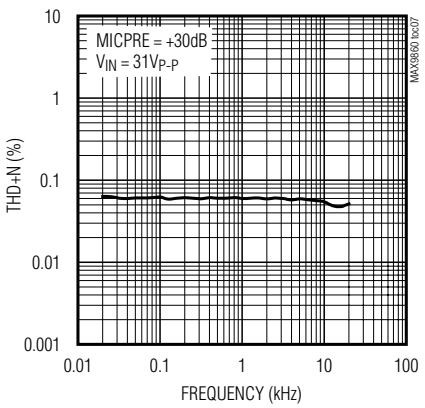

**TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICL TO ADC)**



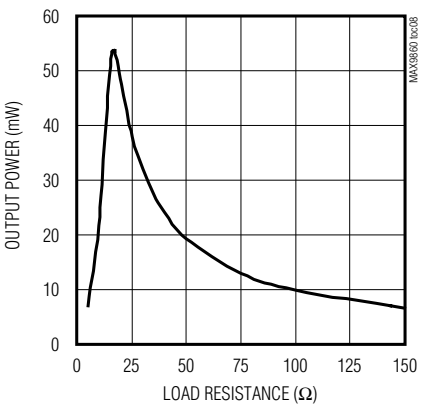

**TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICL TO ADC)**



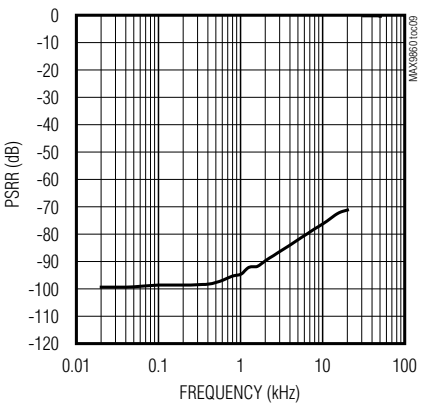

**TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICL TO ADC)**




**HEADPHONE OUTPUT POWER vs. LOAD RESISTANCE**



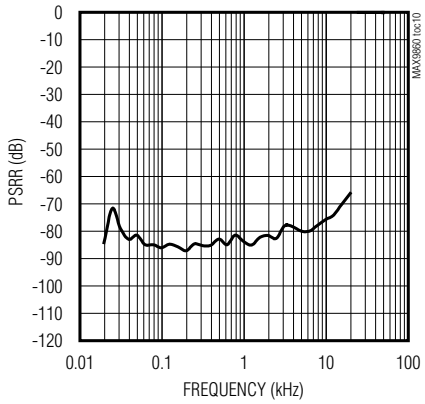

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HP)**



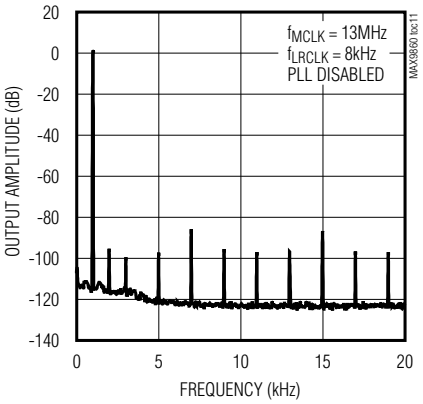
## Typical Operating Characteristics (continued)

($V_{AVDD}$ = +1.8V, $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{PREG}$ = $C_{REG}$ = 1µF, $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, $A_{VPRE}$ = +20dB, $f_{MCLK}$ = 13MHz, $T_A$ = +25°C, unless otherwise noted.)

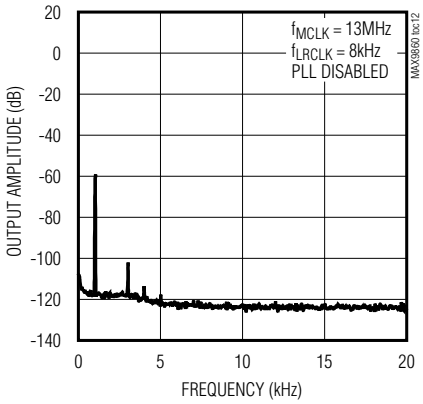
**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)**



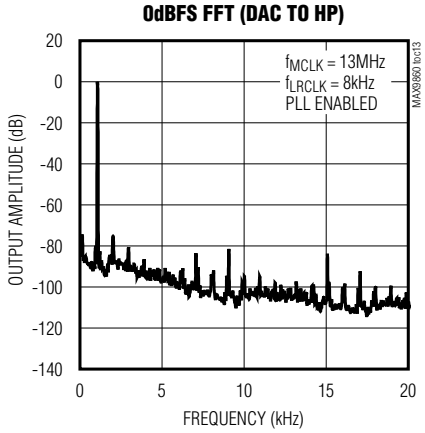

**0dBFS FFT (DAC TO HP)**



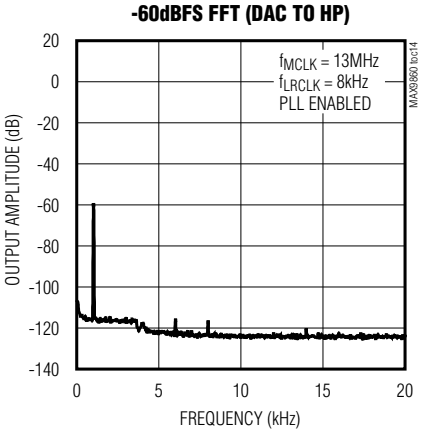

**-60dBFS FFT (DAC TO HP)**



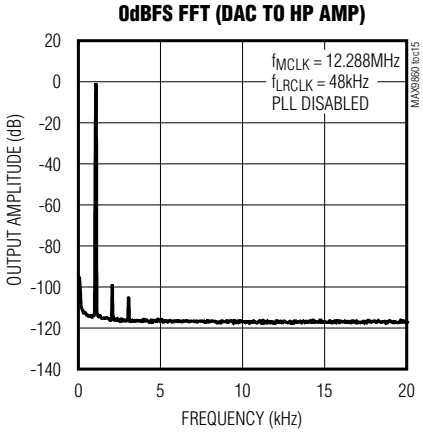

**0dBFS FFT (DAC TO HP)**



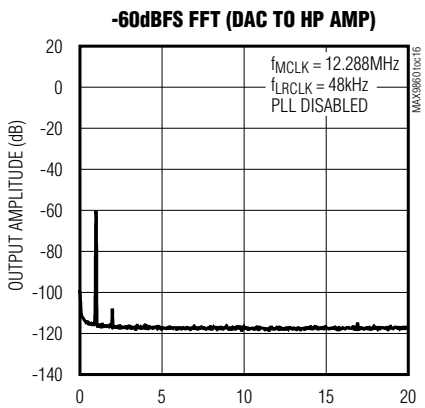

**-60dBFS FFT (DAC TO HP)**



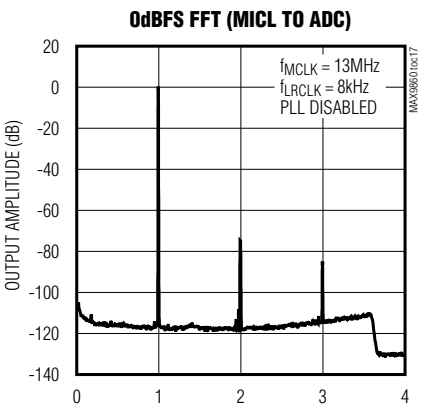

**0dBFS FFT (DAC TO HP AMP)**



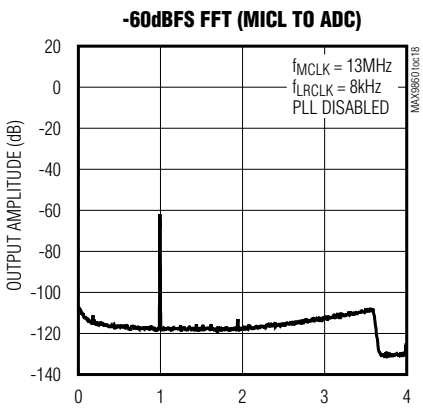

**-60dBFS FFT (DAC TO HP AMP)**




**0dBFS FFT (MICL TO ADC)**



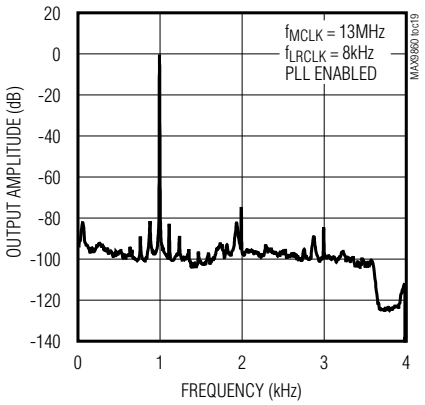

**-60dBFS FFT (MICL TO ADC)**



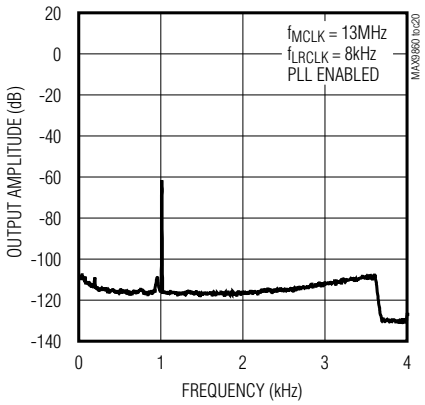
## Typical Operating Characteristics (continued)

($V_{AVDD}$ = +1.8V, $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{PREG}$ = $C_{REG}$ = 1µF, $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, $A_{VPRE}$ = +20dB, $f_{MCLK}$ = 13MHz, $T_A$ = +25°C, unless otherwise noted.)

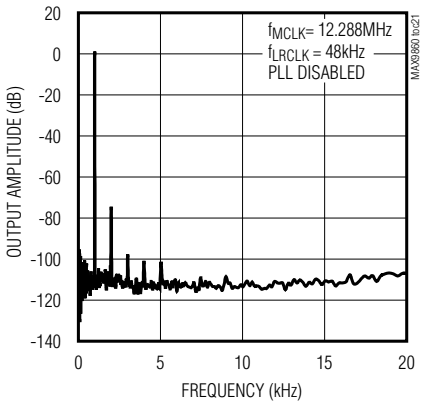
**0dBFS FFT (MICL TO ADC)**



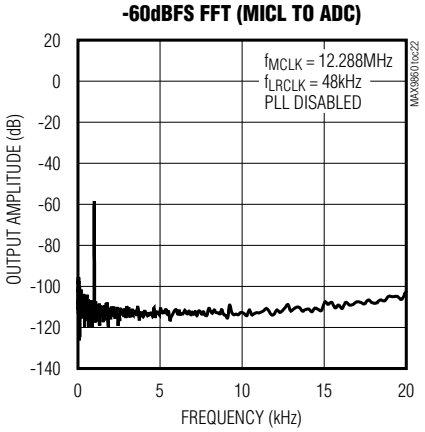

**-60dBFS FFT (MICL TO ADC)**



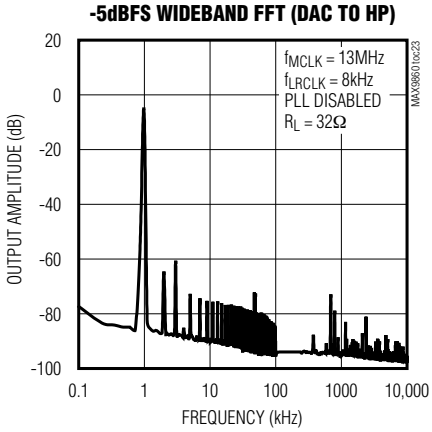

**0dBFS FFT (MICL TO ADC)**



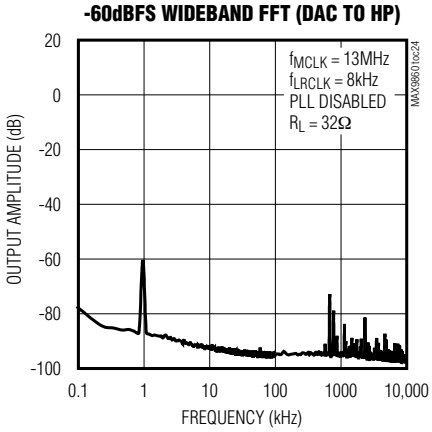

**-60dBFS FFT (MICL TO ADC)**



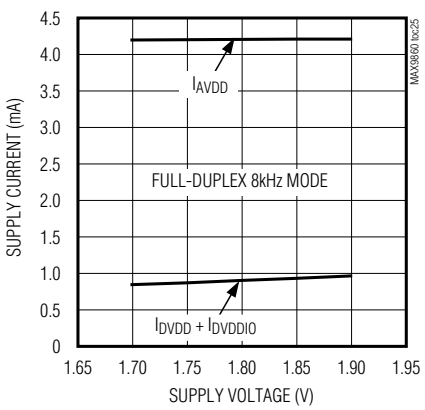

**-5dBFS WIDEBAND FFT (DAC TO HP)**



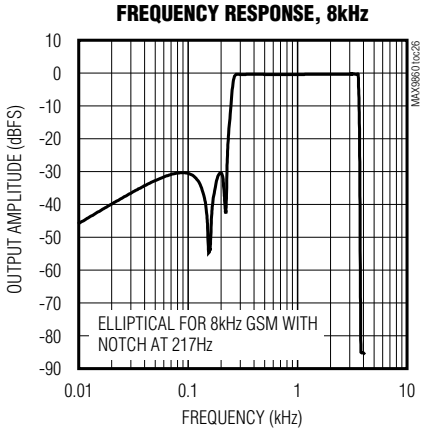

**-60dBFS WIDEBAND FFT (DAC TO HP)**



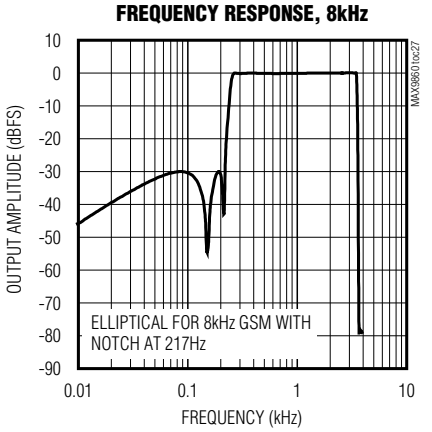

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**




**DAC DIGITAL FILTER FREQUENCY RESPONSE, 8kHz**



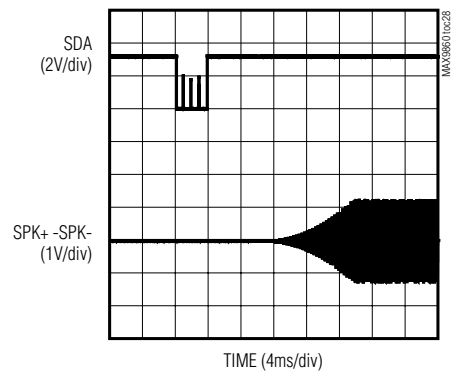

**ADC DIGITAL FILTER FREQUENCY RESPONSE, 8kHz**



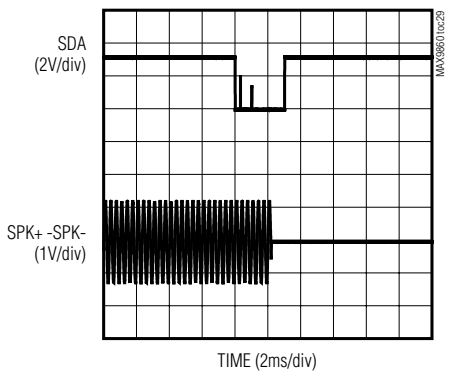
## Typical Operating Characteristics (continued)

($V_{AVDD}$ = +1.8V, $V_{DVDD}$ = $V_{DVDDIO}$ = +1.8V, $R_L$ = ∞, headphone load ($R_L$) connected between OUTP and OUTN, $C_{REF}$ = 2.2µF, $C_{PREG}$ = $C_{REG}$ = 1µF, $C_{MICBIAS}$ = 1µF $A_{VMICPGA}$ = 0dB, $A_{VPRE}$ = +20dB, $f_{MCLK}$ = 13MHz, $T_A$ = +25°C, unless otherwise noted.)

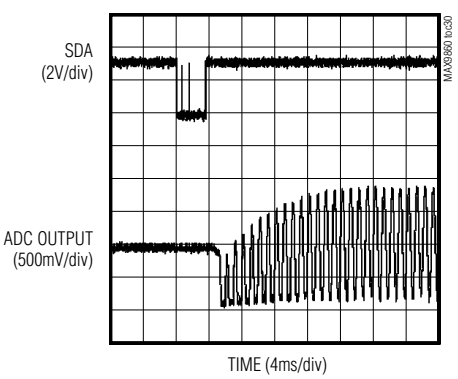
**HEADPHONE STARTUP WAVEFORM**



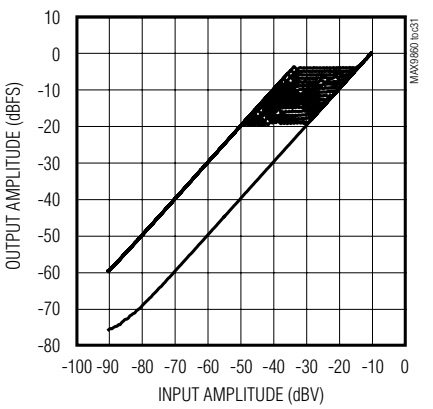

**HEADPHONE SHUTDOWN WAVEFORM**



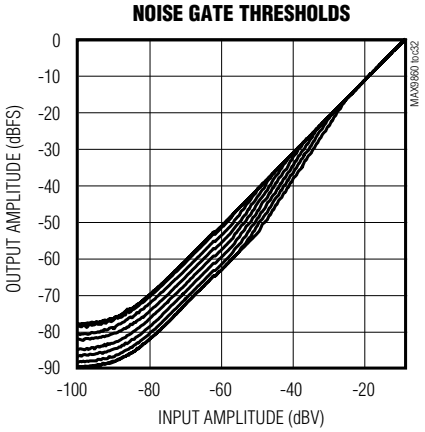

**SOFT-START ADC**



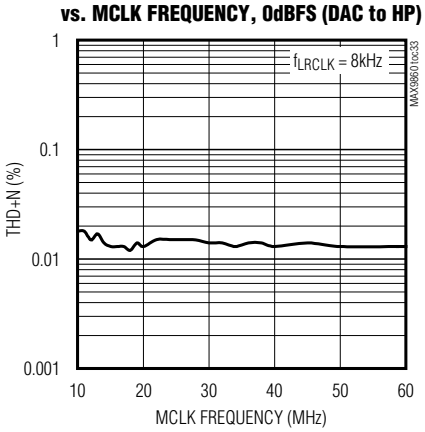

**AUTOMATIC GAIN CONTROL THRESHOLDS**



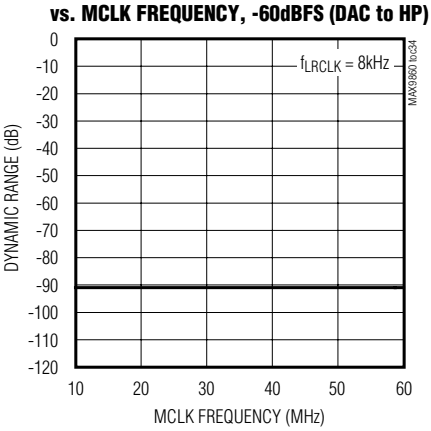

**NOISE GATE THRESHOLDS**




**TOTAL HARMONIC DISTORTION + NOISE vs. MCLK FREQUENCY, 0dBFS (DAC to HP)**




**DYNAMIC RANGE vs. MCLK FREQUENCY, -60dBFS (DAC to HP)**



## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | MICBIAS | Microphone Bias. +1.55V microphone bias for internal and/or external microphone. An external resistor from 2.2kΩ to 470Ω should be used to set the microphone current. Bypass to MICGND with a 1µF capacitor. |
| 2 | REG | Internal Bias. PREG/2 voltage reference. Bypass to AGND with a 1µF capacitor (+0.8V). |
| 3 | PREG | Positive Internal Regulated Supply. Bypass to AGND with a 1µF capacitor (+1.6V). |
| 4 | REF | Converter Reference (1.23V). Bypass to AGND with a 2.2µF capacitor. |
| 5 | AGND | Analog Ground |
| 6 | AVDD | Analog Power Supply. Bypass to AGND with 10µF and 0.1µF capacitors. |
| 7 | OUTP | Positive Headphone Output |
| 8 | OUTN | Negative Headphone Output |
| 9 | SDA | I²C Serial-Data Input/Output |
| 10 | SCL | I²C Serial-Data Clock |
| 11 | DVDDIO | Digital Interface Power Supply. Supply for digital audio interface. Bypass to DGND with a 1µF capacitor. |
| 12 | DGND | Digital Ground |
| 13 | DVDD | Digital Core Power Supply. Bypass to DGND with a 1µF capacitor. |
| 14 | MCLK | Master Clock Input |
| 15 | SDOUT | Serial Audio Interface ADC Data Output |
| 16 | SDIN | Serial Audio Interface DAC Data Input |
| 17 | LRCLK | Serial Audio Interface Left/Right Clock |
| 18 | BCLK | Serial Audio Interface Bit Clock |
| 19 | $\overline{IRQ}$ | Interrupt Request. $\overline{IRQ}$ is an active-low open drain output. Pull up to DVDDIO with a 10kΩ resistor. |
| 20 | MICRN | Negative Right Microphone Input. AC-couple to low-side of microphone or connect to negative signal. AC-couple to ground for single-ended operation. |
| 21 | MICRP | Positive Right Microphone Input. AC-couple to high-side of microphone or connect to positive signal. AC-couple the signal for single-ended operation. |
| 22 | MICLN | Negative Left Microphone Input. AC-couple to low-side of microphone or connect to negative signal. AC-couple to ground for single-ended operation. |
| 23 | MICLP | Positive Left Microphone Input. AC-couple to high-side of microphone or connect to positive signal. AC-couple the signal for single-ended operation. |
| 24 | MICGND | MICBIAS Ground. Connect to AGND. |
| — | EP | Exposed Pad. Connect to AGND. |

## Detailed Description

The MAX9860 low-power, voiceband, mono audio codec provides a complete audio solution for wireless voice headsets and other mono audio devices.

The mono playback path accepts digital audio over a flexible digital audio interface compatible with I²S, TDM, and left-justified audio signals. An oversampling sigma-delta DAC converts an incoming digital data stream to analog audio and outputs through the mono bridge-tied load headphone amplifier.

The stereo record path has two microphone inputs with selectable gain. The microphones are powered by an integrated microphone bias. An oversampling sigma-delta ADC converts the microphone signals and outputs the digital bit stream over the digital audio interface.

The record path includes automatic gain control (AGC) to optimize the signal level and a noise gate to reduce idle noise. The automatic gain control monitors the outputs of the ADC and makes constant adjustments to the input gain to reduce the dynamic range of the incoming microphone signal by up to 20dB. The noise gate corrects for the increase in noise typically associated with AGC by lowering the gain when there is no audio signal.

Integrated digital filtering provides a range of notch and highpass filters for both the playback and record paths to limit undesirable low-frequency signals and GSM transmission noise. The digital filtering provides attenuation of out-of-band energy by up to 76dB, eliminating audible aliasing. A digital sidetone function allows audio from the record path to be summed into the playback path after digital filtering.

The MAX9860's flexible clock circuitry utilizes a programmable clock divider and a digital PLL to allow the DAC and ADC to operate at maximum dynamic range for all combinations of master clock (MCLK) and sample rate (LRCLK). Any master clock between 10MHz to 60MHz is supported as are all sample rates from 8kHz to 48kHz. Master and slave mode are supported for maximum flexibility.

## I²C Registers

The MAX9860 audio codec is completely controlled through software using an I²C interface. The power-on default setting is software shutdown, requiring that the internal registers be programmed to activate the device. See Table 1 for the device's complete register map.

### I²C Slave Address

The MAX9860 responds to the slave address 0x20 for all write commands and 0x21 for all read operations.

## Table 1. I²C Register Map

| REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | REGISTER ADDRESS | POR | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **STATUS/INTERRUPT** | | | | | | | | | | | |
| Interrupt Status | CLD | SLD | ULK | 0 | 0 | 0 | 0 | 0 | 0x00 | — | R |
| Microphone NG/AGC Readback | NG | | | AGC | | | | | 0x01 | — | R |
| Interrupt Enable | ICLD | ISLD | IULK | 0 | 0 | 0 | 0 | 0 | 0x02 | 0x00 | R/W |
| **CLOCK CONTROL** | | | | | | | | | | | |
| System Clock | 0 | 0 | PSCLK | | 0 | FREQ | | 16KHZ | 0x03 | 0x00 | R/W |
| Stereo Audio Clock Control High | PLL | NHI | | | | | | | 0x04 | 0x00 | R/W |
| Stereo Audio Clock Control Low | NLO | | | | | | | | 0x05 | 0x00 | R/W |
| **DIGITAL AUDIO INTERFACE** | | | | | | | | | | | |
| Interface | MAS | WCI | DBCI | DDLY | HIZ | TDM | 0 | 0 | 0x06 | 0x00 | R/W |
| Interface | 0 | 0 | ABCI | ADLY | ST | BSEL | | | 0x07 | 0x00 | R/W |
| **DIGITAL FILTERING** | | | | | | | | | | | |
| Voice Filter | AVFLT | | | | DVFLT | | | | 0x08 | 0x00 | R/W |
| **DIGITAL LEVEL CONTROL** | | | | | | | | | | | |
| DAC Attenuation | DVA | | | | | | | | 0x09 | 0x00 | R/W |
| ADC Output Levels | ADCRL | | | | ADCLL | | | | 0x0A | 0x00 | R/W |
| DAC Gain and Sidetone | 0 | DVG | | DVST | | | | | 0x0B | 0x00 | R/W |
| **MICROPHONE LEVEL CONTROL** | | | | | | | | | | | |
| Microphone Gain | 0 | PAM | | PGAM | | | | | 0x0C | 0x00 | R/W |
| **RESERVED** | | | | | | | | | | | |
| Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0D | 0x00 | |
| **MICROPHONE AUTOMATIC GAIN CONTROL** | | | | | | | | | | | |
| Microphone AGC | AGCSRC | AGCRLS | | | AGCATK | | | AGCHLD | 0x0E | 0x00 | R/W |
| Noise Gate, Microphone AGC | ANTH | | | | AGCTH | | | | 0x0F | 0x00 | R/W |
| **POWER MANAGEMENT** | | | | | | | | | | | |
| System Shutdown | $\overline{\text{SHDN}}$ | 0 | 0 | 0 | DACEN | 0 | ADCLEN | ADCREN | 0x10 | 0x00 | R/W |

### Status/Interrupt

Status registers 0x00 and 0x01 are read-only registers that report the status of various device functions. The status register bits are cleared upon a read operation of the status register and are set the next time the event occurs. Register 0x02 determines whether or not the status flags in register 0x00 simultaneously sets $\overline{IRQ}$ high.

## Table 2. Status/Interrupt Registers

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x00 | CLD | SLD | ULK | 0 | 0 | 0 | 0 | 0 |
| 0x01 | NG | | | AGC | | | | |
| 0x02 | ICLD | ISLD | IULK | 0 | 0 | 0 | 0 | 0 |

| BITS | FUNCTION | |
|---|---|---|
| CLD | Clip Detect Flag. Indicates that a signal has become clipped in the ADC or DAC digital signal paths. CLD also indicates that the AGC function, when enabled, has set the microphone PGA to 0dB and no further gain reduction is possible. | |
| SLD | Slew Level Detect Flag. When volume or gain changes are made, the slewing circuitry smoothly steps through all intermediate settings. When SLD is set high, all slewing has completed and the volume or gain is at its final value. | |
| ULK | Digital PLL Unlock Flag. Indicates that the digital audio PLL for the ADC or DAC has become unlocked and digital signal data is not reliable. When beginning operation in master mode, this flag goes high and can be cleared by reading the status register. | |
| NG | Noise Gate Attenuation. When the noise gate is enabled these bits indicate the current noise gate attenuation. | |
| | Code | Attenuation |
| | 000 | 0dB |
| | 001 | 1dB |
| | 010 | 2dB |
| | 011 | 3dB |
| | 100 | 6dB |
| | 101 | 8dB |
| | 110 | 10dB |
| | 111 | 12dB |
| AGC | AGC Gain. When the AGC is enabled these bits indicate the AGC controlled level to the MIC preamp. The levels indicated by these bits correspond to the levels defined for the PGAM bits described in register 0x0C. | |

### Clock Control

The MAX9860 can work with a master clock (MCLK) supplied from any system clock within the range of 10MHz to 60MHz. Internally, the MAX9860 requires a 10MHz to 20MHz clock so a prescaler divides by 1, 2, or 4 to create the internal clock (PCLK). PCLK is used to clock all portions of the MAX9860.

The MAX9860 is capable of supporting any sample rate from 8kHz to 48kHz, including all common sample rates (8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, 48kHz). To accommodate a wide range of system architectures, the MAX9860 supports three main clocking modes:

**Normal Mode:** This mode uses a 15-bit clock divider coefficient to set the sample rate relative to the prescaled MCLK input (PCLK). This allows high flexibility in both the MCLK and LRCLK frequencies and can be used in either master or slave mode.

**Exact Integer Mode:** Common MCLK frequencies (12MHz, 13MHz, and 19.2MHz) can be programmed to operate in exact integer mode for both 8kHz and 16kHz sample rates. In these modes, the MCLK and LRCLK rates are selected by using the FREQ and 16KHZ bits instead of the NHI, NLO, and PLL control bits.

**PLL Mode:** When operating in slave mode, a PLL can be enabled to lock onto externally generated LRCLK signals that are asynchronously related to PCLK.

## Table 3. Clock Control Registers

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x03 | 0 | 0 | PSCLK | | 0 | FREQ | | 16KHZ |
| 0x04 | PLL | NHI | | | | | | |
| 0x05 | NLO | | | | | | | |

| BITS | FUNCTION |
|---|---|
| PSCLK[1:0] | **MCLK Prescaler**<br>Divides MCLK down to generate a PCLK between 10MHz and 20MHz.<br><br>00 = Disable clock for low-power shutdown.<br>01 = Select if MCLK is between 10MHz and 20MHz.<br>10 = Select if MCLK is between 20MHz and 40MHz.<br>11 = Select if MCLK is greater than 40MHz. |
| FREQ[1:0] | **Integer Clock Mode**<br>Enables exact integer mode for three predefined PCLK frequencies. Exact integer mode is normally intended for master mode, but can be enabled in slave mode if the externally supplied LRCLK exactly matches the frequency specified in each mode.<br><br>00 = Normal operation (configure clocking with the PLL, NHI, and NLO bits).<br>01 = Select when PCLK is 12MHz (LRCLK = PCLK/1500 or PCLK/750).<br>10 = Select when PCLK is 13MHz (LRCLK = PCLK/1625 or PCLK/812.5).<br>11 = Select when PCLK is 19.2MHz (LRCLK = PCLK/2400 or PCLK/1200).<br><br>When FREQ ≠ 00, the PLL, NHI, and NLO bits are unused. |
| 16KHZ | **16kHz Mode**<br>When FREQ ≠ 00:<br>0 = LRCLK is exactly 8kHz.<br>1 = LRCLK is exactly 16kHz.<br><br>When FREQ = 00, 16KHZ is used to set the AGC clock rate:<br>0 = Use when LRCLK ≤ 24kHz.<br>1 = Use when LRCLK > 24kHz. |

## Table 3. Clock Control Registers (continued)

| BITS | FUNCTION |
|---|---|
| PLL | **PLL Enable**<br>0 = (Valid for slave and master mode)—The frequency of LRCLK is set by the NHI and NLO divider bits. Set PLL = 0 in slave mode only if the externally generated LRCLK can be exactly selected using the LRCLK divider.<br><br>1 = (Valid for slave mode only)—Used when the audio master generates an LRCLK not selectable using the LRCLK divider. A digital PLL locks on to the externally supplied LRCLK signal regardless of the MCLK frequency.<br><br>**Rapid Lock Mode**<br>To enable rapid lock mode set NHI and NLO to the nearest desired ratio and set NLO[0] = 1 (Register 0x05, bit 0) before setting the PLL mode bit. |
| NHI and NLO | **LRCLK Divider**<br>NHI and NLO control a 15-bit clock divider (N). When the PLL = 0 and FREQ = 00, the frequency of LRCLK is determined by the clock divider. See Table 4 for common N values.<br><br>$N = (65{,}536 \times 96 \times f_{LRCLK})/f_{PCLK}$<br>$f_{LRCLK}$ = LRCLK frequency<br>$f_{PCLK}$ = prescaled MCLK internal clock frequency (PCLK) |

## Table 4. Common N Values

| MCLK (MHz) | LRCLK (kHz) | | | | | |
|---|---|---|---|---|---|---|
| | **PSCLK** | **8** | **16** | **32** | **44.1** | **48** |
| **11.2896** | 01 | 116A | 22D4 | 45A9 | ***6000*** | 687D |
| **12** | 01 | 1062 | 20C5 | 4189 | 5A51 | 624E |
| **12.288** | ***01*** | ***1000*** | ***2000*** | ***4000*** | 5833 | ***6000*** |
| **13** | 01 | F20 | 1E3F | 3C7F | 535F | 5ABE |
| **19.2** | 01 | A3D | 147B | 28F6 | 3873 | 3D71 |
| **24** | 10 | 1062 | 20C5 | 4189 | 5A51 | 624E |
| **26** | 10 | F20 | 1E3F | 3C7F | 535F | 5ABE |
| **27** | 10 | E90 | 1D21 | 3A41 | 5048 | 5762 |

***Note:*** *Values in bold italics are exact integers that provide maximum full-scale performance.*

### Digital Audio Interface

The MAX9860's digital audio interface supports a wide range of operating modes to ensure maximum compatibility. See Figures 1 through 4 for timing diagrams. In master mode, the MAX9860 outputs LRCLK and BCLK, while in slave mode, they are inputs. When operating in master mode, BCLK can be configured in a number of ways to ensure compatiblity with other audio devices.

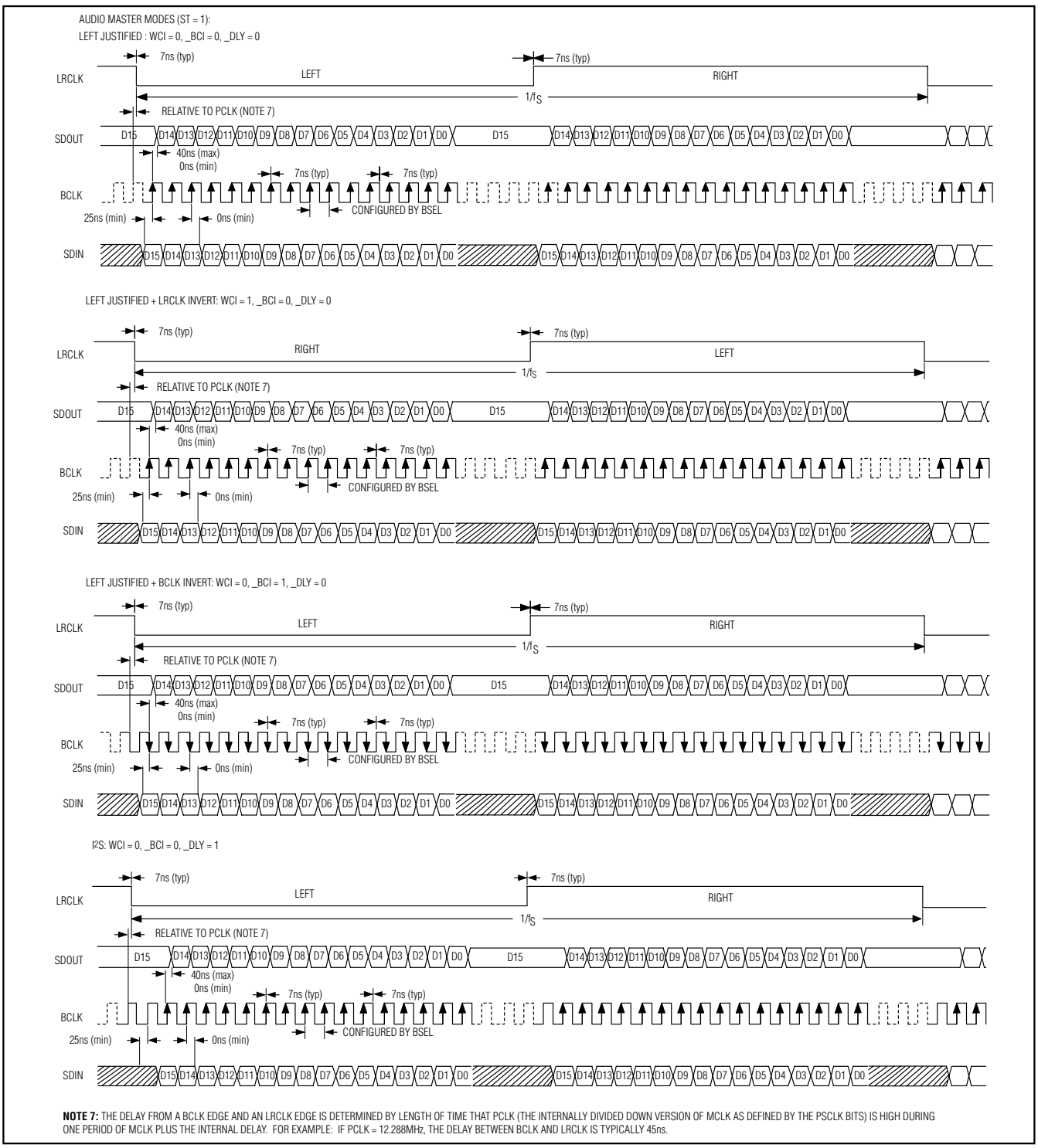
## Table 5. Digital Audio Interface Registers

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x06 | MAS | WCI | DBCI | DDLY | HIZ | TDM | 0 | 0 |
| 0x07 | 0 | 0 | ABCI | ADLY | ST | BSEL | | |

| BITS | FUNCTION |
|---|---|
| MAS | **Master Mode**<br>0 = The MAX9860 operates in slave mode with LRCLK and BCLK configured as inputs.<br>1 = The MAX9860 operates in master mode with LRCLK and BCLK configured as outputs. |
| WCI | **LRCLK Invert**<br>0 = Left-channel data is input and output while LRCLK is low.<br>1 = Right-channel data is input and output while LRCLK is low.<br><br>WCI is ignored when TDM = 1. |
| DBCI | **DAC BCLK Invert (must be set to ABCI)**<br>In master and slave mode:<br>0 = SDIN is latched into the part on the rising edge of BCLK.<br>1 = SDIN is latched into the part on the falling edge of BCLK.<br><br>In master mode:<br>0 = LRCLK changes state following the rising edge of BCLK.<br>1 = LRCLK changes state following the falling edge of BCLK. |
| DDLY | **DAC Delay Mode**<br>0 = SDIN data is latched on the first BCLK edge following an LRCLK edge.<br>1 = SDIN data is assumed to be delayed one BCLK cycle so that it is latched on the 2nd BCLK edge following an LRCLK edge ($I^2S$-compatible mode).<br><br>DDLY is ignored when TDM = 1. |
| HIZ | **SDOUT High-Impedance Mode**<br>0 = SDOUT is set either high or low after all data bits have been transferred out of the part.<br>1 = SDOUT goes to a high-impedance state after all data bits have been transferred out of the part, allowing SDOUT to be shared by other devices.<br><br>Use HIZ only when TDM = 1. |
| TDM | **TDM Mode Select**<br>0 = LRCLK signal polarity indicates left and right audio.<br>1 = LRCLK is a framing pulse which transitions polarity to indicate the start of a frame of audio data consisting of multiple channels.<br><br>When operating in TDM mode the left channel is output immediately following the frame sync pulse. If right-channel data is being transmitted, the 2nd channel of data immediately follows the 1st channel data. |
| ABCI | **ADC BCLK Invert (must be set to DBCI)**<br>0 = SDOUT is valid on the rising edge of BCLK and transitions immediately after the rising edge.<br>1 = SDOUT is valid on the falling edge of BCLK and transitions immediately after the falling edge. |

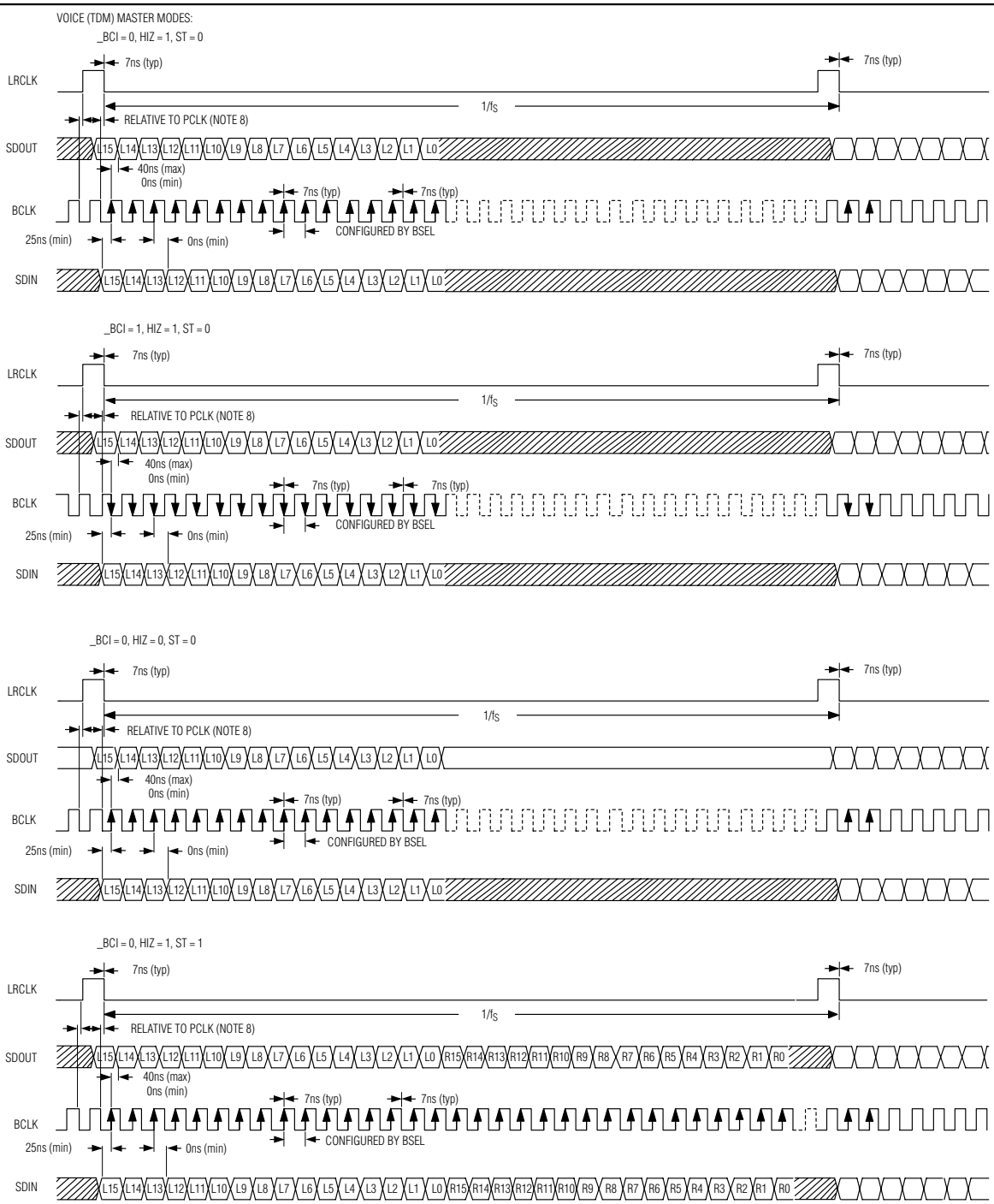
## Table 5. Digital Audio Interface Registers (continued)

| BITS | FUNCTION |
|---|---|
| ADLY | **ADC Delay Mode**<br>0 = SDOUT data is valid on the first BCLK edge following an LRCLK edge.<br>1 = SDOUT data is delayed one BCLK cycle so that it is valid on the 2nd BCLK edge following an LRCLK edge ($I^2S$-compatible mode).<br><br>ADLY is ignored when TDM = 1. |
| ST | **Stereo Enable**<br>0 = The interface transmits and receives only one channel of data. If right record path is enabled, no data from this channel is transmitted.<br>1 = The interface operates in stereo. The left and right incoming data are summed to mono and then routed to the DAC. The summed data is divided by 2 to prevent overload. Both the left and right record signals are transmitted. |
| BSEL | **BCLK Select**<br>Configures BCLK when operating in master mode. BSEL has no effect in slave mode. Set BSEL = 010, unless sharing the bus with multiple devices.<br><br>000 = Off<br>001 = 64x LRCLK (192x internal clock divided by 3)<br>010 = 48x LRCLK (192x internal clock divided by 4)<br>011 = Reserved for future use.<br>100 = PCLK/2<br>101 = PCLK/4<br>110 = PCLK/8<br>111 = PCLK/16 |




**NOTE 7:** THE DELAY FROM A BCLK EDGE AND AN LRCLK EDGE IS DETERMINED BY LENGTH OF TIME THAT PCLK (THE INTERNALLY DIVIDED DOWN VERSION OF MCLK AS DEFINED BY THE PSCLK BITS) IS HIGH DURING ONE PERIOD OF MCLK PLUS THE INTERNAL DELAY. FOR EXAMPLE: IF PCLK = 12.288MHz, THE DELAY BETWEEN BCLK AND LRCLK IS TYPICALLY 45ns.

*Figure 1. Digital Audio Interface Audio Master Mode Examples*




**NOTE 8:** THE DELAY FROM A BCLK EDGE AND AN LRCLK EDGE IS DETERMINED BY LENGTH OF TIME THAT PCLK (THE INTERNALLY DIVIDED DOWN VERSION OF MCLK AS DEFINED BY THE PSCLK BITS) IS HIGH DURING ONE PERIOD OF MCLK PLUS THE INTERNAL DELAY. FOR EXAMPLE: IF PCLK = 12.288MHz, THE DELAY BETWEEN BCLK AND LRCLK IS TYPICALLY 45ns.

*Figure 2. Digital Audio Interface Voice Master Mode Examples*

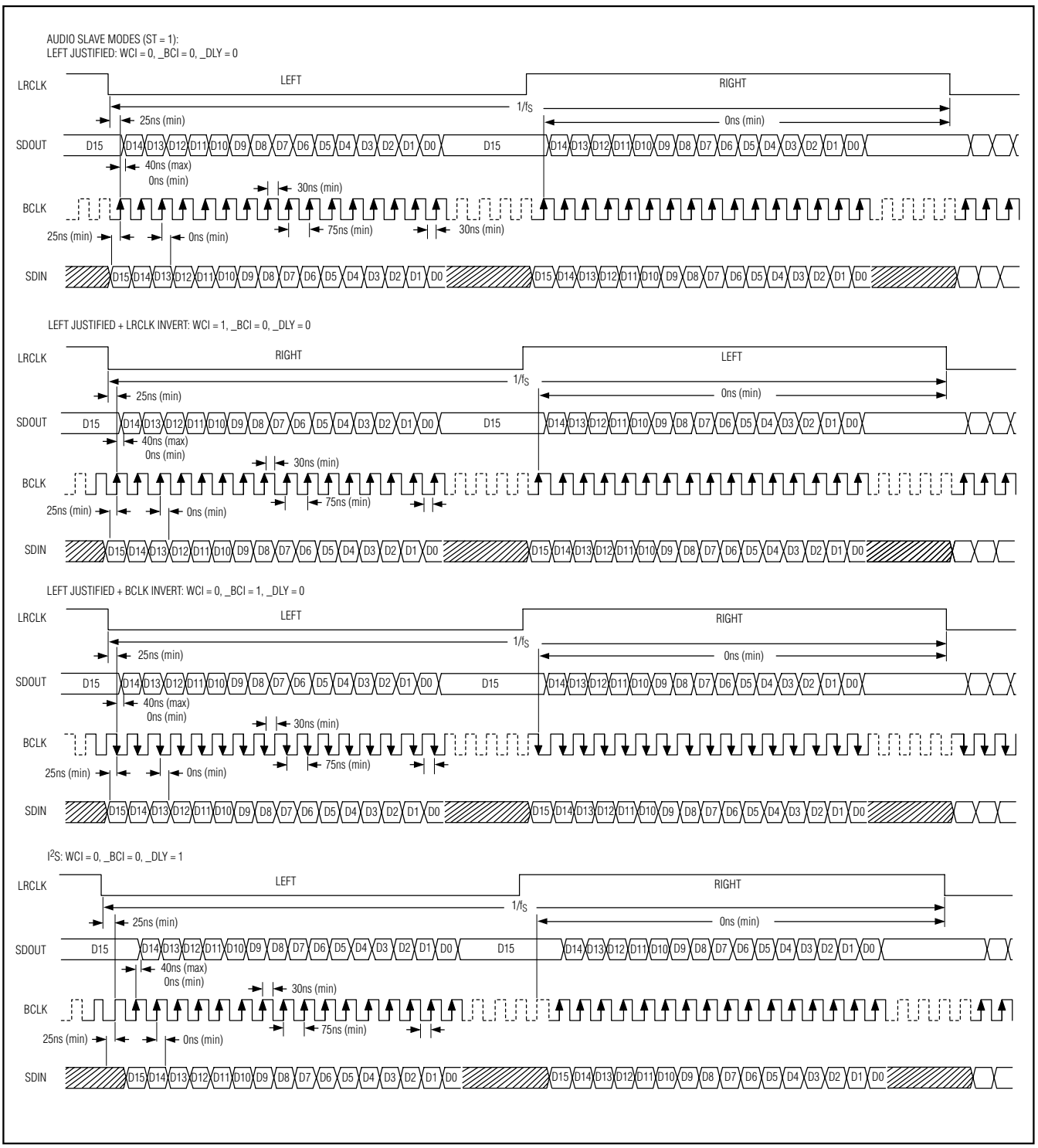



*Figure 3. Digital Audio Interface Audio Slave Mode Examples*

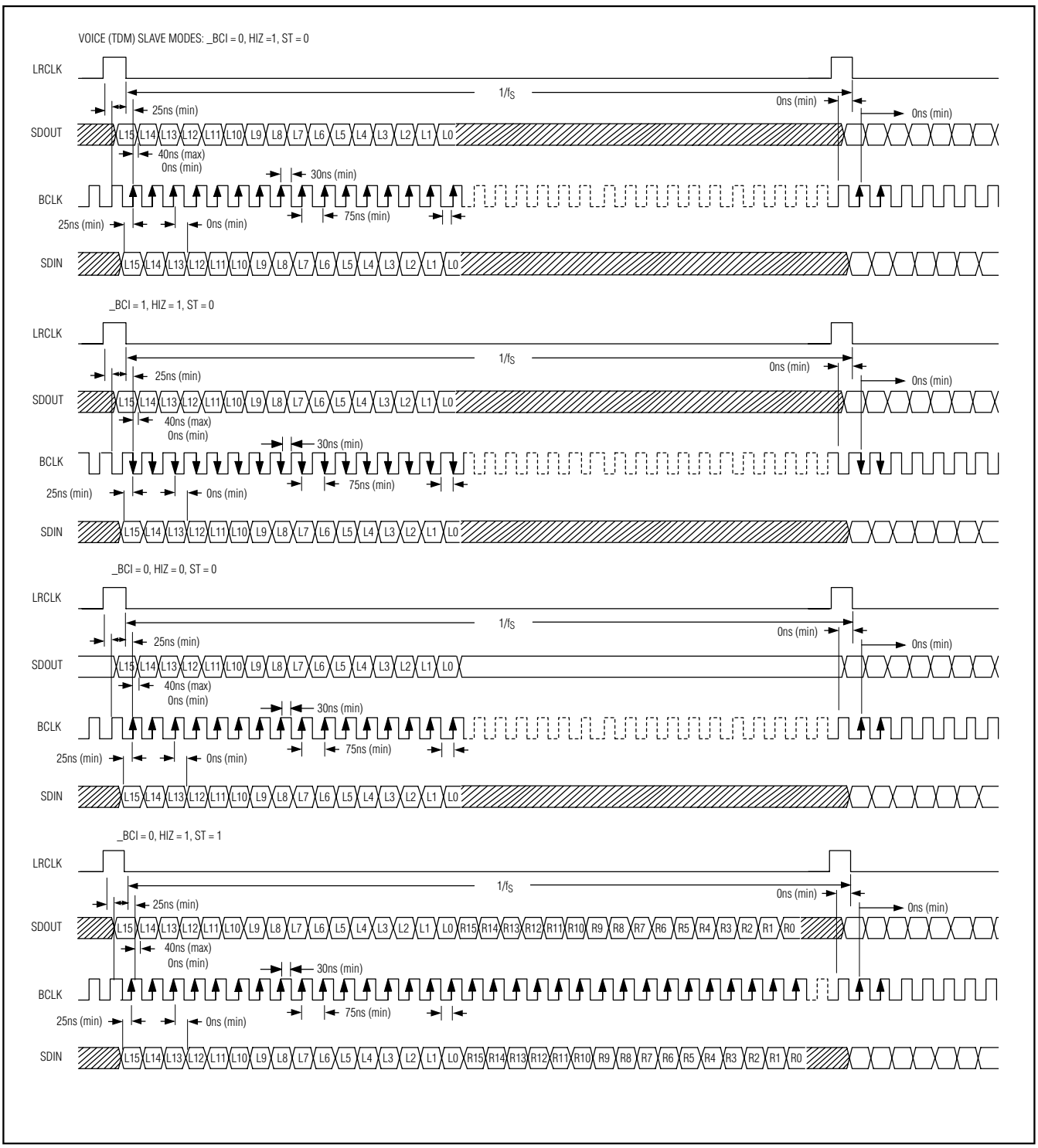



*Figure 4. Digital Audio Interface Voice Slave Mode Examples*

### Digital Filtering

The MAX9860 incorporates selecable highpass and notch filters for both the playback and record paths. Each filter is valid for a specific sample rate.

## Table 6. Digital Filter Registers

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x08 | AVFLT | | | | DVFLT | | | |

| BITS | FUNCTION |
|---|---|
| **AVFLT** | ADC Voice Filter Frequency Select. See Table 7. |
| **DVFLT** | DAC Voice Filter Frequency Select. See Table 7. |

## Table 7. Digital Filters

| CODE | FILTER TYPE | SAMPLE RATE | DESCRIPTION |
|---|---|---|---|
| 0x0 | — | — | Disabled |
| 0x1 | Elliptical | 16kHz | Elliptical highpass with 217Hz notch |
| 0x2 | Butterworth | 16kHz | 500Hz Butterworth highpass |
| 0x3 | Elliptical | 8kHz | Elliptical highpass with 217Hz notch |
| 0x4 | Butterworth | 8kHz | 500Hz Butterworth highpass |
| 0x5 | Butterworth | 48kHz | 200Hz Butterworth highpass |
| 0x6 to 0xF | — | — | Reserved |

### Digital Level Control

The MAX9860 includes digital gain adjustment for the playback and record paths. Independent gain adjustment is provided for the two record channels. Sidetone gain adjustment is also provided to set the sidetone level relative to the playback level.

## Table 8. Digital Level Control Registers

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x09 | DVA | | | | | | | |
| 0x0A | ADCRL | | | | ADCLL | | | |
| 0x0B | 0 | DVG | | DVST | | | | |

| BITS | FUNCTION | | | | | |
|---|---|---|---|---|---|---|
| DVA | DAC Level Adjust<br>Adjusts the digital audio level before being converted by the DAC. The least significant bit of DVA is always 0. | | | | | |
| | **CODE** | **GAIN** | **CODE** | **GAIN** | **CODE** | **GAIN** |
| | 0x00 | +3 | 0x40 | -29 | 0x80 | -61 |
| | 0x02 | +2 | 0x42 | -30 | 0x82 | -62 |
| | 0x04 | +1 | 0x44 | -31 | 0x84 | -63 |
| | 0x06 | 0 | 0x46 | -32 | 0x86 | -64 |
| | 0x08 | -1 | 0x48 | -33 | 0x88 | -65 |
| | 0x0A | -2 | 0x4A | -34 | 0x8A | -66 |
| | 0x0C | -3 | 0x4C | -35 | 0x8C | -67 |
| | 0x0E | -4 | 0x4E | -36 | 0x8E | -68 |
| | 0x10 | -5 | 0x50 | -37 | 0x90 | -69 |
| | 0x12 | -6 | 0x52 | -38 | 0x92 | -70 |
| | 0x14 | -7 | 0x54 | -39 | 0x94 | -71 |
| | 0x16 | -8 | 0x56 | -40 | 0x96 | -72 |
| | 0x18 | -9 | 0x58 | -41 | 0x98 | -73 |
| | 0x1A | -10 | 0x5A | -42 | 0x9A | -74 |
| | 0x1C | -11 | 0x5C | -43 | 0x9C | -75 |
| | 0x1E | -12 | 0x5E | -44 | 0x9E | -76 |
| | 0x20 | -13 | 0x60 | -45 | 0xA0 | -77 |
| | 0x22 | -14 | 0x62 | -46 | 0xA2 | -78 |
| | 0x24 | -15 | 0x64 | -47 | 0xA4 | -79 |
| | 0x26 | -16 | 0x66 | -48 | 0xA6 | -80 |
| | 0x28 | -17 | 0x68 | -49 | 0xA8 | -81 |
| | 0x2A | -18 | 0x6A | -50 | 0xAA | -82 |
| | 0x2C | -19 | 0x6C | -51 | 0xAC | -83 |
| | 0x2E | -20 | 0x6E | -52 | 0xAE | -84 |
| | 0x30 | -21 | 0x70 | -53 | 0xB0 | -85 |
| | 0x32 | -22 | 0x72 | -54 | 0xB2 | -86 |
| | 0x34 | -23 | 0x74 | -55 | 0xB4 | -87 |
| | 0x36 | -24 | 0x76 | -56 | 0xB6 | -88 |
| | 0x38 | -25 | 0x78 | -57 | 0xB8 | -89 |
| | 0x3A | -26 | 0x7A | -58 | 0xBA | -90 |
| | 0x3C | -27 | 0x7C | -59 | ≥ 0xBC | MUTE |
| | 0x3E | -28 | 0x7E | -60 | — | — |

## Table 8. Digital Level Control Registers (continued)

<table>
<tr><th>BITS</th><th>FUNCTION</th></tr>
<tr><td>ADCRL/ADCLL</td><td>Left and Right ADC Output Level<br>Adjusts the digital audio level output by the ADCs.
<table>
<tr><th>CODE</th><th>GAIN</th></tr>
<tr><td>0x0</td><td>+3</td></tr>
<tr><td>0x1</td><td>+2</td></tr>
<tr><td>0x2</td><td>+1</td></tr>
<tr><td>0x3</td><td>0</td></tr>
<tr><td>0x4</td><td>-1</td></tr>
<tr><td>0x5</td><td>-2</td></tr>
<tr><td>0x6</td><td>-3</td></tr>
<tr><td>0x7</td><td>-4</td></tr>
<tr><td>0x8</td><td>-5</td></tr>
<tr><td>0x9</td><td>-6</td></tr>
<tr><td>0xA</td><td>-7</td></tr>
<tr><td>0xB</td><td>-8</td></tr>
<tr><td>0xC</td><td>-8</td></tr>
<tr><td>0xD</td><td>-10</td></tr>
<tr><td>0xE</td><td>-11</td></tr>
<tr><td>0xF</td><td>-12</td></tr>
</table></td></tr>
<tr><td>DVG</td><td>DAC Gain<br>The gain set by DVG adds to the level set by DVA.
<table>
<tr><th>CODE</th><th>GAIN</th></tr>
<tr><td>00</td><td>0</td></tr>
<tr><td>01</td><td>+6</td></tr>
<tr><td>10</td><td>+12</td></tr>
<tr><td>11</td><td>+18</td></tr>
</table></td></tr>
<tr><td>DVST</td><td>Sidetone<br>Sets the level of left ADC output mixed into the DAC.
<table>
<tr><th>CODE</th><th>GAIN</th><th>CODE</th><th>GAIN</th></tr>
<tr><td>0x00</td><td>Disabled</td><td>0x10</td><td>-30</td></tr>
<tr><td>0x01</td><td>0</td><td>0x11</td><td>-32</td></tr>
<tr><td>0x02</td><td>-2</td><td>0x12</td><td>-34</td></tr>
<tr><td>0x03</td><td>-4</td><td>0x13</td><td>-36</td></tr>
<tr><td>0x04</td><td>-6</td><td>0x14</td><td>-38</td></tr>
<tr><td>0x05</td><td>-8</td><td>0x15</td><td>-40</td></tr>
<tr><td>0x06</td><td>-10</td><td>0x16</td><td>-42</td></tr>
<tr><td>0x07</td><td>-12</td><td>0x17</td><td>-44</td></tr>
<tr><td>0x08</td><td>-14</td><td>0x18</td><td>-46</td></tr>
<tr><td>0x09</td><td>-16</td><td>0x19</td><td>-48</td></tr>
<tr><td>0x0A</td><td>-18</td><td>0x1A</td><td>-50</td></tr>
<tr><td>0x0B</td><td>-20</td><td>0x1B</td><td>-52</td></tr>
<tr><td>0x0C</td><td>-22</td><td>0x1C</td><td>-54</td></tr>
<tr><td>0x0D</td><td>-24</td><td>0x1D</td><td>-56</td></tr>
<tr><td>0x0E</td><td>-26</td><td>0x1E</td><td>-58</td></tr>
<tr><td>0x0F</td><td>-28</td><td>0x1F</td><td>-60</td></tr>
</table></td></tr>
</table>

### Microphone Inputs

The MAX9860 provides two differential microphone inputs and a low-noise 1.55V microphone bias for powering the microphones. In typical applications, the left microphone is used to record a voice signal and the right microphone is used to record a background noise signal. In applications that require only one microphone, use the left microphone input and disable the right ADC. The microphone signals are amplified by two stages of gain and then routed to the ADCs. The first stage offers selectable 0dB, 20dB, or 30dB settings. The second stage is a programmable gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps. Zero-crossing detection is included on the PGA to minimize zipper noise while making gain changes. See Figure 5 for a detailed diagram of the microphone input structure.

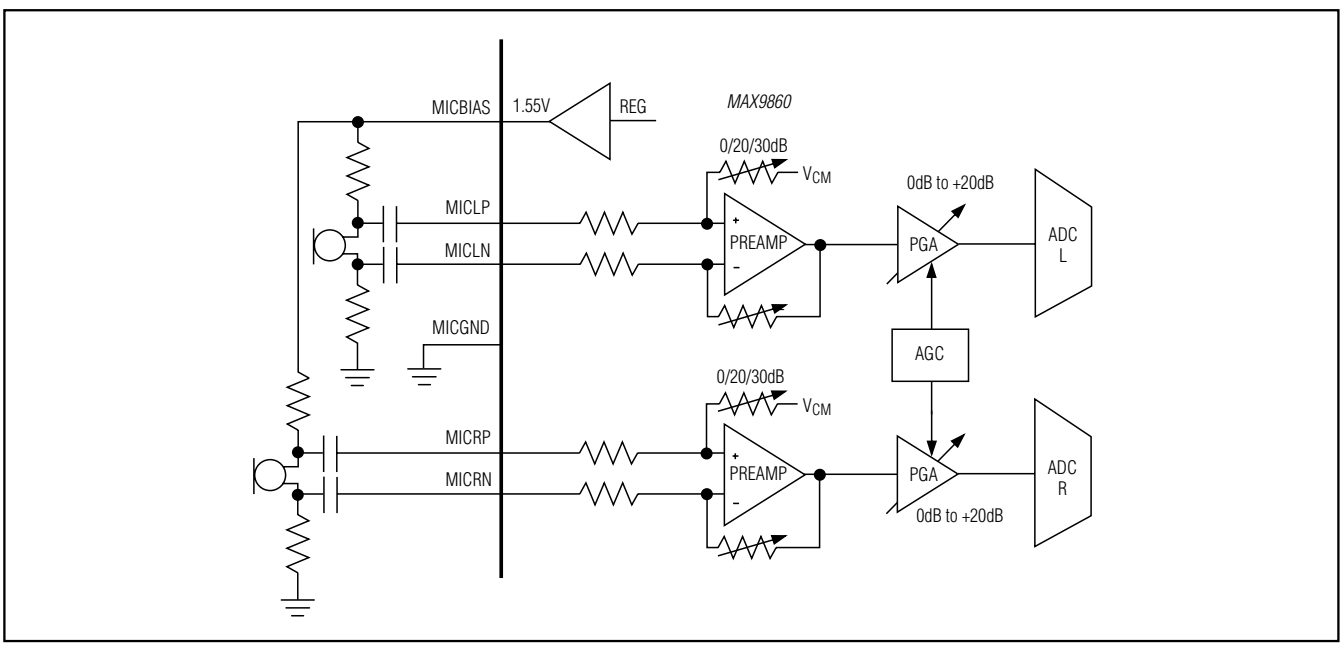



*Figure 5. Microphone Input Block Diagram*

## Table 9. Microphone Input Register

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x0C | 0 | PAM | | PGAM | | | | |

| BITS | FUNCTION |
|---|---|
| PAM | **Left and Right Microphone Preamp Gain**<br>**CODE** / **GAIN (dB)**<br>00 / Disabled<br>01 / 0<br>10 / +20<br>11 / +30<br>**Note:** Selecting 00 disables the microphone inputs and microphone bias automatically. |
| PGAM | **Left and Right Microphone PGA**<br>**CODE** / **GAIN (dB)** / **CODE** / **GAIN (dB)**<br>0x00 / +20 / 0x0B / +9<br>0x01 / +19 / 0x0C / +8<br>0x02 / +18 / 0x0D / +7<br>0x03 / +17 / 0x0E / +6<br>0x04 / +16 / 0x0F / +5<br>0x05 / +15 / 0x10 / +4<br>0x06 / +14 / 0x11 / +3<br>0x07 / +13 / 0x12 / +2<br>0x08 / +12 / 0x13 / +1<br>0x09 / +11 / ≥ 0x14 / 0<br>0x0A / +10 / — / —<br>**Note:** When AGC is enabled, the AGC controller overrides these settings. |

### Automatic Gain Control (AGC) and Noise Gate

The MAX9860 includes AGC on both microphone inputs. AGC is enabled by setting the hold time through AGCHLD. AGC dynamically controls the analog PGA microphone input gain to hold the level constant over a 20dB input range, enhancing the voice path operation for various use conditions. When AGC is enabled, it monitors the signal level at the output of the ADC and then makes gain adjustments by controlling the analog microphone PGA. When AGC is enabled, PGAM is not user programmable.

Since AGC increases the level of all signals below a user-defined threshold, the noise floor effectively is increased by 20dB. To counteract this, a noise gate is included to reduce the gain at low levels. Unlike typical noise gates that completely silence the output below a threshold, the noise gate in the MAX9860 reduces the gain for signals below the defined level. As the signal level becomes further below the threshold, the gain is further reduced. The Automatic Gain Control Thresholds and Noise Gate Thresholds graphs in the *Typical Operating Characteristics* show the resulting steady-state transfer curves when AGC and the noise gate are enabled.

## Table 10. AGC and Noise Gate Registers

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x0E | AGCSRC | AGCRLS | | | AGCATK | | AGCHLD | |
| 0x0F | ANTH | | | | AGCTH | | | |

| BITS | FUNCTION |
|---|---|
| AGCSRC | **AGC/Noise Gate Signal Source Select**<br>0 = The left ADC output is used by the AGC and noise gate.<br>1 = The sum of the left and right ADC outputs is used by the AGC and noise gate. |
| AGCRLS | **AGC Release Time**<br>Time taken by the AGC circuit to increase the gain from minimum to maximum. |

| CODE | TIME |
|---|---|
| 000 | 78ms |
| 001 | 156ms |
| 010 | 312ms |
| 011 | 625ms |
| 100 | 1.25s |
| 101 | 2.5s |
| 110 | 5s |
| 111 | 10s |

| BITS | FUNCTION |
|---|---|
| AGCATK | **AGC Attack Time**<br>The time constant of the AGC gain reduction curve. |

| CODE | TIME (ms) |
|---|---|
| 00 | 3 |
| 01 | 12 |
| 10 | 50 |
| 11 | 200 |

| BITS | FUNCTION |
|---|---|
| AGCHLD | **AGC Hold Time**<br>Time the AGC circuit waits before beginning to increase gain when a signal below the threshold is detected. |

| CODE | TIME (ms) |
|---|---|
| 00 | AGC disabled |
| 01 | 50 |
| 10 | 100 |
| 11 | 400 |

## Table 10. AGC and Noise Gate Registers (continued)

<table>
<tr><th>BITS</th><th colspan="5">FUNCTION</th></tr>
<tr><td rowspan="11">ANTH</td><td colspan="5">Noise Gate Threshold<br>The signal level at which the noise gate begins reducing the gain. When the signal level is above the threshold the noise gate has no effect. When the signal level is below the threshold, the noise gate decreases the gain by 1dB for every 2dB the signal is below the threshold.<br><br>The noise gate can be enabled independently from AGC. When AGC is enabled, PGAM must be set to +20dB (indicating a small signal is present) for the noise gate to attenuate.<br><br>For microphone signals, use the noise gate and AGC simultaneously with ANTH set between -16dB and -28dB.</td></tr>
<tr><td>ANTH[3:0]</td><td>LEVEL (dBFS)</td><td>ANTH[3:0]</td><td>LEVEL (dBFS)</td><td></td></tr>
<tr><td>0x0</td><td>Disabled</td><td>0x8</td><td>-44</td><td></td></tr>
<tr><td>0x1</td><td>-72</td><td>0x9</td><td>-40</td><td></td></tr>
<tr><td>0x2</td><td>-68</td><td>0xA</td><td>-36</td><td></td></tr>
<tr><td>0x3</td><td>-64</td><td>0xB</td><td>-32</td><td></td></tr>
<tr><td>0x4</td><td>-60</td><td>0xC</td><td>-28</td><td></td></tr>
<tr><td>0x5</td><td>-56</td><td>0xD</td><td>-24</td><td></td></tr>
<tr><td>0x6</td><td>-52</td><td>0xE</td><td>-20</td><td></td></tr>
<tr><td>0x7</td><td>-48</td><td>0xF</td><td>-16</td><td></td></tr>
<tr><td rowspan="11">AGCTH</td><td colspan="5">AGC Signal Threshold<br>The target output signal level. When the signal level is below the threshold, the AGC increases the gain. The signal level is measured after ADCRL and ADCLL are applied to the ADC output.</td></tr>
<tr><td>ANTH[3:0]</td><td>LEVEL (dBFS)</td><td>ANTH[3:0]</td><td>LEVEL (dBFS)</td><td></td></tr>
<tr><td>0x0</td><td>-3</td><td>0x8</td><td>-11</td><td></td></tr>
<tr><td>0x1</td><td>-4</td><td>0x9</td><td>-12</td><td></td></tr>
<tr><td>0x2</td><td>-5</td><td>0xA</td><td>-13</td><td></td></tr>
<tr><td>0x3</td><td>-6</td><td>0xB</td><td>-14</td><td></td></tr>
<tr><td>0x4</td><td>-7</td><td>0xC</td><td>-15</td><td></td></tr>
<tr><td>0x5</td><td>-8</td><td>0xD</td><td>-16</td><td></td></tr>
<tr><td>0x6</td><td>-9</td><td>0xE</td><td>-17</td><td></td></tr>
<tr><td>0x7</td><td>-10</td><td>0xF</td><td>-18</td><td></td></tr>
</table>

### Power Management

The MAX9860 includes complete power management control to minimize power usage. The DAC and both ADCs can be independently enabled so that only the required circuitry is active.

## Table 11. Power Management Register

| REGISTER ADDRESS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0x10 | $\overline{SHDN}$ | 0 | 0 | 0 | DACEN | 0 | ADCLEN | ADCREN |

| BITS | FUNCTION |
|---|---|
| $\overline{SHDN}$ | **Active-Low Software Shutdown**<br>0 = MAX9860 is in full shutdown.<br>1 = MAX9860 is powered on.<br><br>When $\overline{SHDN}$ = 0. All register settings are preserved and the I²C interface remains active. |
| DACEN | **DAC Enable**<br>0 = DAC disabled.<br>1 = DAC enabled. |
| ADCLEN/ADCREN | **ADC Left/Right Enable**<br>0 = Left/right ADC disabled.<br>1 = Left/right ADC enabled.<br><br>The left ADC must be enabled when using the right ADC. |

### Revision Code

The MAX9860 includes a revision code to allow easy identification of the device revision. The current revision code is 0x40.

## Table 12. Revision Code Register

| ADDR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 0xFF | REV | | | | | | | |

### I²C Serial Interface

The MAX9860 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9860 and the master at clock rates up to 400kHz. Figure 6 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX9860 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9860 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9860 transmits the proper slave address followed by a series of nine SCL pulses. The MAX9860 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9860 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

*SMBus is a trademark of Intel Corp.*

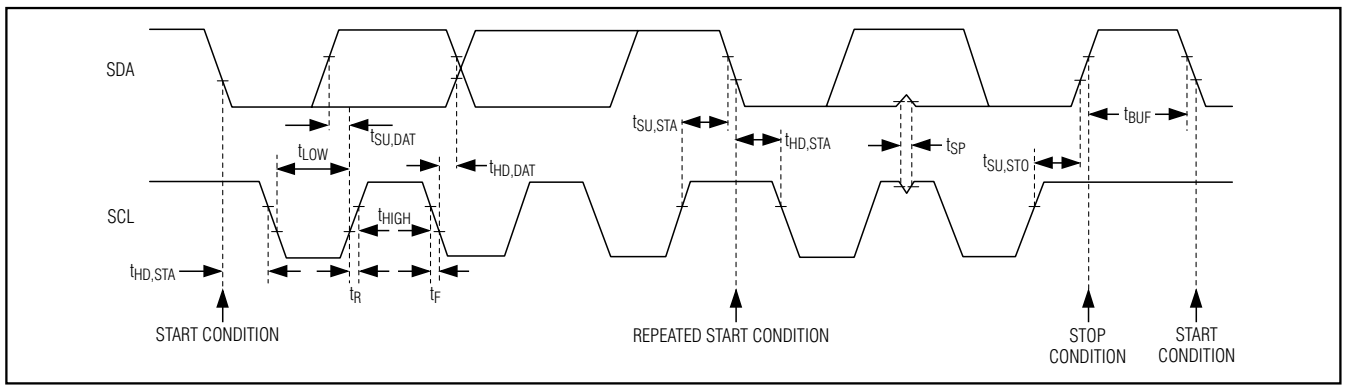



*Figure 6. 2-Wire Interface Timing Diagram*

### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

### START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low-to-high transition on SDA while SCL is high (Figure 7). A START condition from the master signals the beginning of a transmission to the MAX9860. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

### Early STOP Conditions

The MAX9860 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

### Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX9860, the seven most significant bits are 0010000. Setting the read/write bit to 1 (slave address = 0x21) configures the MAX9860 for read mode. Setting the read/write bit to 0 (slave address = 0x20) configures the MAX9860 for write mode. The address is the first byte of information sent to the MAX9860 after the START condition.

### Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9860 uses to handshake receipt each byte of data when in write mode (see Figure 8). The MAX9860 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX9860 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9860, followed by a STOP condition.

### Write Data Format

A write to the MAX9860 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 9 illustrates the proper frame format for writing one byte of data to the MAX9860. Figure 10 illustrates the frame format for writing n bytes of data to the MAX9860.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9860. The MAX9860 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX9860's internal register address pointer. The pointer tells the MAX9860 where to write the next byte of data. An acknowledge pulse is sent by the MAX9860 upon receipt of the address pointer data.

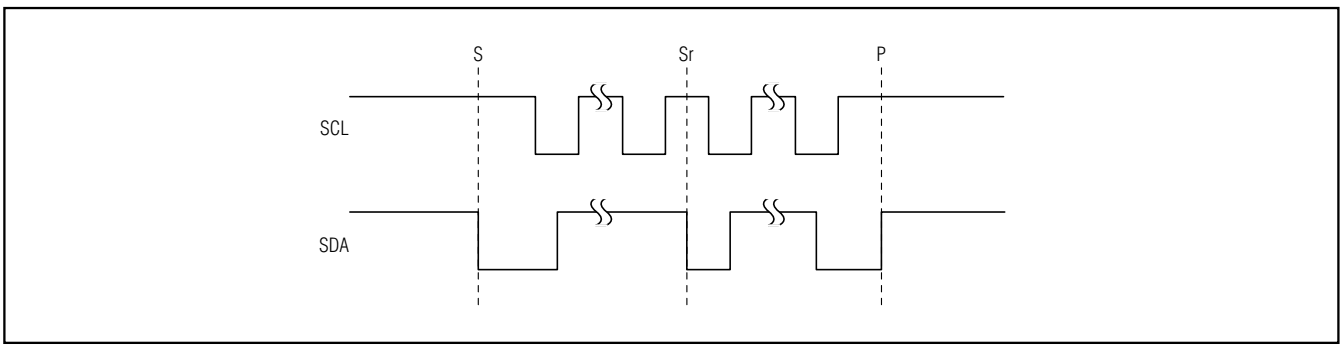



*Figure 7. START (S), STOP (P), and REPEATED START (Sr) Conditions*

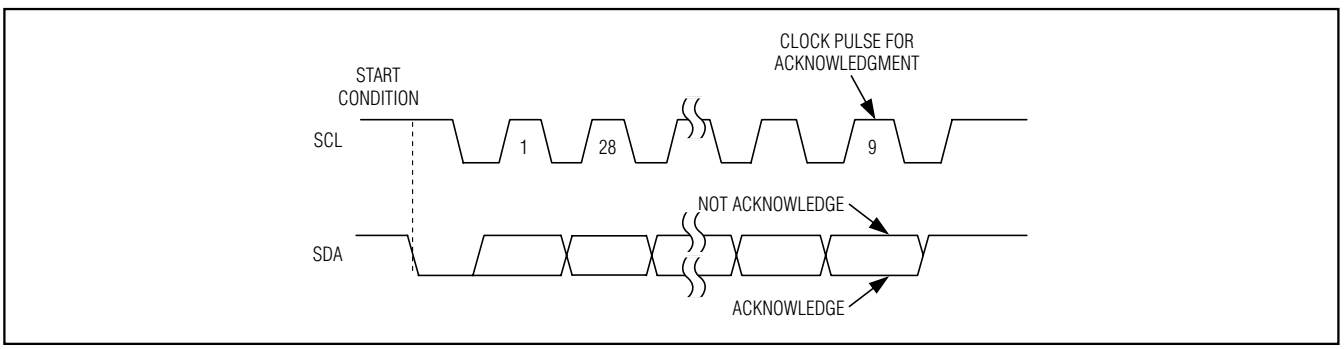



*Figure 8. Acknowledge*

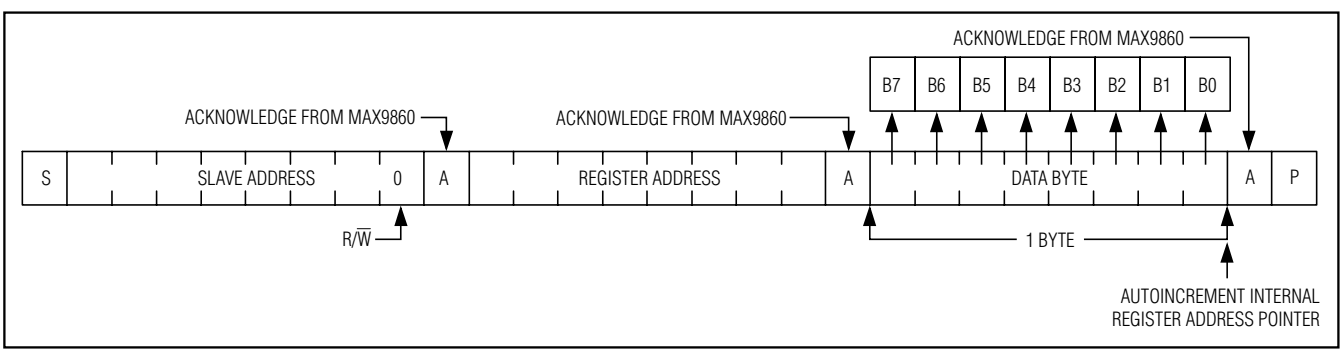



*Figure 9. Writing One Byte of Data to the MAX9860*

The third byte sent to the MAX9860 contains the data that is written to the chosen register. An acknowledge pulse from the MAX9860 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Figure 10 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0x10 are reserved. Do not write to these addresses.

### *Read Data Format*

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX9860 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX9860 is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement

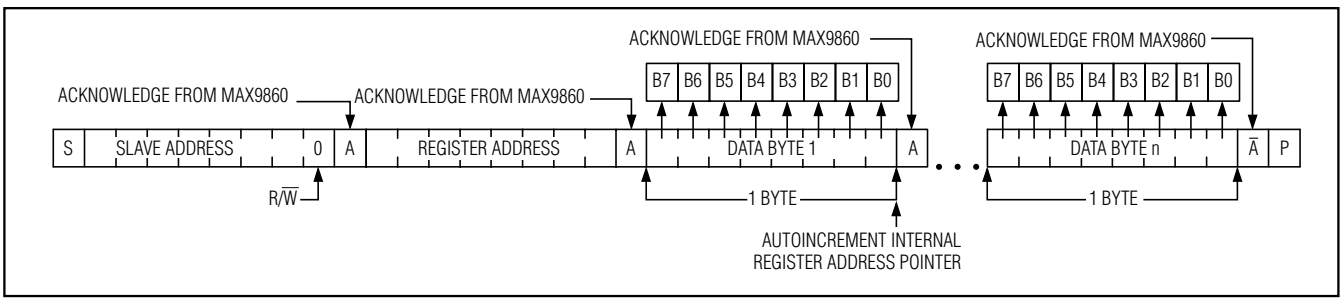



*Figure 10. Writing N Bytes of Data to the MAX9860*

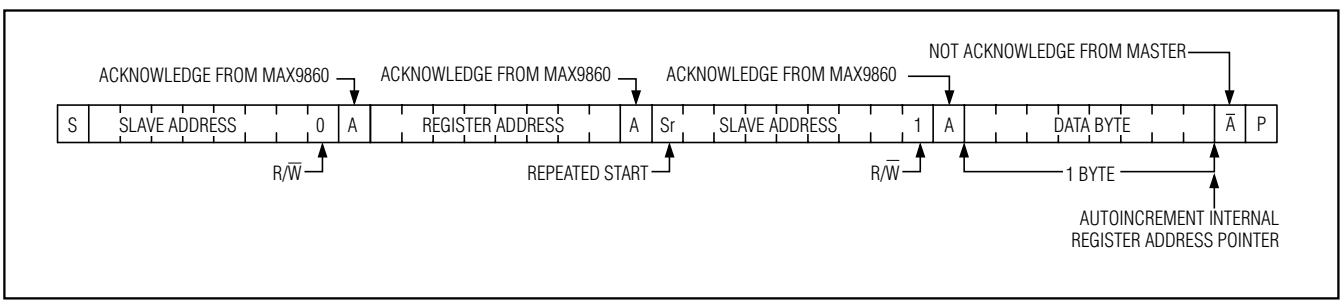



*Figure 11. Reading One Byte of Data from the MAX9860*

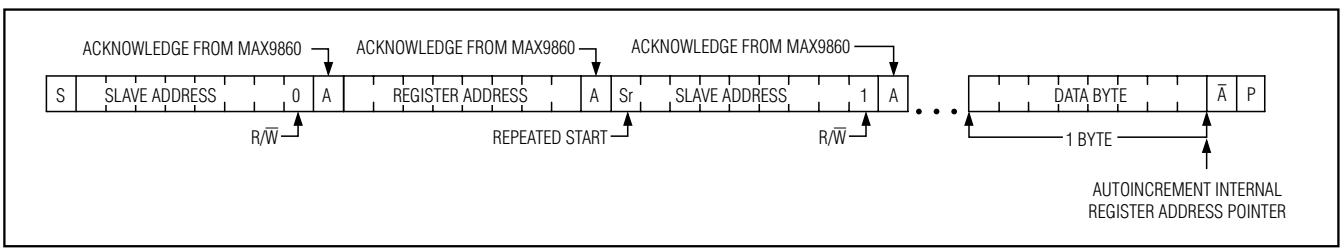


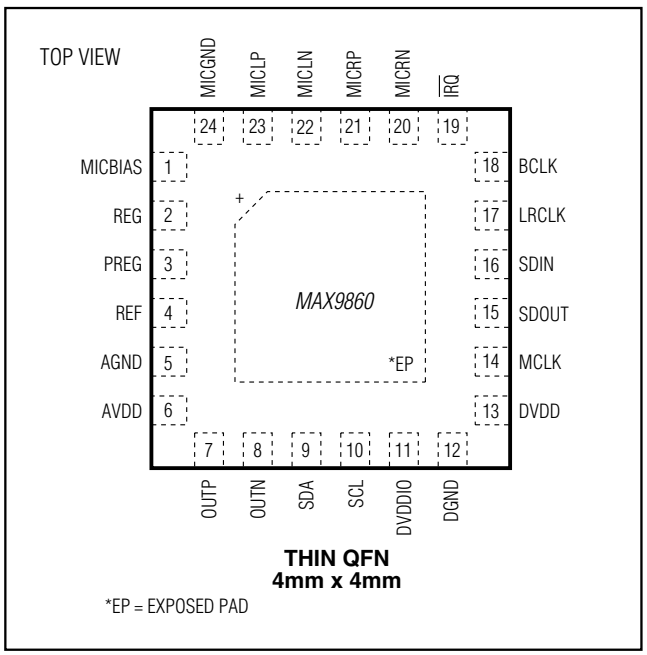

*Figure 12. Reading N Bytes of Data from the MAX9860*

feature allows all registers to be read sequentially within one continuous frame. A STOP (P) condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX9860's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START (Sr) condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9860 then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 11 illustrates the frame format for reading one byte from the MAX9860. Figure 12 illustrates the frame format for reading multiple bytes from the MAX9860.

## Pin Configuration




## Applications Information

Proper layout and grounding are essential for optimum performance. When designing a PCB for the MAX9860, partition the circuitry so that the analog sections of the MAX9860 are separated from the digital sections. This ensures that the analog audio traces do not need to be routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND, DGND, and MICGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signal.

Ground the bypass capacitors on REG, PREG, and REF directly to the ground plane with minimum trace length. Also be sure to minimize the path length to AGND and MICGND. Bypass AVDD directly to AGND. Bypass MICBIAS directly to MICGND.

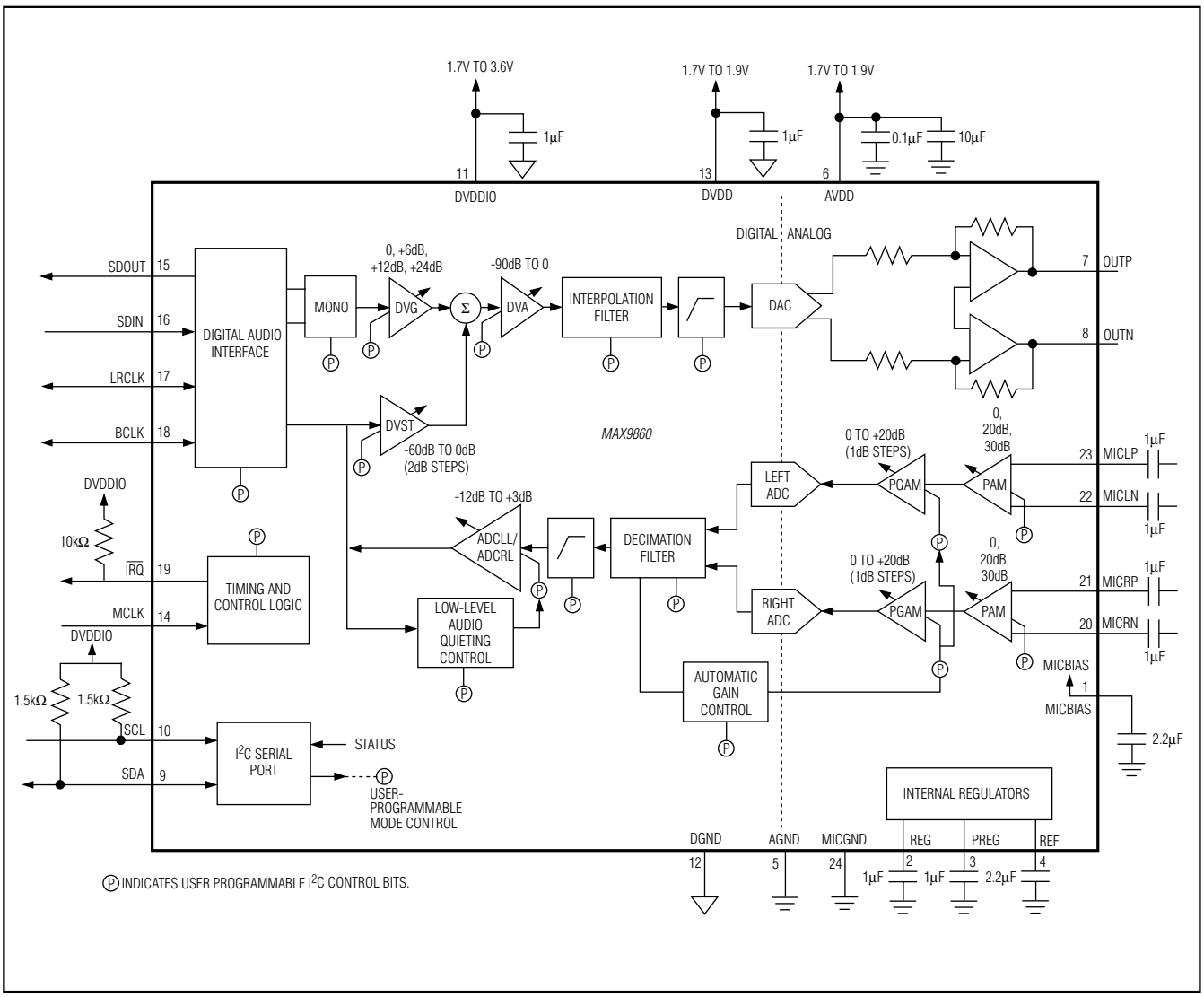
Connect all digital I/O termination to the ground plane with minimum path length to DGND. Bypass DVDD and DVDDIO directly to DGND.

Route microphone signals from the microphone to the MAX9860 as a differential pair, ensuring that the positive and negative signals follow the same path as closely as possible with equal trace length. When using single-ended microphones or other single-ended audio sources, AC ground the negative microphone input signal as near to the audio source as possible and then treat the positive and negative traces as differential pairs.

The MAX9860 thin QFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to AGND.

An evaluation kit (EV kit) is available to provide an example layout for the MAX9860. The EV kit allows quick setup of the MAX9860 and includes easy-to-use software allowing all internal registers to be controlled.

## Functional Diagram/Typical Operating Circuit




## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 24 TQFN-EP | T2444+4 | 21-0139 | 90-0022 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/08 | Initial release | — |
| 1 | 9/09 | Corrected error in Table 11 | 32 |
| 2 | 2/12 | Removed $V_{OS}$ typical spec and updated max spec | 5 |

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