Frequently Asked Questions

TLE4941/42 series

Version 1.1

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Document history:

Rev. 1.1: 26.03.01 TLE 4941-2 type added, minor changes in Q 35, repair of broken links

1. What is the difference between TLE4942 and TLE4942-2 type?

The TLE4942-2 shows output signal in the uncalibrated mode after signal start-up. Therefore the TLE4942-2 will give speed information much earlier (after 1st or 2nd magnetic edge). During uncalibrated mode the duty cycle and the phase shift of the output signal may vary.
The delay between the startup of the signal, the entering calibrated mode and the first calibrated output with correct direction information is the same for both TLE4942 and TLE4942-2.
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2. What is the typical behavior after supply line interruptions and undervoltages?

2.1 Static / quasistatic undervoltage:

Definition: The supply voltage is below 4,5V for a longer time period.
Depending on temperature and process variations the IC might work at voltages below 4,5 V.
For voltages around 2,6-2,7 V an internal undervoltage reset will be triggered. It will stop the IC signal output and trigger a new calibration. The output status after calibration is low.
At voltages below 4V the power supply consumption will virtually break down completely (see also typical diagram at Appendix A).
After re supply of voltage >4,5 V the IC will start up in calibration mode. After the type specific delay the IC will activate the output.

The following points comment typical behavior. Given numbers largely depend on temperature and process tolerances.

- The pulse length of the stop pulses may be shortened at undervoltage and output signal might decrease.
- Mainly the high current will get smaller for supply voltages lower 4,5 V. Low current will decrease less and at lower voltages as the high current.
- Undervoltage pulses may cause missing output pulses.
- The spec is not valid for voltages below 4,5 V. This voltage value has to be reached at the pins of the IC. The voltage drop at R_M is **not included** in the 4,5 V.

Please remember that the supply voltage might vary for high and low outputs due to different power consumption. Due to different voltage drops at high and low current at R_M the IC might toggle between reset and non-reset range if it is running below 4,5 V.

2.2 Dynamic undervoltage or supply line interruptions (micro breaks):

Definition: Dynamic undervoltages describe a reduction of voltage supply, which occurs only for a short time period.
The following examples show the relation between low supply voltage pulses, duration of drop and the internal supply voltage. The measurements have been done without a capacitor and without external load resistor at the IC. The capacitor would help to hold the supply voltage if microbreaks were to occur. The effect of capacitor depends on the application circuit typical voltage level and on the actual output state.
Measurement has been done at room temperature (25° C) with a ceramic type. The internal voltage for operation of IC is 3 V. Given numbers largely depend on temperature and process tolerances.

Examples:
A voltage drop from 12 V to 3 V, which occurs for 100 ns, should be uncritical for this IC.
A voltage drop from 12 V to 0 V, which occurs for 20 ns, should be uncritical for this IC
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3. What is the initial output state after power-up of IC without a magnetic input signal?

TLE4941 series: The output state is low (typical value: 7 mA).
TLE4942 series: the output is low (typical value: 7 mA). A pulse of about 1,44 ms (stop pulse) is triggered typically after 737ms. This pulse is generated every 737 ms.
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4. What is the initial output state after start of signal with a powered IC?

TLE4941: The output state is low (typical value: 7 mA). The input signal starts. Until the initial calibration is done (n_{start} = max. 6 magnetic edges for rare extra cases see application notes, Appendix B) the output is low. After this initial calibration the output starts to switch at the zero crossing of the differential magnetic input signal.

TLE4941-2: The output state is low (typical value: 7 mA). The input signal starts. At least after the 2nd edge the output starts to switch in uncalibrated mode. After the initial calibration (n_{start} = max. 6 magnetic edges for rare extra cases see application notes, Appendix B) the IC will change to calibrated mode. After this initial calibration the output will switch with the zero crossing of the differential magnetic input signal. A phase shift between uncalibrated and calibrated mode might occur.

TLE4942: the output is low (typical value: 7 mA) or a stop pulse is apparent. The input signal starts. Within the initial start up calibration phase (max. 6 pulses, for rare extra cases see application notes or Appendix B) the output state does not change. After this phase the output signal starts with its speed signal. The direction signal might give up to 3 spurious output pulses.

TLE4942-2: the output is low (typical value: 7 mA) or a stop pulse is apparent. The input signal starts. The uncalibrated mode is searching for extreme values (minimum or maximum values). The output signal (stop pulse or low signal) is cut off after an extreme is detected. Starting at a local extreme an in- or decrease of input signal larger than the digital noise constant of actual PGA stage is necessary to allow detection. In case of detection a speed pulse at the output with a 45 µs pre bit is generated. This pulse may have any length (45 -720 µs) and is followed or stopped by the next detected extreme. In uncalibrated mode the output switches after each detected extreme value.
After at least 6 magnetic edges the IC switches to calibrated mode (max. 6 pulses, for rare extra cases see application note Appendix B).
The direction signal might be spurious for 3 further output pulses after the IC has reached calibrated mode. When the IC is in calibrated mode the output starts to switch with the zero crossing of the differential magnetic input signal.
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5. What happens if the target wheel pitch is other than 5 mm?

You will get smaller amplitudes for speed and direction signal. A larger magnetic field or a smaller airgap should compensate the degradation of amplitudes.

Speed signal (TLE4941/42 series):

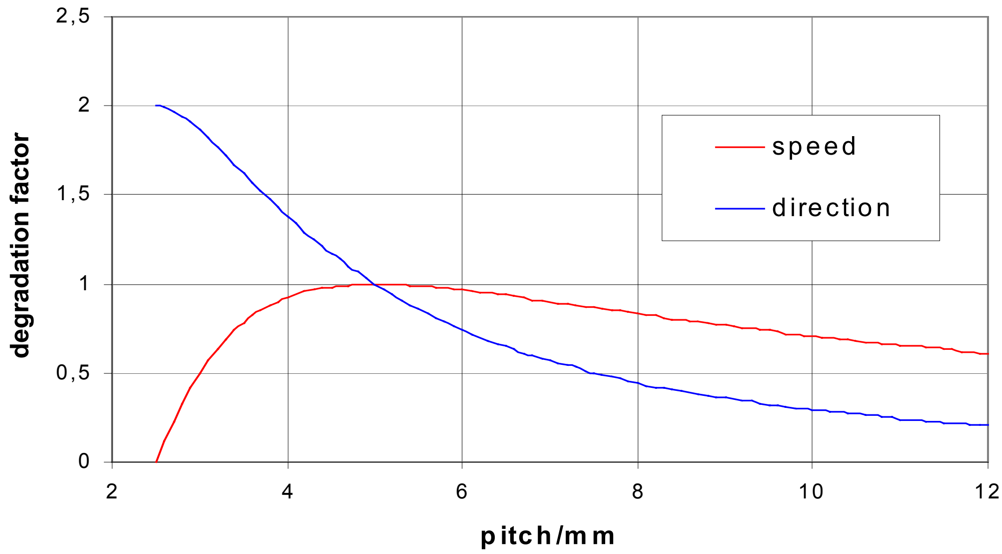
With pitches other than 5 mm you will get a different internal signal. Two main effects will occur. First effect is that there is systematic speed signal degradation due to the calculation method used for speed signal (see Figure 1). This curve shows the impact of pitch to the degradation factor (=maximum of internal speed signal amplitude at specific pitch/ maximum internal speed signal amplitude at 5 mm pitch). The factor decreases for variations in both directions of pitch.
The calculation of speed is done with signal from two Hall probes (A and C) spaced 2,5 mm. The phase shift (2p) is the distance in degrees between two target teeth (=pitch, p=90° for a 5 mm pitch).
$A = B_{Field} \sin(\varpi t)$ $C = B_{Field} \sin(\varpi t + 2p)$ $p = [((\text{distance A-C})/2)*360)]/\text{pitch} = [(2,5\ \text{mm}/2)*360°]/\text{pitch}$
Speed = A-C
$= B_{Field} * (\sin(\varpi t) - \sin(\varpi t+2p))$
$= -2 B_{Field} \cos(\varpi t+p) \sin(p) = -\Delta_{BField} \cos(\varpi t+p) \sin(p)$

So the maximum value of the speed signal is determined by B_{Field} 2*sin (p).
Thermal noise of the signal has to be taken into account.
Small pitches will produce a very homogeneous magnetic field in the airgap. This additionally will decrease the speed signal due to homogenizing effect.
Larger pitch will result in a decreased signal to noise ratio. This will lead to larger jitter.

Direction signal (only TLE4942 and TLE4942-2):

The direction signal is calculated by the signals from the three Hall probes (A, B and C) spaced 1.25mm.
A= B_{Field} sin (ϖt) B= B_{Field} sin (ϖt + p) C= B_{Field} sin (ϖt + 2p) p = [((distance A-C)/2)*360)]/pitch = [(2,5 mm/2)*360°]/pitch
Direction = (A+C)/2-B
= 0,5*B_{Field} {[sin (ϖt) + sin (ϖt+2p)] – 2*sin (ϖt+p)}
= -B_{Field} (cos (p) – 1) sin (ϖt+p)
The maximum value of the direction signal is determined by B_{Field} (cos(p)-1).
The direction signal degradation in Fig. 1 is calculated by the direction signal amplitude at specific pitch divided by the direction signal amplitude at pitch 5.
For pitches larger than 5..6 mm the direction degradation becomes dominant. This might lead to a wrong direction signal before a warning bit (45µs) occurs.
For small pitches you will get a very homogeneous magnetic field in the airgap. This will decrease the direction signal additionally.

Fig. 1



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6. What is the output status of the TLE4941 if it has been operating within spec parameter and the signal (magnetic field) is suddenly clearly lower ΔB_{limit}?

The IC output holds his last regular status until it gets a sufficient higher differential magnetic input signal (>ΔB_{limit}).
See also questions 19-21 for signal levels close to ΔB_{limit}.
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7. How much magnetic bias field is allowed between the Hall probes.

The TLE4941/42 series do compensate such “offsets” with a specific offset calibration circuit.
The bias field difference between the Hall probes must be within the limits of the spec (+/-20 mT). For magnet circuit design see question 28.
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8. What should be considered for correct air gap warning bit detection?

Noise, electrical and input signal variances like dynamic air gap changes will lead to an increasing number of warning bit pulses (45 µs). So the magnetic threshold for warning bit detection is fuzzy due to noise. This might result in a mix of output signals (warning Bit or direction + speed information) when the signal is next to the warning bit threshold.
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9. What is a simple test to check the value of the magnetic field with a TLE4923?

The best circuit is just to supply the IC (TLE4923) with power (typ. 12 V pin 1 and 2) and measure with an oscilloscope between Pin 3 (C, this is for normal operation not the signal output) and 2 (gnd).
On these pins an output voltage is generated. This voltage is proportional to the differential magnetic field at the differential Hall sensor and is superposed by a bias DC voltage. This voltage might vary due to process variations and magnetic offset.
This DC voltage relates not to the bias magnetic field of the magnet due to the differential principle. The AC signal is related to the moving wheel (bypassing of tooth or magnets from polewheel = differential magnetic field).
Standard TLE4923 will show a Filter bias voltage around 2 V (DC signal) and a filter sensitivity 8.5 mV/mT (AC signal) (typical values for 25°C, Data Book 2000, p. 306). Both values depend on temperature (please check with diagrams on page 316) and do have a statistic distribution.
Use high ohm voltage probes (>/=10 MOhm) at the oscilloscope, guarded cables (BNC) with shortest possible length and a stabile power supply.

We do recommend an IC which has a known filter sensitivity at Pin 3 to get reasonable results.

A similar measurement is possible with the TLE4921-5U (different bias voltage and sensitivity, see question 34).

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10. Why is the EL Bit rejected above 117 Hz?

The EL Bit with direction right has the widest pulse length, typical value: 720 µs + 45 µs pre pulse (worst case: 828 + 52 µs). This pulse is generated twice per input pulse. So you need at least 1530 (1760) µs at the output for one input pulse on the assumption that the duty cycle is 50%. A speed frequency with 117 Hz would need a space of 8547µS. At higher frequencies there would not be enough space between edges to show full pulse length.
The EL Bit is used for test purposes within production. Usually these tests are done with low frequency because then they are less time and energy consuming.

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11. What is the use of the capacitor mentioned in the application circuit between V_{CC} and signal pin (TLE4941/42)

This capacitor is used to supply the sensor if microbreaks were (short loss of supply voltage) to occur. The maximum time span for microbreaks can be calculated with the recharge process from the capacitor. Important values are the supply voltage Uv, the allowed minimum supply voltage (Umin = 4,5 V) from the IC and the constant supply current of IC (I_{max} = 16,8 mA).
$I=C^*(dU/dt)$ $\Delta t = C^*\Delta U / I_{max} = C^*(Uv-U_{min}) / I_{max}$
Example:
Supply voltage U_v =12V, I_{max} = 16,8mA, C = 1,8nF, U_{min} = 4,5 V, T=20°C. The time span until the voltage reaches 4,5 V is around 1µs. The capacitance values may vary +-5% for TLE494x-C types (1,8 nF) and also might be influenced by temperature (see spec of capacitor).

Furthermore the capacitor helps to improve the EMI/EMC performance.

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12. Which type of capacitor should be used for TLE4941/42

No polarity capacitors should be used because of possibility of reversed polarity from voltage supply, which might destroy the capacitor.
The TLE494x-C types use a 1,8nF NPO-ceramic type capacitor. Temperature specification: COG/CG.

Datasheet is available under:

http://www.epcos.com/inf/20/10/db/cc_99/00150026.pdf

Epcos order number: B37940-J5182-J60

Only difference between the used type (J) and the data sheet type (K) is a different metallic contact area.

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13. What is the correlation of magnetic input orientation, chip-internal signals and output signal state for TLE4941 series.

The Hall probe next to the Vs pin is called "left", the Hall probe next to the signal (Gnd) pin is called "right". If a magnetic field is directed from the marked side of the IC (top) towards the unmarked side (bottom/back side) it is called "positive" (south pole on back side of IC).
If a positive field is applied to the left Hall probe and a negative field (or a weaker field than on the left Hall probe) is applied to the right Hall probe, the resulting output current state is "high".
Electrically the analog signal path is laid out differentially. Therefore from the Hall probes to the comparator the signal swing is symmetrical. A "high" output of the comparator is running through some latch and multiplexer (e.g. of the test interface) and results in a "high" current at the output.

The TLE4942 series will operate with positive or negative orientation of magnetic field.

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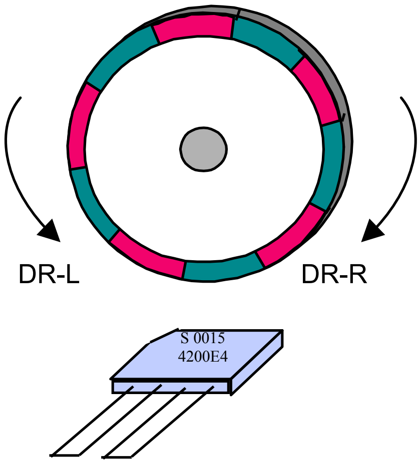
14. What is the connection between the magnetic field and the direction information for the TLE4942 series?

The IC is observed from above onto the marked side of the chip. The observer is in front of the IC and the pins point to the viewer. The left pin is the VCC pin and is called "left". The magnetic field is applied (does not depend on magnetic orientation) to the IC. The result would be the direction information "left" if the magnetic field moves from the VCC pin (left pin) to the GND Pin (right pin).



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15. What effects influence the duty cycle?

__Influence:__

Bad signal offset: Shortly after start up, after fast magnetic amplitude changes (magnetic circuit problems, target wheel wobbles), or after fast change of rotation direction.
Inhomogenious magnetic field: In the case of a non-ideal magnetic field (bad target wheel, missing or bad shaped tooth, unmatching pitch) a poorer duty cycle can be obtained.

__No influence:__

Jitter: has a similar effect to the output but is specified separately
High Temperature: This will increase noise and the zero detection of this signal will be influenced. This will mainly influence the jitter.

All duty cycle tests for spec are done with 2mT differential field, 25° C ambient temperature, 5 mm pitch and a sinusoidal magnetic field.
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16. What influences the output signal jitter?

The maximum jitter (1 sigma value) is +-2% for a signal frequency below 2500 Hz. This value has to be added to the 45...55% duty cycle if only a small number of pulses are evaluated.
The maximum deviation from ideal switching points is calculated by:
Duty cycle error + jitter error + propagation delay time
Usual applications use an average value from the output signal. For a large amount of data points the jitter effect is reduced due to averaging.

The jitter will increase when:

- The input signal is decreasing (pitch, field, air gap)
- The EMV/EMI noise increases
- The temperature increases (thermal noise)
- Dynamic mechanical stress occurs

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17. What would happen if the magnetic signal frequency were above 2500 Hz?

Following information is calculated with a duty cycle of 50%. Duty cycles other than 50% will reduce the shown values of frequencies

TLE4942: Above 2220 Hz (typical value, minimum value 1930 Hz) signal frequency the output pulses (strongest influenced DR-R) will be cut off. The two direction signals (DR-L, DR-R) will have same length around 3,7 kHz. Sensitivity will decrease slightly due to internal low pass noise filter (magnetic thresholds increase).

TLE4941: At signal frequencies slightly above 2500 Hz sensitivity will decrease due to internal low pass noise filter (magnetic thresholds increase).

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18. What would happen if the integrated Hall probes of the TLE4941/42 were to a different distance to the magnet (IC tilt)?

This IC tilt results in different magnetic signal amplitude at the two Hall probes and therefore in an offset at the probe which is next to the tooth or pole wheel. The difference of these signals is used for the speed signal detection. This signal will be unsymmetrical.

The unsymmetrical amplitude will lead to a shift of zero crossings of the signal. The zero crossings are used to switch the output and therefore the shift of zero crossings will lead to an imperfect duty cycle. The offset calibration algorithm compensates this behavior after a few pulses.

The direction detection also depends on the zero crossing and therefore on the duty cycle. A bad duty cycle causes imperfect digitizing and might lead to a wrong direction information.

So a proper (normal to the field) mounting of Hall IC's is important to obtain good results and the bias field difference between the Hall probes must be within the limits of the spec (+/-20 mT). The maximum back bias field at all probes must be below 500 mT.

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19. What happens to the output signal of the TLE4941 when the input signal stops at a differential signal maximum?

The input signal stops at a signal maximum and stays at this level. That means one tooth was stopped directly above the Hall probe next to VCC pin and the magnetic field has a positive orientation. The other Hall probe is directly above the gap between the teeth.
The output of the TLE4941 will be in high status.
The input signal will stay at this level. No further extremes will be detected, therefore no offset correction is possible. No zero crossings are detected the output will stay in this last status. At least 737 ms after the stop of the signal a recalibration is done. The TLE4941 will hold the last status. The magnetic input noise (mechanic vibrations of target wheel) has to be significantly smaller than ΔB_{limit} to avoid further switching.

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20. What happens to the output signal of the TLE4941 if it is in status high and the input signal stops close to the zero crossing and stays there?

If the input signal stops close before a zero crossing, noise may trigger a single switching event. This might happen any time after the stop of signal until a recalibration is done.
The magnetic input noise (mechanic vibrations of target wheel) has to be significantly smaller than ΔB_{limit} to avoid further switching. At least 737 ms after the stop of the signal a recalibration is done. The TLE4941 will hold this last status.

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21. What happens to the output signal of the TLE4942 series if the input signal stops at a specific level and stays there?

If the input signal stops at a level close to the zero crossing of the input signal, due to noise effects one further output pulse may occur due to zero crossing. This might happen any time after the stop of signal and the pulse may have any length. After t_{stop} the stop pulse is generated and no further switching due to noise is possible if the magnetic input noise (mechanic vibrations of target wheel) is significantly smaller than ΔB_{limit}.
For all other levels the TLE4942 will complete the last pulse or it will already be in the low level after the stop of the signal. No further extremes and no zero crossings will be detected. After t_{Stop} the IC will do a self-calibration and the output will show the stop pulse typically every 737 ms.
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22. What are the main advantages of the TLE494x series

Two wire current interfaces
No filter capacitor as used in TLE4921 and TLE4923 series
Offset calibration algorithm
Direction information (TLE4942)
Assembly position information (EL Bit, TLE4942) for testing
Air gap warning bit (LR warning Bit, TLE4942)
Stop information
Flexibility in magnetic circuit design
Smaller packages
Fast start up time
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23. What are the main differences between TLE4941 and TLE4942

The TLE4942 provides direction, assembly position and an airgap information.
The output signals are different. The TLE4941 changes output state (high or low) at zero crossing of input signal. The TLE4942 provides a direction and speed dependent output pulse for every zero crossing. The same input signal will provide twice as many output pulses when using the TLE4942.
This also results in a different definition of the duty cycle.
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24. Which influence has the value of the resistor R_M in the application circuit

The value of R_M depends on the application.
The value of R_M has an influence on:

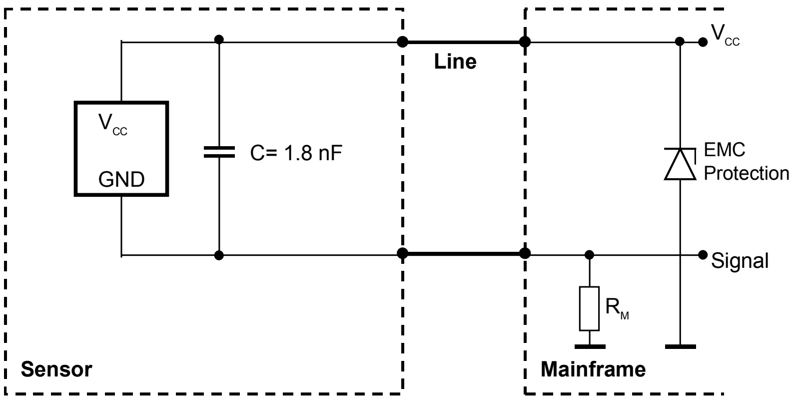
Slew rate: With an increasing value of R_M the slew rate will decrease.

Output voltage: With an increasing value of R_M the output voltage at signal pin will increase. This increases the signal to noise ratio (not valid for current induced noise).

Current limitation: If the supply voltage has wrong polarity the R_M has to limit the current (<200 mA). For a 12 V supply the resistor has to be larger 60 Ohm (see also Q 26).

Supply voltage: A very important point is to maintain the V_{CC} voltage. This voltage must be above 4.5 V. A large resistor might reduce the voltage at the IC below the 4,5 V.

Example: For R_M = 115 Ohm and the worst case high current I_{High} (16,8 mA) the supply voltage of the circuit has to be at least V_{CCmin} = 6,432 V (V_{Ccmin} = 4,5 V + 115 Ohm* 0,0168mA= 6,43 V).



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25. How large is the propagation delay time t_d?

The propagation delay time is defined as the time between a zero crossing of the magnetic input signal and the rising edge of the signal current (50% I_{high}). The typical value is t_d = 5-8 µs (See also typical diagrams in spec).
For the TLE4942 series the time between a zero crossing of the magnetic input signal and the rising edge of the signal current (50% I_{high}) is the propagation delay time + the pre low bit time. The typical value is $t = t_d + t_{pre\text{-}low}$ = 5-10 µs + 38-52 µs = 43 - 62 µs.
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26. What happens if the supply voltage has wrong polarity?

A reverse current larger I_{high} (typ. 14 mA) will flow. The resistor R_M limits the reverse current I_{rev} through the sensor. For a safe operation the I_{rev} has to be <200 mA (duration <4h).
Example: For a typical value of R_M = 75 Ohm and a reverse supply voltage of 12 V the reverse current will be limited to 160 mA. If the sensor is connected directly (without current limitation) the maximum allowed reverse polarity voltage is 0,3 V at ambient temperature (<80°).

Note: Generally the TLE4941/42 series has no internal protection against wrong polarity supply voltage. Protection has to be done externally (with value of R_M and if possible diodes).

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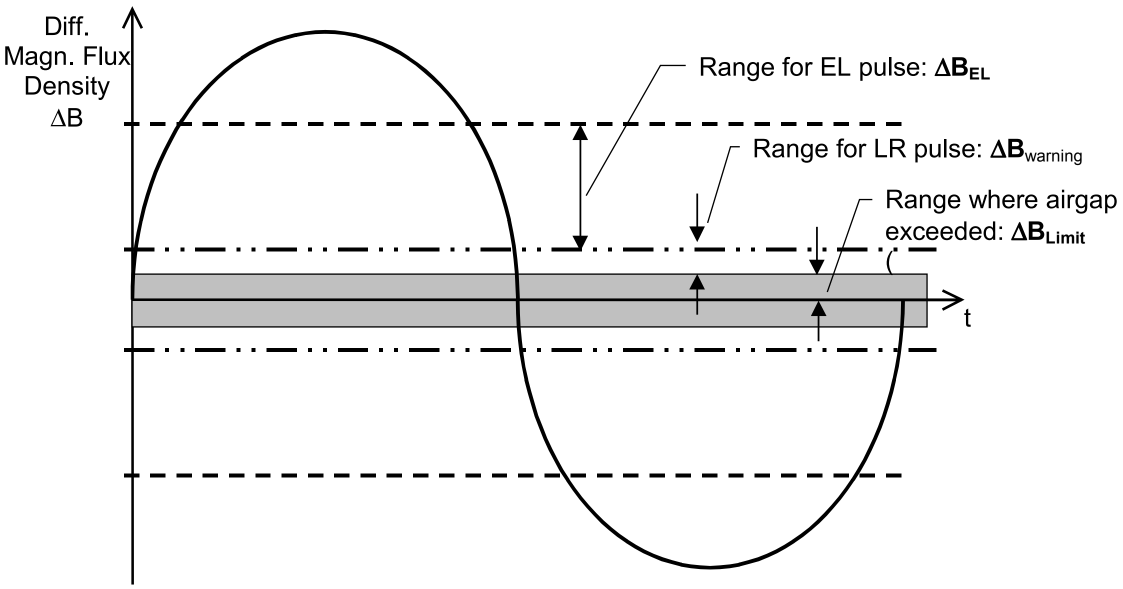
27. What is the use of the assembly bit (EL)?

The assembly bit (EL) is set when the magnetic field does not reach a defined value. As the TLE4942 series uses a pulse width modulated output, the EL information has a specific pulse length (360/720 µs).
The EL Bit can be used to confirm the correct mounting of sensor and magnetic circuit. This test can be done in production line applying a low frequency speed signal. The EL bit is only shown at signal frequencies smaller 117 Hz. The EL Bit occurs when the differential magnetic input signal is smaller as the EL threshold.



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28. Does the value of the differential magnetic field have influence on the jitter?

Yes, the jitter will decrease with an increasing magnetic field. So the jitter is equivalent to the signal to noise ratio.
Example from a TLE4941:
The measurement results show that at a magnetic field of 10mT the jitter is about a factor of 5 times smaller than at 2mT. The same results are with 10mT to 1mT (app. 10 times) and so on.

TLE4941	f_{signal} [Hz[	ΔB [mT]	Jitter Abs.	Jitter [%]
	1000	1,1	6,3 us	0,63%
		1,96	3,6 us	0,36%
		12,43	0,6 us	0,06%

The presented values may vary due to process variations for different lots.
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29. What are the main noise sources within TLE4941/42 series.

The Hall probes and the first amplifier stage produce the most significant noise. The noise depends highly on temperature (thermal noise).
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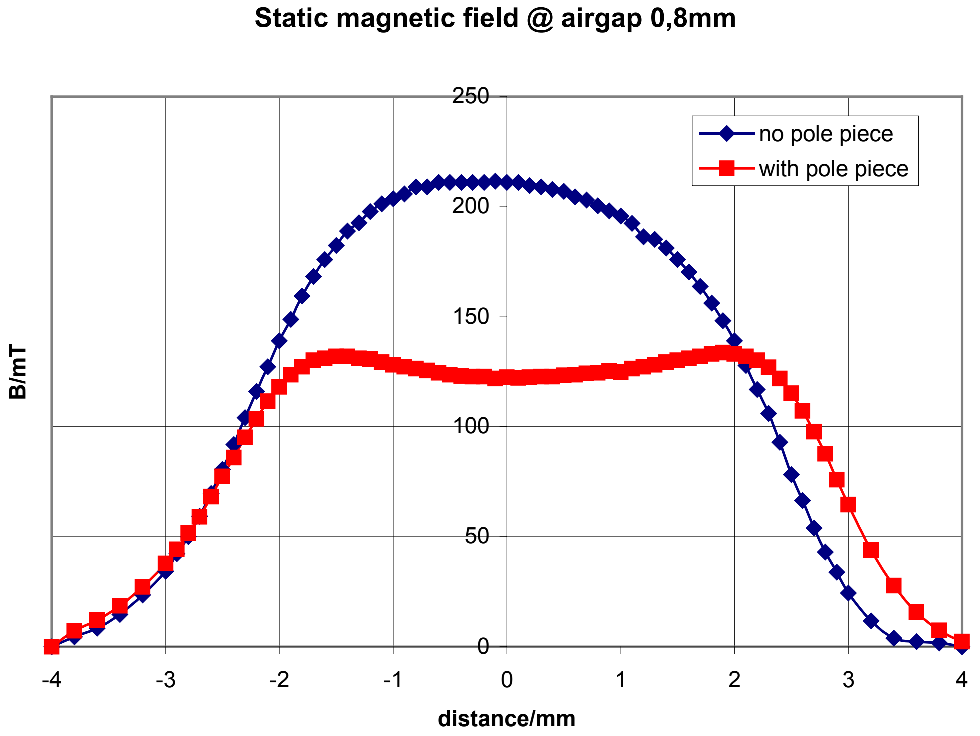
30. What is important for the back bias magnet design?

The chosen magnet needs to have a bias field differential between mean value of outer Hall probes and central Hall probe below +/-20 mT. Same maximum value is allowed between the outer Hall probes. In first evaluation check the magnetic field at a distance +/-1,25 mm from the central Hall probe (= distance between Hall probes). If the magnetic field is critical, a pole piece should be used to get a magnetic back bias field which is within above spec parameter. A second solution would be to use a broader magnet. The positioning process tolerances have to the taken in account. A bad situated magnet or pole piece will influence the shape of the bias field. Always check the differential magnetic field by using a TLE4921, TLE4923 or with a Gauss meter. The figure below shows a back bias field of a typical magnet with and without pole piece:



The values for this example without pole piece are at the distance=0, B=211 mT, distance=+1,25mm, B= 185 mT and distance=-1,25mm, B=192 mT. Therefore the bias field between mean of outer probes and central Hall probe is 22,5 mT, and the difference between outer probes is 7 mT. This magnet would not fulfil the specification values.

The values for this example with pole piece are at the distance=0, B=122mT, distance=+1,25mm, B= 128 mT and distance=-1,25mm, B=131 mT. Therefore the bias field between means of outer probes and the central Hall probe is 7,5 mT, and the difference between outer probes is 3 mT. This magnet would fulfil the specification values.

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31. Which general information can be given about the bending of IC pins?

The bending line of the pins should be in line with the holes in the pins.
The pins have to be fixed between bending line (hole) and IC to minimize the stress onto chip.
No torsion moment to the IC package is allowed.
Theoretically any angle is possible.
The pin material is Wieland K62 (CuSn1CrNiTi) and is covered with $SnPb_{8020}$.

Bending of the leads is the responsibility of the customer. Infineon does not take warranty for this process.
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32. Which general information can be given about the molding process?

Different applications showed that an overmolding is possible with a temperature up to 305°C and a pressure up to 300 bar. The pins of the IC are covered with tin. So with higher temperatures the tin may melt and may cause problems (short circuit at the package). The molding process should not raise mechanical stress normal to the Hall probes. So it is necessary to develop a molding tool which can cope with these demands.
Overmolding is the responsibility of the customer. Infineon does not take warranty for this process.
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33. Which general information can be given about the connection process between pins and wires?

No mechanical stress should occur to the IC pins during welding or soldering. Thermal processes should happen at the same time on both IC pins. The pin material is Wieland K62 (CuSn1CrNiTi) and is covered with $SnPb_{8020}$.
Used technologies could be soldering, welding, resistance laser welding and laser soldering.
Connecting wires is the responsibility of the customer. Infineon does not take warranty for this process.
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34. What is a simple test to check the value of the magnetic field with TLE4921-5U?

The best circuit is just to supply the IC (TLE4921-5U) with power (typ. 12 V pin 1 and 3) and measure with an oscilloscope between Pin 4 (C, this is for normal operation not the signal output) and 3 (gnd). No external capacitor is connected.
On these pins an output voltage is generated. This voltage is proportional to the differential magnetic field at the differential Hall sensor and is superposed by a bias DC voltage. This voltage might vary due to process variations and magnetic offset.
This DC voltage relates not to the bias magnetic field of the magnet due to the differential principle. The AC signal is related to the moving wheel (bypassing of tooth or magnets from polewheel = differential magnetic field).
Standard TLE 4921-5U will show a Filter bias voltage around 1,6 V (DC signal) and a filter sensitivity -4 mV/mT (AC signal) (typical values for 25°C, Data Book 2000, p. 288).

Both values depend on temperature (please check with diagrams on page 299) and do have a statistic distribution.
Use high ohm voltage probes (>/=10 MOhm) at the oscilloscope, guarded cables (BNC) with shortest possible length and a stabile power supply.
We do recommend an IC which has a known filter sensitivity at Pin 3 to get reasonable results.
A similar measurement is possible with the TLE4923 (different bias voltage and sensitivity see question 9).

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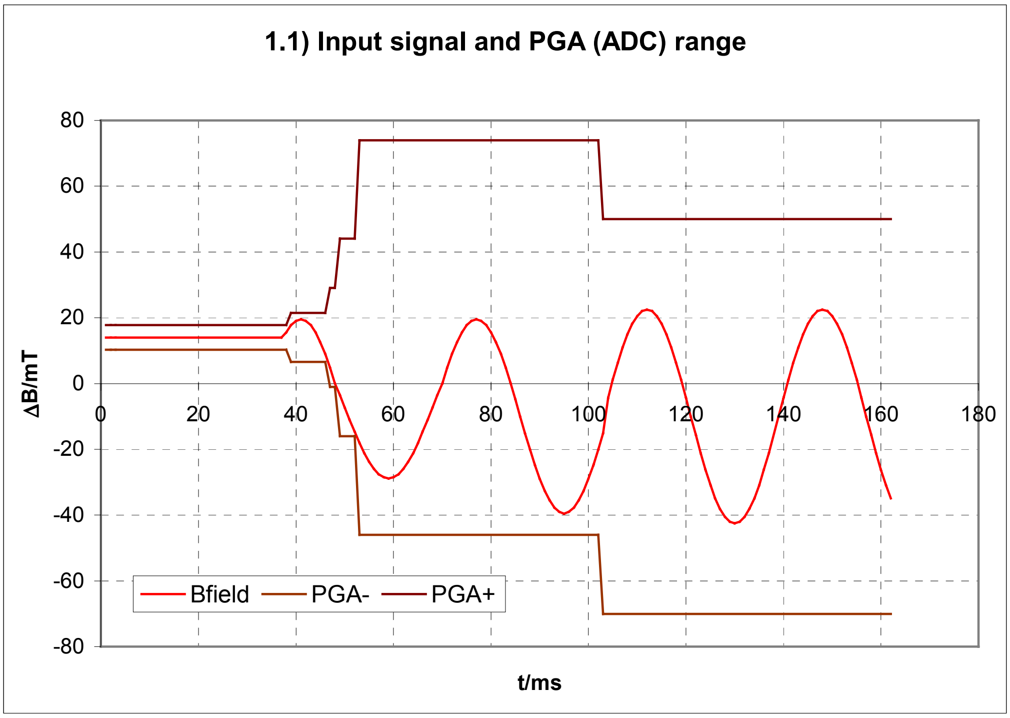
35. What might happen if the magnetic input signal amplitude is changing during uncalibrated and an additional PGA switching is necessary?

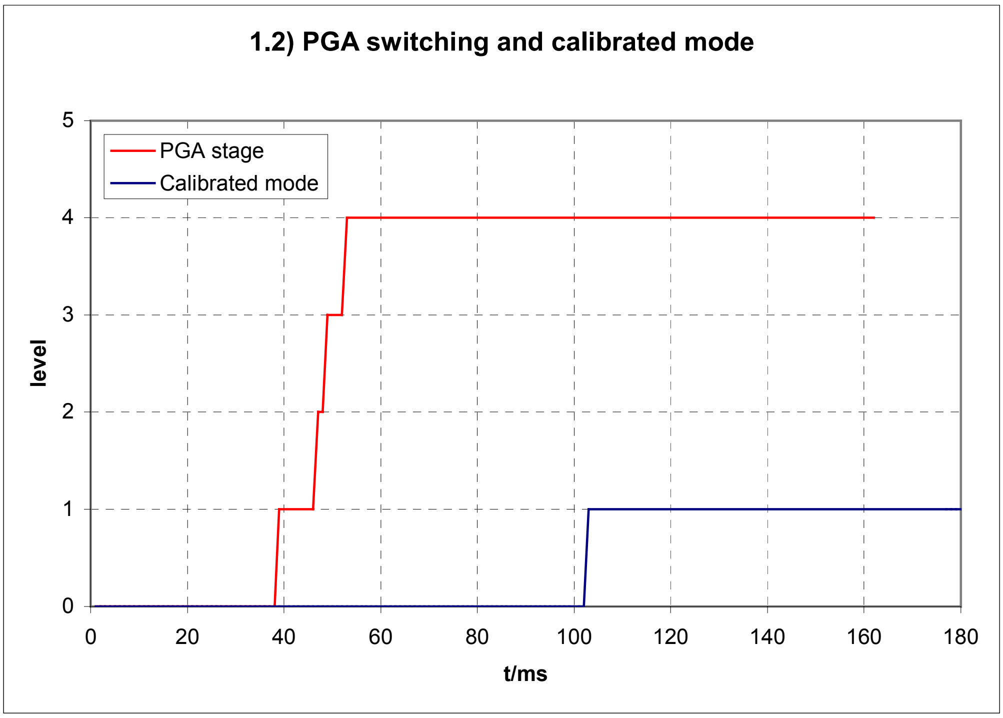
Usually all PGA (programmable gain amplifier) switching into the correct gain happens within less than one signal period after start-up of the signal. This time is included in the calculation for n_{start}. In case that the signal amplitude is close to the full range of the PGA or the following ADC (analog to digital converter) respectively, a slight change of the signal amplitude can cause one further switching event. This can be caused either by non-perfect magnetic signal (amplitude modulation due to polewheel or tooth wheel) or chip-internal noise.

TLE4941/42: The additional PGA switching can result in a further delay of the signal output (speed & direction) up to three magnetic edges.
TLE4942 –2: Signal output still starts with the 2nd edge latest. The additional PGA switching can result in a delayed transition to calibrated mode. Therefore the correct direction information can be delayed for two edges. (11 edges/output pulses instead of 9 edges at worst case a typical value for correct direction information is 5 edges).

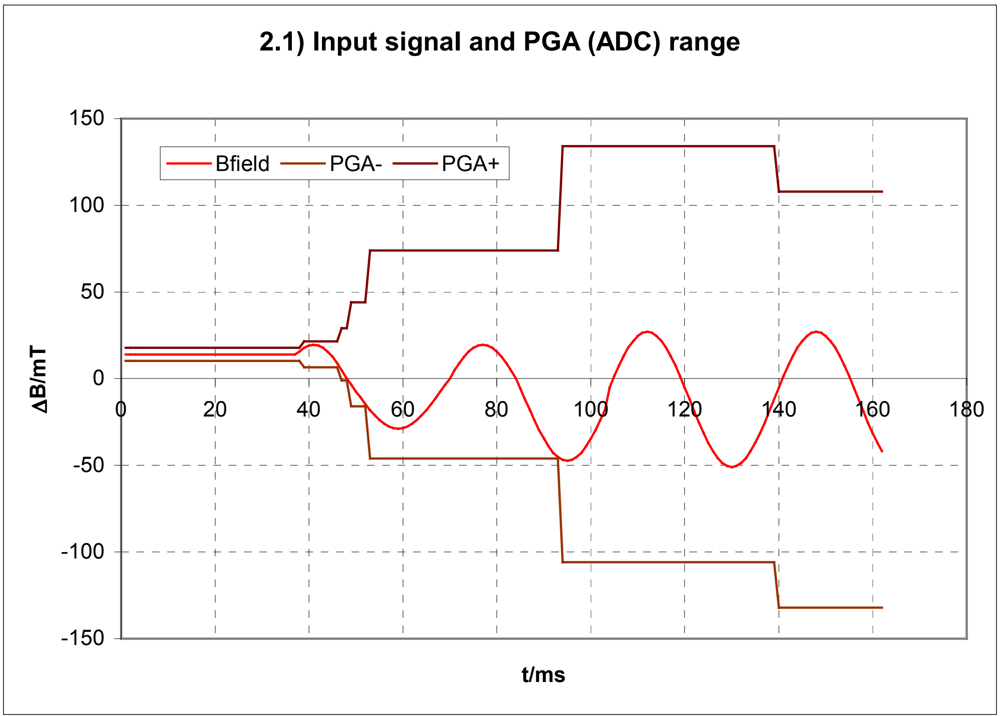
A start up time to calibrated mode of more than 6 edges happens with a very small probability (never seen in the lab, but can happen obviously). As above mentioned a change of input signal is the cause of this behavior (amplitude modulation, temperature changes, noise,..). A magnetic operating point that is clearly away from a PGA threshold could reduce the probability of occurrence. Due to process variation (+/- 30%) of the PGA thresholds the internal electrical operating point of the sensor is not exactly predictable. Furthermore mechanical and magnet tolerances have to be taken into account. So it is not possible for the application designer to choose a specific operating point.

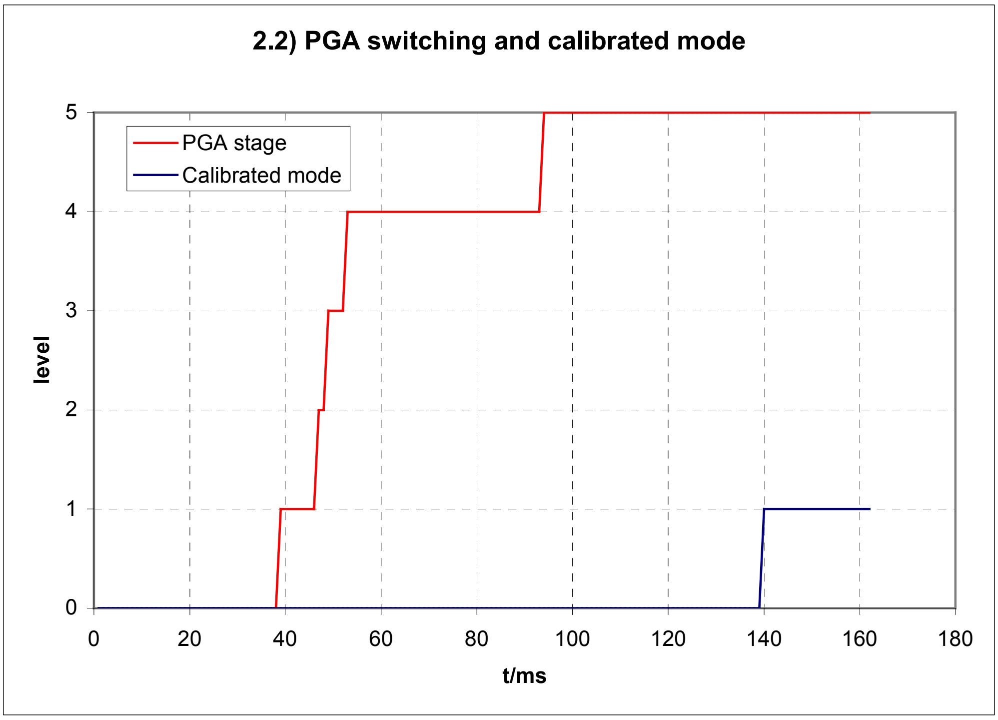
Examples:
1: IC Start-up where the PGA is switching early.





2: 2: IC Start-up where the PGA is switching late due to an increase of differential magnetic amplitude





Description:
The ΔB_{field} curve (Fig. 1.1 and 2.1) shows the differential magnetic signal in front of the offset compensation point. The relative ranges of the PGA stages are shown in curve PGA_+ and PGA_-. The PGA stages are changed if the input signal is larger than the current ADC/PGA range. The Figures 1.2 and 2.2 contain the current PGA stage number (0-6) and the time when the IC is switching to calibrated mode.

The internal measurement circuit centers the first signal within the ADC range. The PGA is in stage zero (most sensitive stage - for smallest signal).
The differential magnetic input signal (ΔB_{field}) is sinusoidal, has a negative offset and starts up with a 55° phase shift.
The input signal increases above the current ADC/PGA range. This switches the PGA to the next stage (stage 1). Then the signal decreases and over-ranges the negative edge from stage 1 after a while. The PGA switches again. This process happens again until a suitable PGA stage (example stage 4) is reached. The IC will switch to calibrated mode if extremes have been found and after a PGA stage and signal depending delay time.
In this examples the minimum at 60ms is not valid for offset calibration because the PGA switching has happened next to the minimum (distance less than the digital noise constant).

At example 1 the IC finds the necessary extremes for the offset correction (maximum at 75 ms, minimum at 95 ms). After a small delay the IC switches to calibrated mode (103 ms).

At example 2 the IC is searching for extremes to do the offset correction. The maximum at 75 ms is found. Then the input signal increases above the PGA range 4 shortly before the minimum at 95 ms is reached. This PGA switching to stage 5 deletes all old extremes and switching to calibrated mode is not allowed. The search for extremes starts again. The minimum at 95ms is not a valid minimum (switching next to the minimum).
New extremes are found after 112 and 130 ms. After the above mentioned delay the IC switches to calibrated mode at 140 ms. In this example the calibrated mode is activated with the 7^{th} magnetic edge.

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