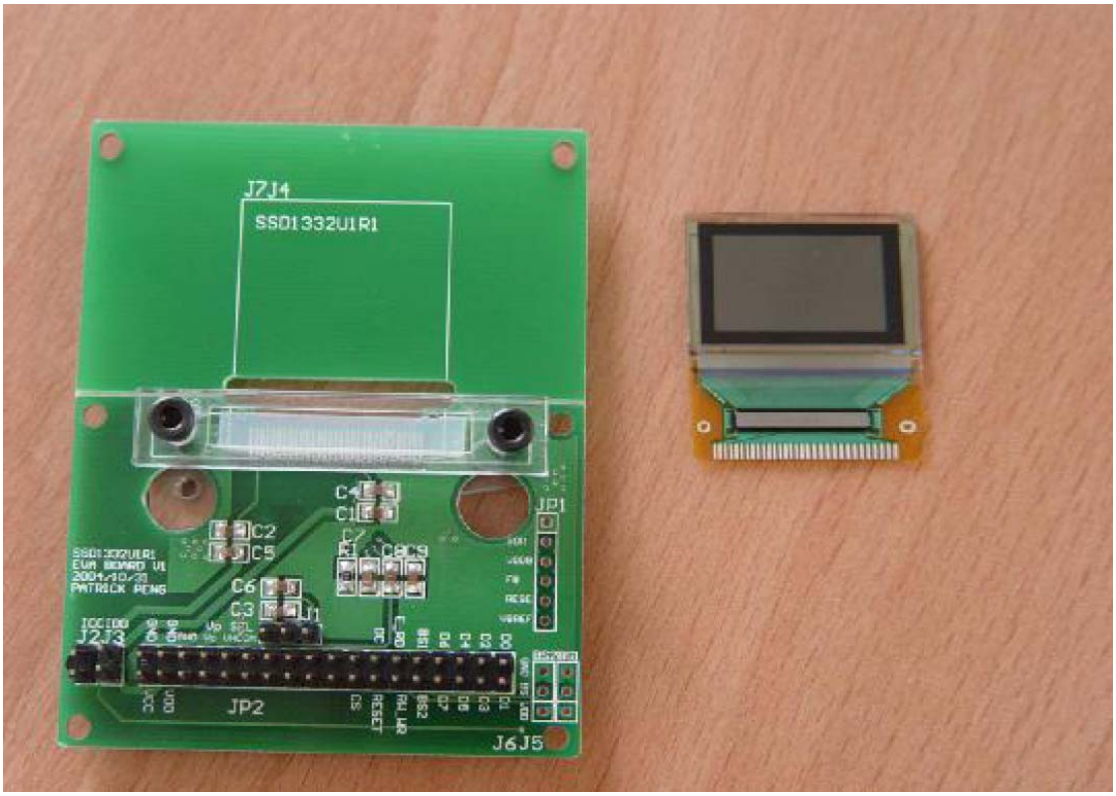
OLED DISPLAY MODULE

Application Notes

PRODUCT NUMBER	DD-9664FC-1B with EVK board



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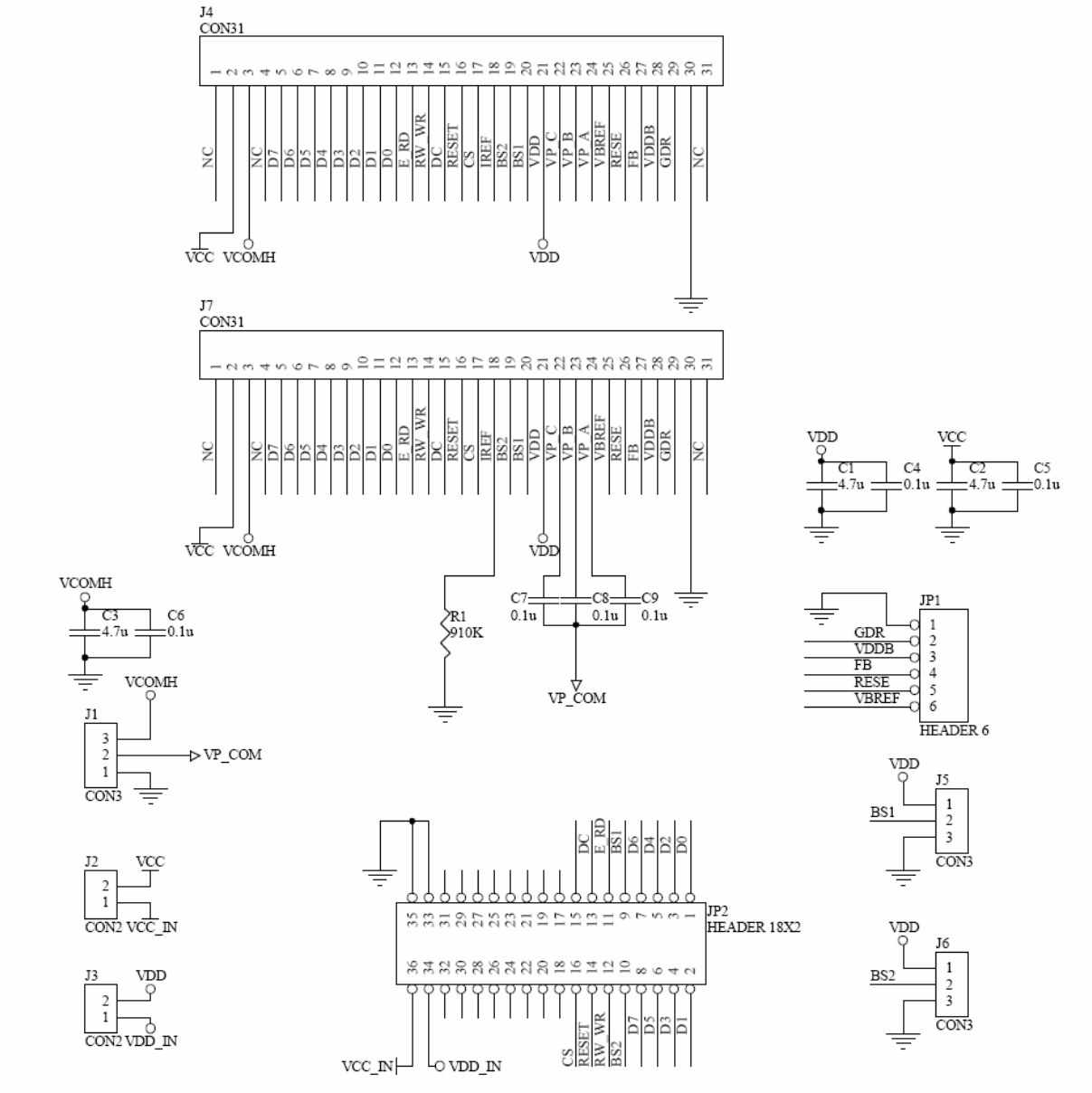
REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	06-Jul-06			First Issue	

1 EVK Schematic



2 Symbol Definition

D0-D7：These pins are 8-bit bi-directional data bus to be connected to the MCU's data bus.

BS1, BS2：These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table. User can fix these pins by jumper (J5, J6) or can setup by programme.

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS1	**0**	**1**	**0**
BS2	**1**	**1**	**0**

Table 1 – MCU Interface Selection Setting

E/RD#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.
When connecting to an 8080-microprocessor, this pin receives the Read (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD) must be connected to VSS.

R/W#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.
When 8080 interface mode is selected, this pin is the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W must be connected to VSS.

D/C#：This pin is Data/Command control pin. When the pin is pulled high, the data at D0-D8 is treated as display data. When the pin is pulled low, the data at D0-D8 is transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams at following pages and datasheet.

RES#：This pin is reset signal input. When the pin is low, initialization of the chip is executed.

CS#：This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

VCC：This is the most positive voltage supply pin of the chip.

VDD：Power supply pin for logic operation of the driver.

GND：Power supply ground.

VCC_IN: This is the external most positive voltage supply. This pin should be shorted with VCC by Jumper 2 (J2)

VDD_IN: This is the external positive voltage supply. This pin should be shorted with VDD by Jumper 3 (J3)

3 Timing characteristics

VDD = 2.4 to 3.5V, TA= -40to 85°C

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 2 6800-Series MPU Parallel Interface Timing Characteristics

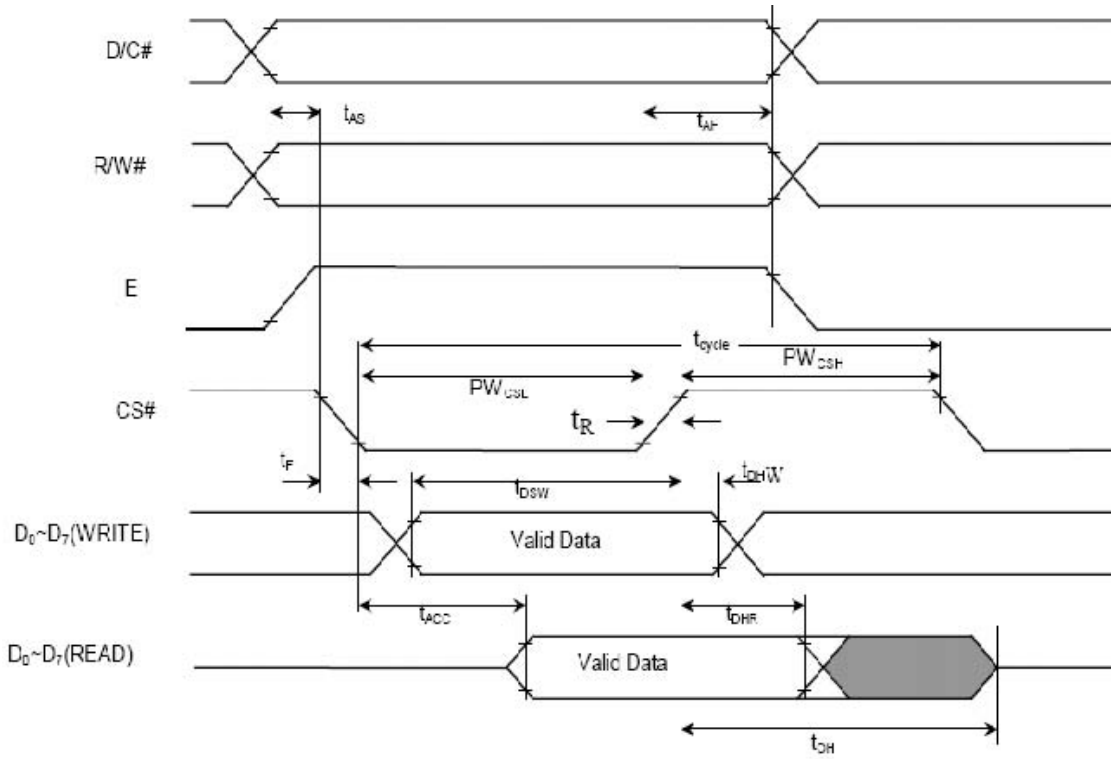


Figure 1 6800-series MPU parallel interface characteristics

VDD = 2.4 to 3.5V, TA= -40to 85°C

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 3 8080-Series MPU Parallel Interface Timing Characteristics

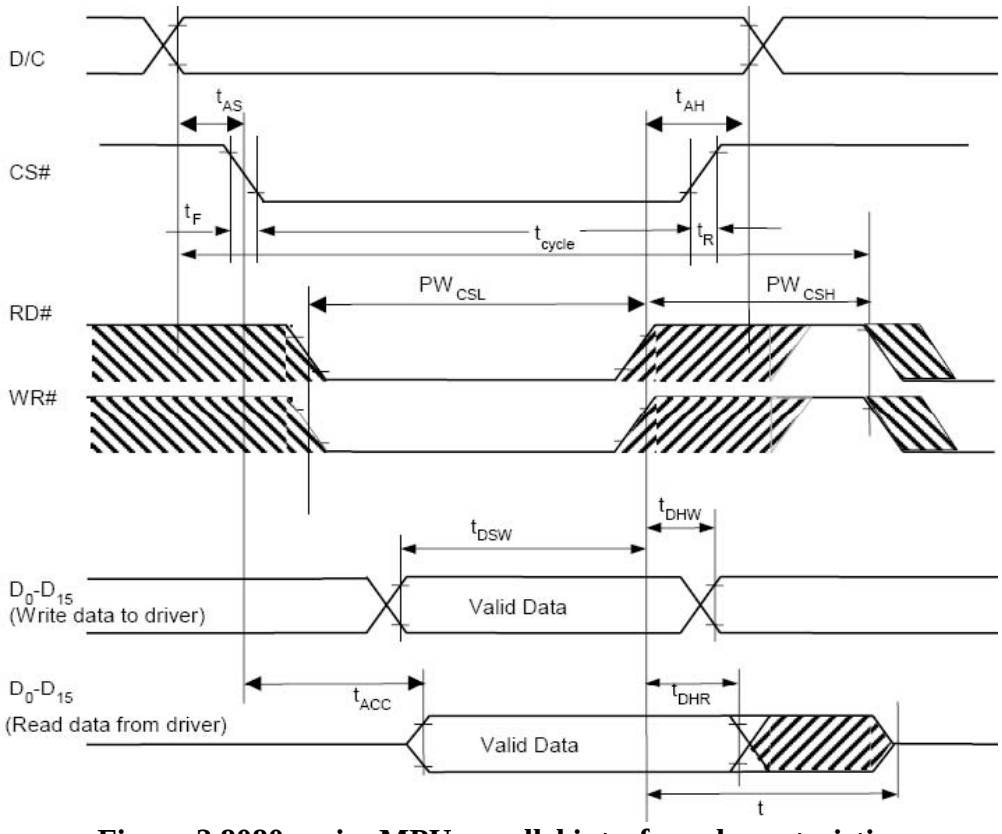


Figure 2 8080-series MPU parallel interface characteristics

Note：When 8 bit used: D_0 ~ D_7 instead.

VDD = 2.4 to 3.5V, TA= -40to 85°C

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Table 4 Serial Interface Timing Characteristics

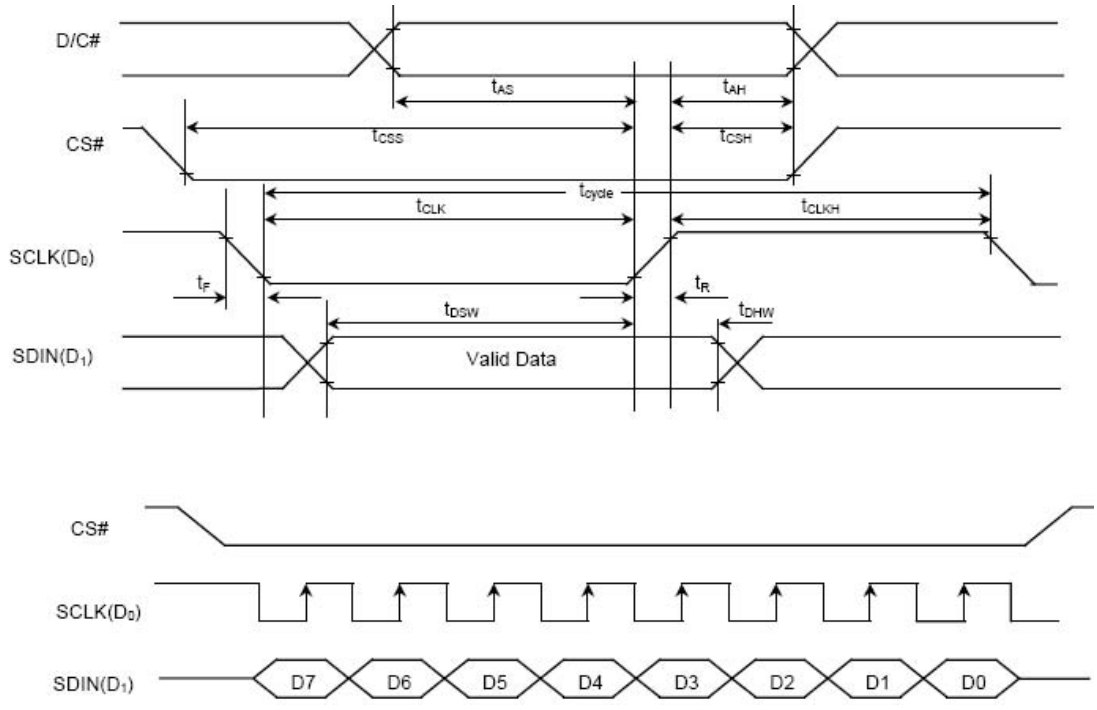


Figure 3 Serial interface characteristics

4 Connection Between OLED and EVK

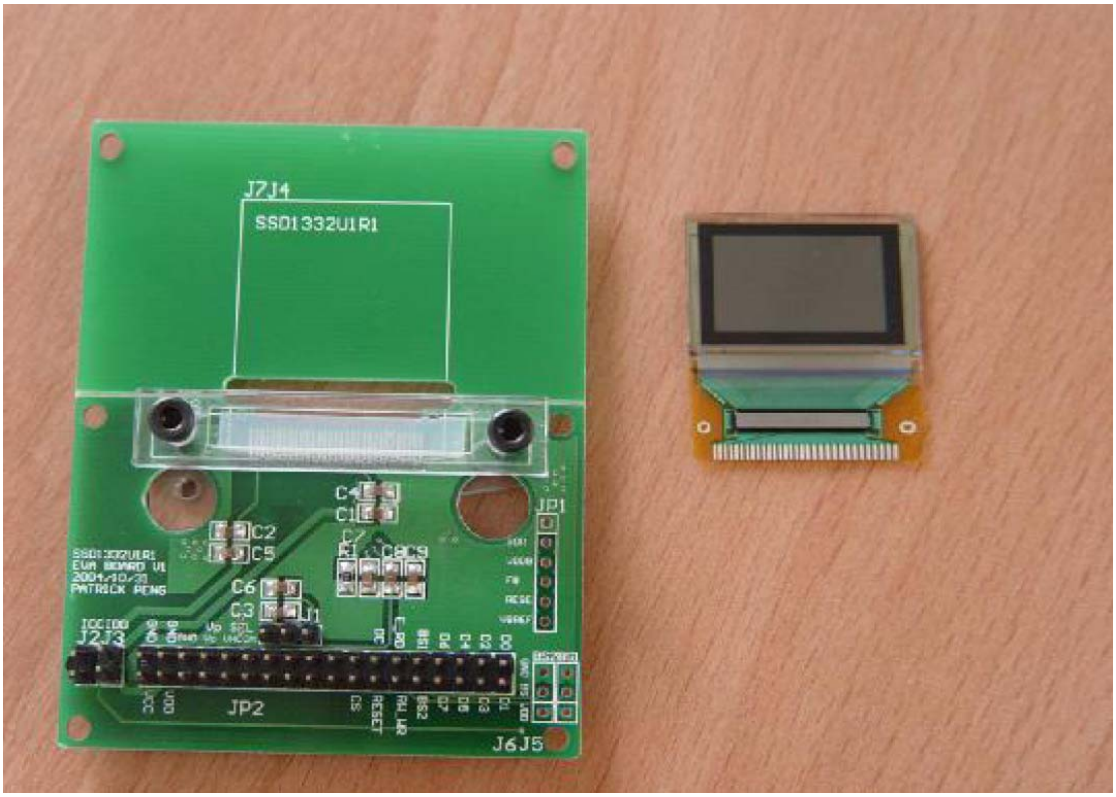


Figure 4 EVK PCB and DD-9664FC-1B Module

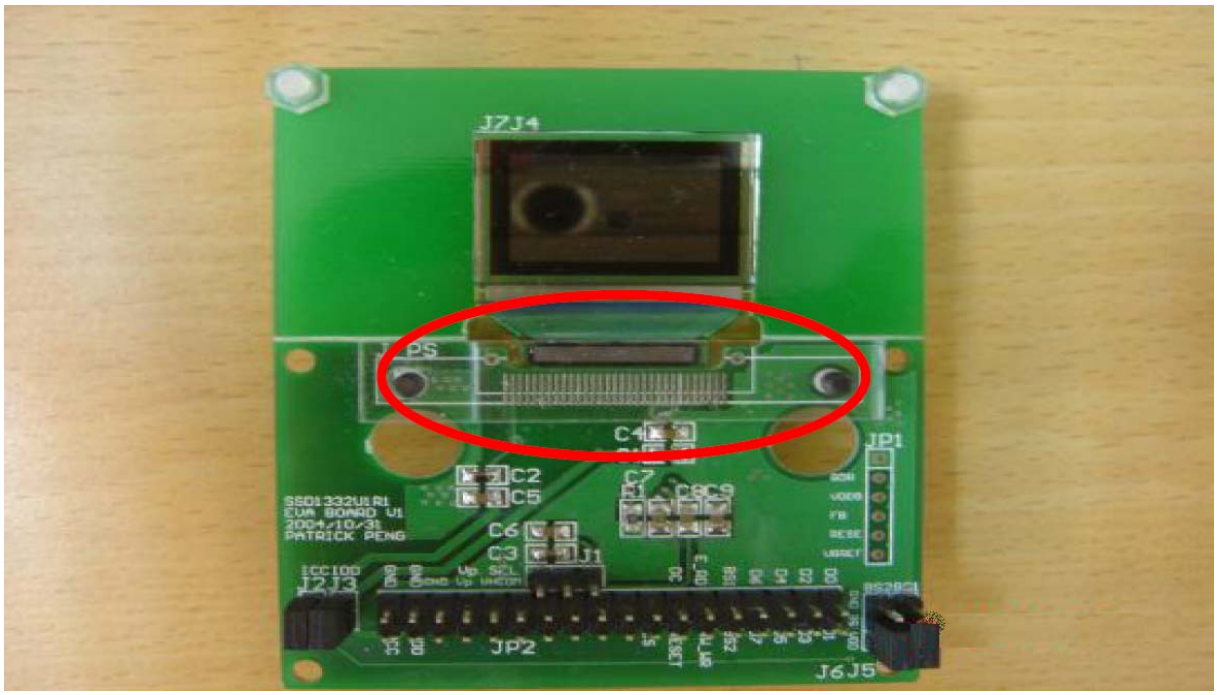


Figure 5 the DD-9664FC-1B and EVK assembled (Top view)

As the package is TCP, the connector pads are double sided. When assembling the OLED, make sure it is in the right direction as shown in Figure 5 and tightened with the two hexagonal bolts.

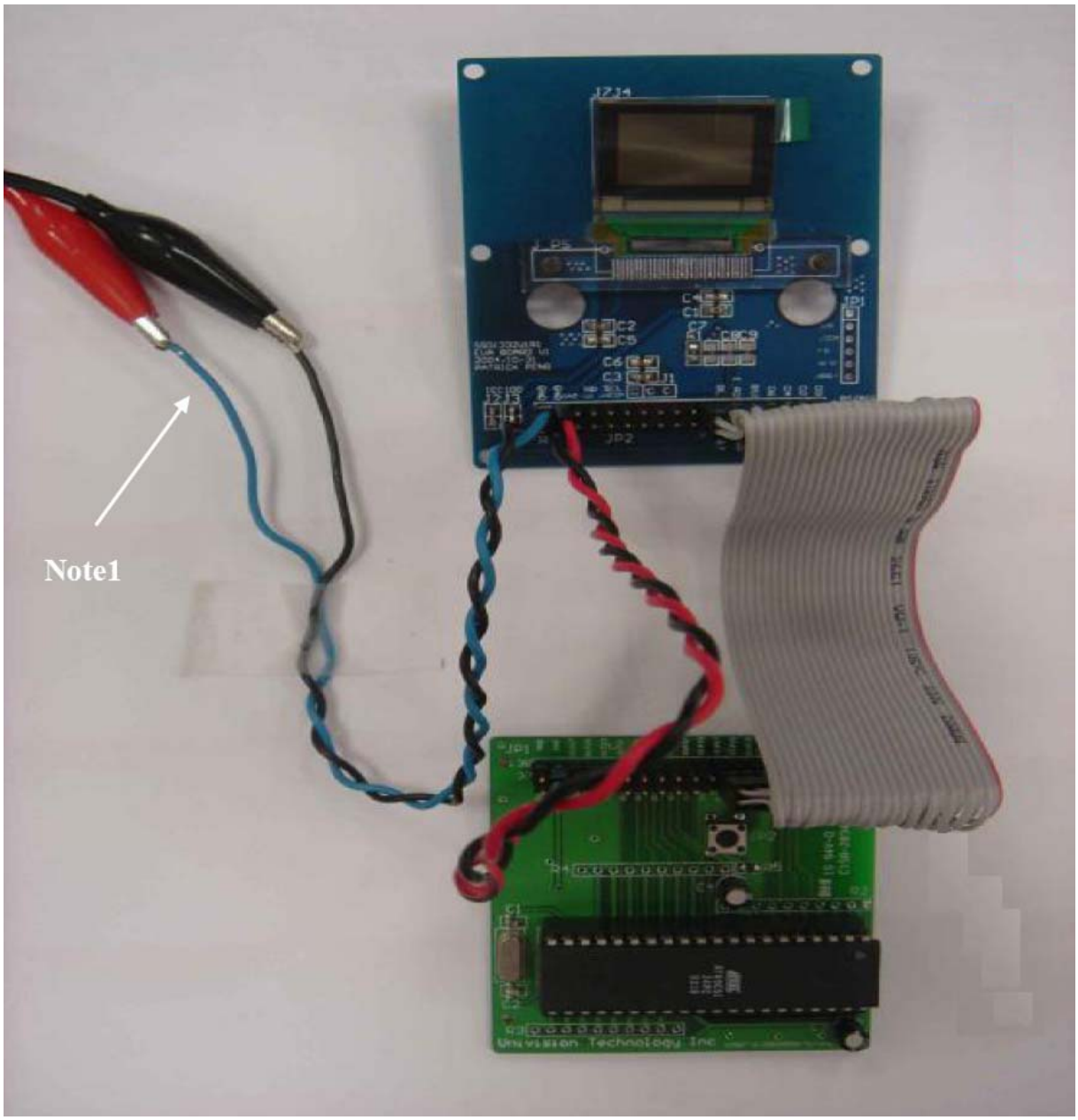
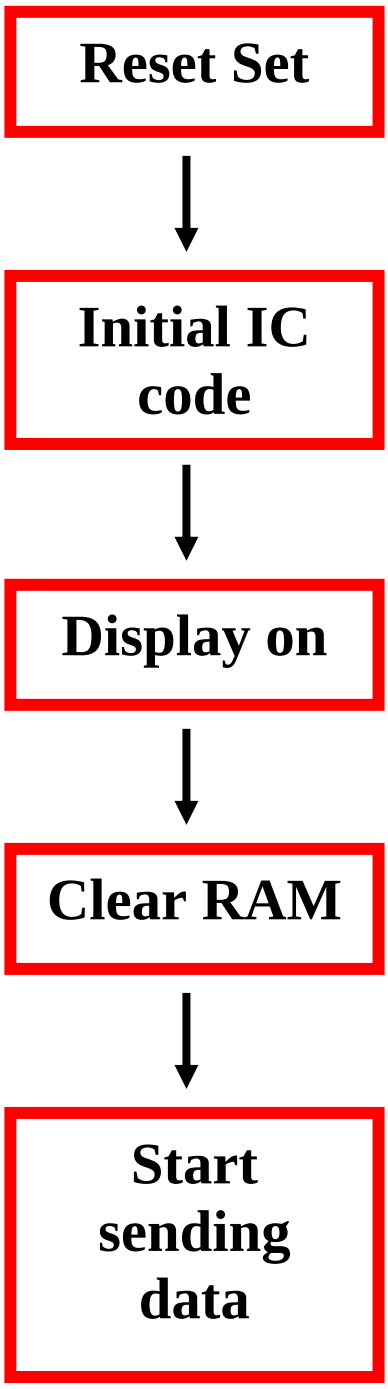


Figure 6 control MCU (not supplied) connected with EVK

Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.

5 How to use the DD-9664FC-1B



RES#=0; Delay 100ms; RES#=1

Suggest all registers set again

6 How to use the DD-9664FC-1B

6.1 Recommended Initial code

```
Void Initial_ic(void)
{
        IOCLR=0xffffffff;          //data=0
        IOSET=bBS1|bBS2|bRES|bCS|bE_RD;
        IOCLR=bD_C|bR_W;
        Reset_SSD1332();
        SubComOut (0xAE);     //Display off
        SubComOut (0xA0);     //Set Re-map / Color Depth
        SubComOut (0x70);     //65K 8bit B->G->R
        SubComOut (0xA1);     // Set display start line
        SubComOut (0x00);     //Start 00h
        SubComOut (0xA2);     //Set display offset
        SubComOut (0x00);     //Start 00h
        SubComOut (0xA4);     //Normal display
        SubComOut (0xB0);     //Power saving mode
        SubComOut (0x00);     //Normal mode
        SubComOut (0x87);     //Set master contrast
        SubComOut (0x0F);     //No change
        SubComOut (0xA8);     //Set Duty
        SubComOut (0x3F);     //63+1
        SubComOut (0x81);     //Set contrast A
        SubComOut (0x3C);
        SubComOut (0x82);     //Set contrast B
        SubComOut (0x37);
        SubComOut (0x83);     //Set contrast C
        SubComOut (0x73);
        SubComOut (0xBB);     //Set Vpa
        SubComOut (0x12);
        SubComOut (0xBC);     //Set Vpb
        SubComOut (0x13);
        SubComOut (0xBD);     //Set Vpc
        SubComOut (0x14);
        SubComOut (0xBE);     //Set VcomH
        SubComOut (0x46);
        SubComOut (0xAD);     //Set Master config
        SubComOut (0x8C);     //VcomH External
        SubComOut (0xB1);     //Set Pre-charge
        SubComOut (0x1F);
        SubComOut (0x81);     //Set contrast current for A
        SubComOut (0xC3);     // Color A
        SubComOut (0x82);     //Set contrast current for B
        SubComOut (0x82);     // Color B
        SubComOut (0x83);     //Set contrast current for C
        SubComOut (0xBE);     // Color C
        SubComOut (0xB3);     //Clock & frequency
        SubComOut (0xF0);     //Clock=Divser+1 frequency=fh
        SubComOut (0xAF);     //Display on
}
```

```
void Reset_SSD1332(void)
{
        IOCLR=bRES;
        Delay_1ms(10);
        IOSET=bRES;
}
void SubComOut (unsigned char out_command)
{
        IOCLR=bD_C;
        IOCLR=bCS;
        IOCLR=bR_W;
        IOCLR=0x000000ff;
        IOSET= out_command;
        IOSET=bR_W;
        IOSET=bCS;
}
void SubDataOut(unsigned char out_data)
{
        IOSET=bD_C;
        IOCLR=bCS;
        IOCLR=bR_W;
        IOCLR=0x000000ff;
        IOSET=out_data;
        IOSETbR_W;
        IOSET=bCS;
}
void Delay_1ms(int Cycle)
{
        unsigned int i,k;
        for (i=0 ;i<Cycle;i++)
        for(k=0;k<0x2fff;k++);
}
```