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NTE74LS138
Integrated Circuit
TTL – 3–Line–to–8–Line Decoder/Demultiplexer

Description:

The NTE74LS138 is a 3–line–to–8–line decoder/demultiplexer in a 16–Lead plastic DIP type package designed to be used in high–performance memory decoding or data–routing applications requiring very short propagation delay times. In high–performance memory systems this device can be used to minimize the effects of system decoding. When employed with high–speed memories utilizing a fast enable circuit the delay times of the decoder and the enable time of th memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky–clamped system decoder is negligible.

The NTE74LS138 decodes one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active–low and one active–high enable inputs reduce the need for external gates or inverters when expanding. A 24–line decode can be implemented without external inverters and a 32–line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The NTE74LS138 features fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high–performance Schottky diodes to suppress line–ringing and to simplify system design.

Features:

- Designed Specifically for High–Speed:
  - Memory Decodes
  - Data Transmissions Systems
- 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Schottky–Clamped for High Performance

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Input Voltage	V_{IH}	2	–	–	V
Low−Level Input Voltage	V_{IL}	–	–	0.8	V
High−Level Output Current	I_{OH}	–	–	−0.4	mA
Low−Level Output Current	I_{OL}	–	–	8	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = 0.4mA		2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	Enable	–	–	−0.4	mA
			A, B, C	–	–	−0.2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Outputs Enabled and Open		–	6.2	10	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Levels of Logic	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (From Binary Input to Any Output)	t_{PLH}	2	R_L = 2kΩ, C_L = 15pF	–	11	20	ns
	t_{PHL}	2		–	18	41	ns
Propagation Delay Time (From Select Input to Any Output)	t_{PLH}	3		–	21	27	ns
	t_{PHL}	3		–	20	39	ns
Propagation Delay Time (From Enable Input to Any Output)	t_{PLH}	2		–	12	18	ns
	t_{PHL}	2		–	20	32	ns
	t_{PLH}	3		–	14	26	ns
	t_{PHL}	3		–	13	38	ns

Function Table:

Inputs					Outputs							
Enable		Select										
G1	$\overline{G}2$ *	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

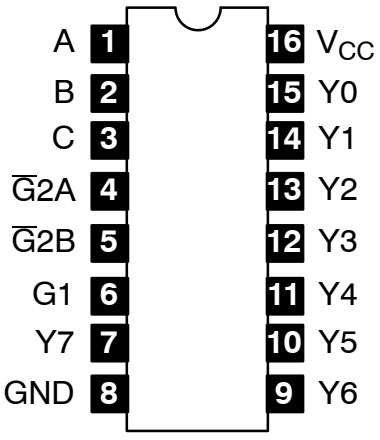
* $\overline{G}2 = \overline{G}2A + \overline{G}2B$

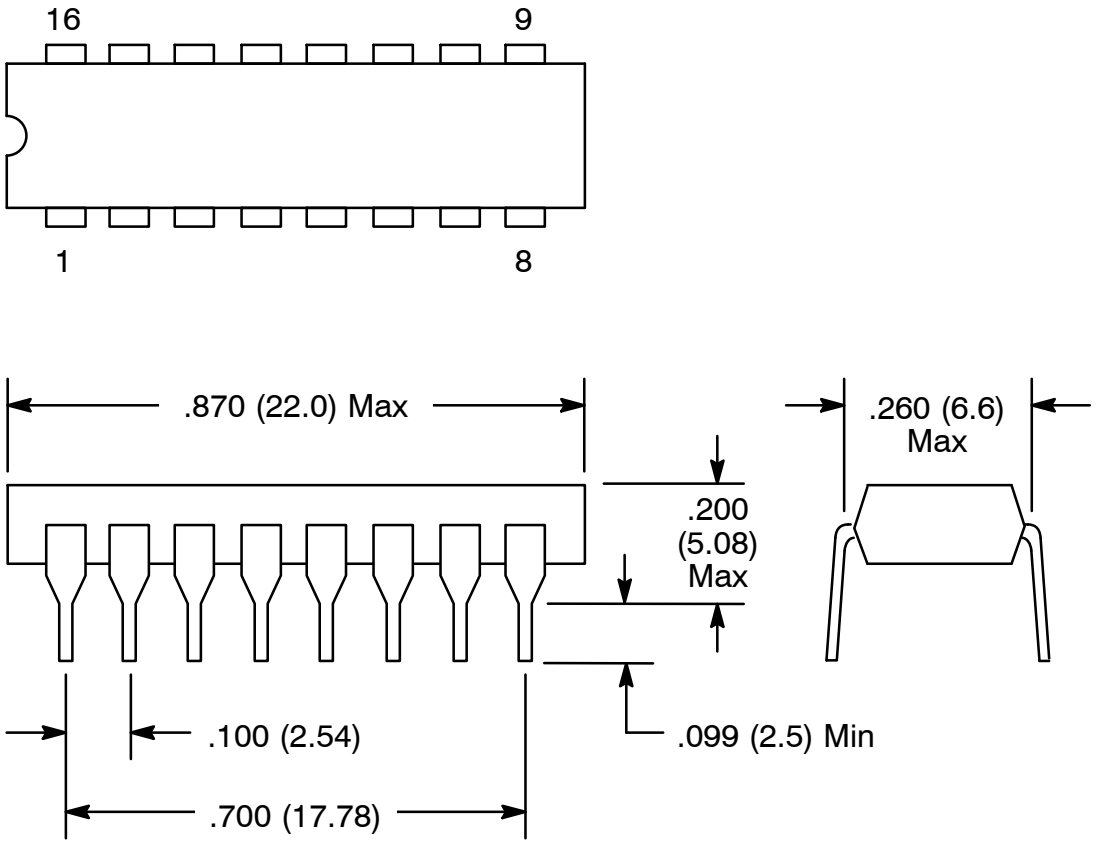
H = HIGH Level

L = LOW Level

X = Don't Care

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)