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NTE74LS164
Integrated Circuit
TTL – 8–Bit Parallel–Out Serial Shift Register

Description:

The NTE74LS164 is an 8–bit parallel–out serial shift register in a 14–Lead plastic DIP type package that features gated serial inputs and asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip–flop to the low level at the next clock pulse. A high–level input enables the other input which will then determine th state of the first flip–flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup–time requirements will be entered. Clocking occurs on the low–to–high–level transition of the clock input. All inputs are diode–clamped to minimize transmission–line effects.

Features:

- Gated Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Power Dissipation (per Bit), P_D 10mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–0.4	mA
Low–Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Clock or Clear Input Pulse	t_w	20	–	–	ns
Data Setup Time	t_{su}	15	–	–	ns
Clear Inactive Setup Time	t_{su}	15	–	–	ns
Data Hold Time	t_h	5	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −0.4μA		2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V		–	–	−0.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5		–	16	27	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time, and duration of the short−circuit should not exceed one second.

Note 5. I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary GND, then 4.5V applied to clear.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 2kΩ, C_L = 15pF	25	36	–	MHz
Propagation Delay Time (High−to−Low−Level Q Outputs from Clear Input)	t_{PHL}		–	24	36	ns
Propagation Delay Time (Low−to−High−Level Q Outputs from Clock Input)	t_{PLH}		–	17	27	ns
Propagation Delay Time (High−to−Low−Level Q Outputs from Clock Input)	t_{PHL}		–	21	32	ns

Function Table:

Inputs				Outputs			
$\overline{Clear}$	Clock	A	B	Q_A	Q_B	. . .	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = HIGH Level (Steady State)

L = LOW Level (Steady State)

X = Irrelevant (Any Input, including Transitions)

↑ = Transition from LOW to HIGH Level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady−state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one−bit shift.

Pin Connection Diagram