

PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

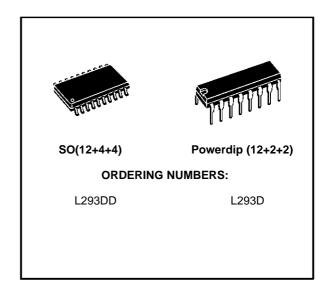
- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (non repetitive) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

DESCRIPTION

The Device is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power transistors.

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

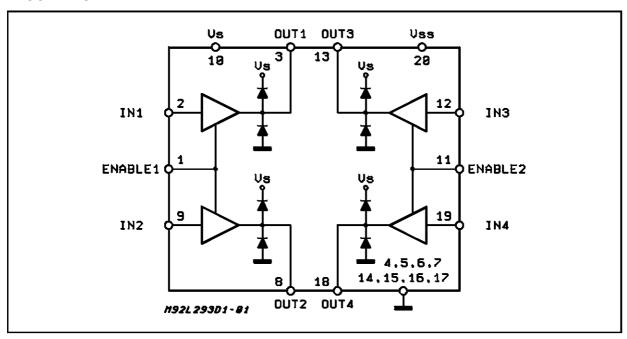
This device is suitable for use in switching applications at frequencies up to 5 kHz.



The L293D is assembled in a 16 lead plastic packaage which has 4 center pins connected together and used for heatsinking

The L293DD is assembled in a 20 lead surface mount which has 8 center pins connected together and used for heatsinking.

BLOCK DIAGRAM

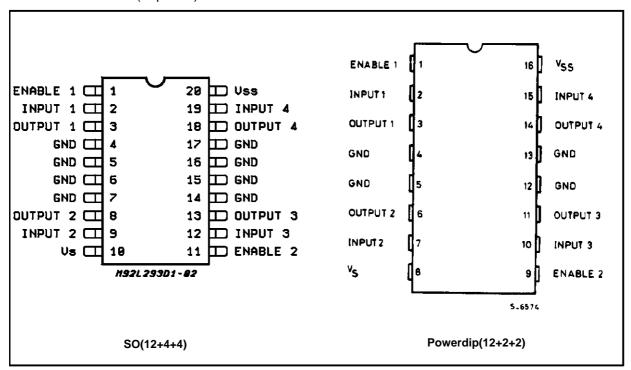


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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage	36	V
V _{SS}	Logic Supply Voltage	36	V
Vi	Input Voltage	7	V
V _{en}	Enable Voltage	7	V
Io	Peak Output Current (100 μs non repetitive)	1.2	Α
P _{tot}	Total Power Dissipation at T _{pins} = 90 °C	4	W
T_{stg}, T_j	Storage and Junction Temperature	- 40 to 150	°C

PIN CONNECTIONS (Top view)



THERMAL DATA

Symbol	Decription	DIP	SO	Unit
R _{th j-pins}	Thermal Resistance Junction-pins max.	_	14	°C/W
R _{th j-amb}	Thermal Resistance junction-ambient max.	80	50 (*)	°C/W
R _{th j-case}	Thermal Resistance Junction-case max.	14	_	

^(*) With 6sq. cm on board heatsink.



ELECTRICAL CHARACTERISTICS (for each channel, $V_S = 24 \text{ V}$, $V_{SS} = 5 \text{ V}$, $T_{amb} = 25 \,^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Vs	Supply Voltage (pin 10)		V _{SS}		36	V
V_{SS}	Logic Supply Voltage (pin 20)		4.5		36	V
Is	Total Quiescent Supply Current	$V_i = L$; $I_O = 0$; $V_{en} = H$		2	6	mA
	(pin 10)	$V_i = H$; $I_O = 0$; $V_{en} = H$		16	24	mA
		V _{en} = L			4	mA
I _{SS}	Total Quiescent Logic Supply	$V_i = L$; $I_0 = 0$; $V_{en} = H$		44	60	mA
	Current (pin 20)	$V_i = H$; $I_O = 0$; $V_{en} = H$		16	22	mA
		V _{en} = L		16	24	mA
V_{IL}	Input Low Voltage (pin 2, 9, 12, 19)		-0.3		1.5	V
V _{IH}	Input High Voltage (pin 2, 9,	V _{SS} ≤ 7 V	2.3		V _{SS}	V
	12, 19)	V _{SS} > 7 V	2.3		7	V
I _{IL}	Low Voltage Input Current (pin 2, 9, 12, 19)	V _{IL} = 1.5 V			- 10	μА
Іін	High Voltage Input Current (pin 2, 9, 12, 19)	$2.3~\text{V} \leq \text{V}_{\text{IH}} \leq \text{V}_{\text{SS}} - 0.6~\text{V}$		30	100	μА
V _{en L}	Enable Low Voltage (pin 1, 11)		-0.3		1.5	V
V _{en H}	Enable High Voltage	V _{SS} ≤ 7 V	2.3		V _{SS}	V
	(pin 1, 11)	V _{SS} > 7 V	2.3		7	V
l _{en L}	Low Voltage Enable Current (pin 1, 11)	V _{en L} = 1.5 V		- 30	- 100	μА
l _{en H}	High Voltage Enable Current (pin 1, 11)	$2.3~\text{V} \leq \text{V}_{\text{en H}} \leq \text{V}_{\text{SS}} - 0.6~\text{V}$			± 10	μА
$V_{\text{CE(sat)H}}$	Source Output Saturation Voltage (pins 3, 8, 13, 18)	$I_{O} = -0.6 \text{ A}$		1.4	1.8	V
V _{CE(sat)L}	Sink Output Saturation Voltage (pins 3, 8, 13, 18)	I _O = + 0.6 A		1.2	1.8	V
V_{F}	Clamp Diode Forward Voltage	I _O = 600nA		1.3		V
t _r	Rise Time (*)	0.1 to 0.9 V _O		250		ns
t _f	Fall Time (*)	0.9 to 0.1 V _O		250		ns
t _{on}	Turn-on Delay (*)	0.5 V _i to 0.5 V _O		750		ns
t _{off}	Turn-off Delay (*)	0.5 V _i to 0.5 V _O		200		ns

^(*) See fig. 1.



TRUTH TABLE (one channel)

Input	Enable (*)	Output
Н	Н	Н
L	Н	L
Н	L	Z
L	L	Z

Z = High output impedance

Figure 1: Switching Times

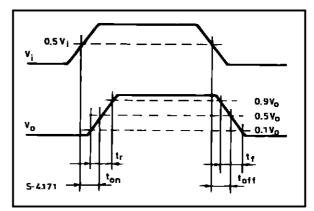
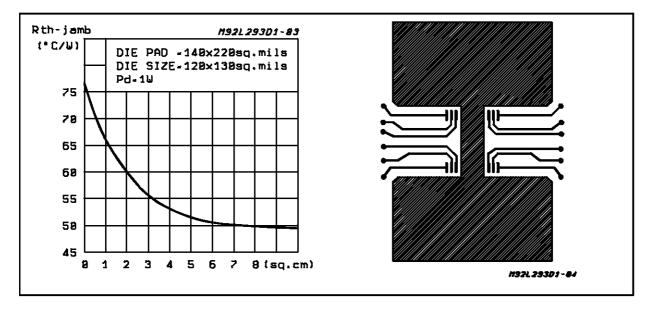


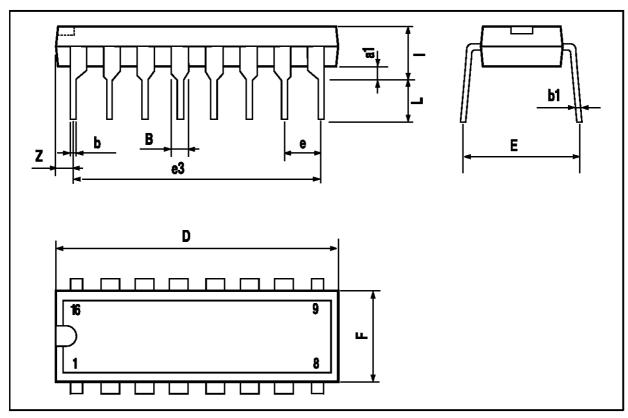
Figure 2: Junction to ambient thermal resistance vs. area on board heatsink (SO12+4+4 package)



^(*) Relative to the considered channel

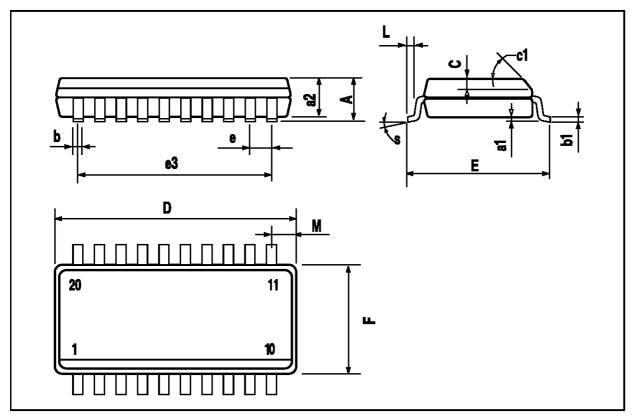
POWERDIP16 PACKAGE MECHANICAL DATA

DIM.		mm			inch	
Dim.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
е		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



SO20 PACKAGE MECHANICAL DATA

DIM.		mm			inch	
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
С		0.5			0.020	
c1		45			1.772	
D		1	12.6		0.039	0.496
E	10		10.65	0.394		0.419
е		1.27			0.050	
e3		11.43			0.450	
F		1	7.4		0.039	0.291
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
М			0.75			0.030
S			8° (ı	max.)		



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PUSH-PULL FOUR CHANNEL DRIVERS

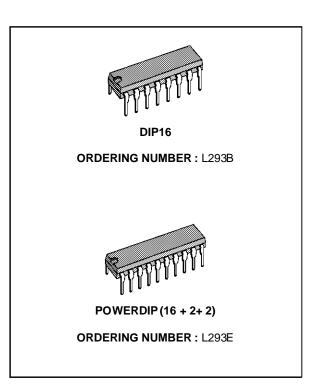
- OUTPUT CURRENT 1A PER CHANNEL
- PEAK OUTPUT CURRENT 2A PER CHANNEL (non repetitive)
- INHIBIT FACILITY
- HIGH NOISE IMMUNITY
- SEPARATE LOGIC SUPPLY
- OVERTEMPERATURE PROTECTION

DESCRIPTION

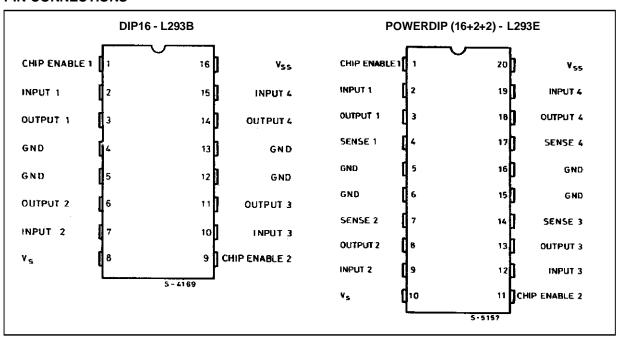
The L293B and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally, the L293E has external connection of sensing resistors, for switchmode control.

The L293B and L293E are package in 16 and 20-pin plastic DIPs respectively; both use the four center pins to conduct heat to the printed circuit board.

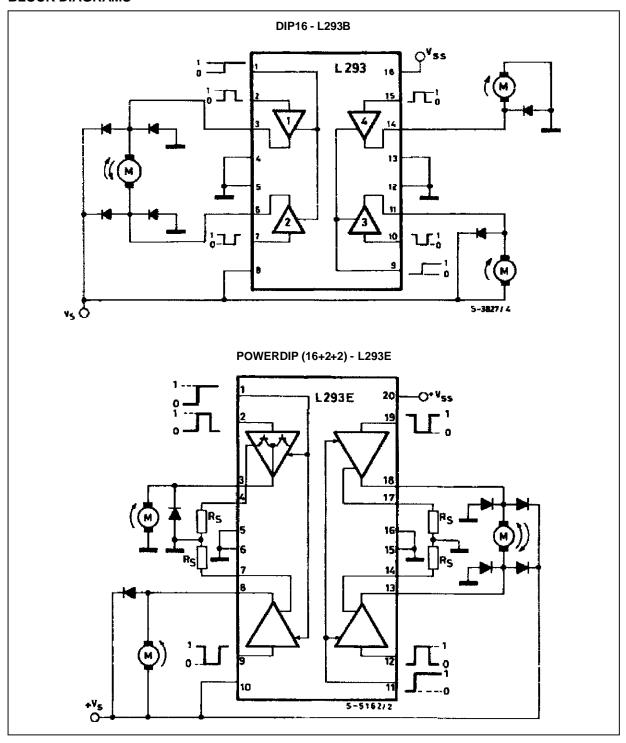


PIN CONNECTIONS

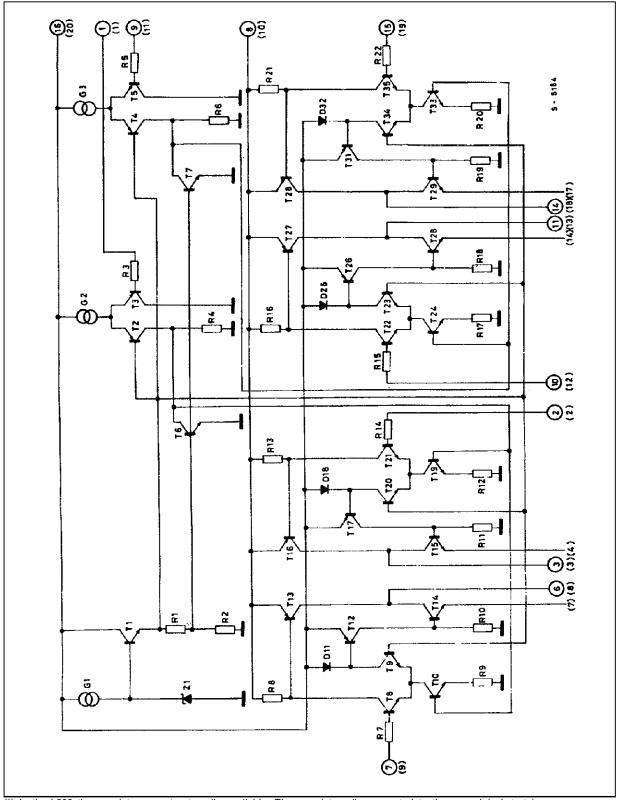


April 1993

BLOCK DIAGRAMS



SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate). O Pins of L293 () Pins of L293E.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage	36	V
V _{ss}	Logic Supply Voltage	36	V
Vi	Input Voltage	7	V
V _{inh}	Inhibit Voltage	7	V
l _{out}	Peak Output Current (non repetitive t = 5ms)	2	Α
P _{tot}	Total Power Dissipation at T _{ground-pins} = 80°C	5	W
T _{stg} , T _j	Storage and Junction Temperature	-40 to +150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-case}	Thermal Resistance Junction-case Max.	14	°C/W
R _{th j-amb}	Thermal Resistance Junction-ambient Max.	80	°C/W

ELECTRICAL CHARACTERISTICS

For each channel, $V_S = 24V$, $V_{SS} = 5V$, $T_{amb} = 25^{\circ}C$, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	TYp.	Max.	Unit
Vs	Supply Voltage		V _{ss}		36	V
V _{ss}	Logic Supply Voltage		4.5		36	V
Is	Total Quiescent Supply Current	$ \begin{array}{cccc} V_i = L & I_o = 0 & V_{inh} = H \\ V_i = H & I_o = 0 & V_{inh} = H \\ & V_{inh} = L \end{array} $		2 16	6 24 4	mA
I _{ss}	Total Quiescent Logic Supply Current	$ \begin{array}{lll} V_i = L & I_o = 0 \\ V_i = H & I_o = 0 \end{array} & \begin{array}{lll} V_{inh} = H \\ V_{inh} = H \\ V_{inh} = L \end{array} $		44 16 16	60 22 24	mA
V _{iL}	Input Low Voltage		-03.		1.5	V
V _{iH}	Input High Voltage	$V_{SS} \le 7V$ $V_{SS} > 7V$	2.3 2.3		V _{ss} 7	V
l _{iL}	Low Voltage Input Current	$V_{il} = 1.5V$			-10	μΑ
I _{iH}	High Voltage Input Current	$2.3V \le V_{IH} \le V_{ss} - 0.6V$		30	100	μΑ
V _{inhL}	Inhibit Low Voltage		-0.3		1.5	V
V _{inhH}	Inhibit High Voltage	$V_{SS} \le 7V$ $V_{ss} > 7V$	2.3 2.3		V _{ss} 7	>
linhL	Low Voltage Inhibit Current	$V_{inhL} = 1.5V$		-30	-100	μΑ
I _{inhH}	High Voltage Inhibit Current	$2.3V \le V_{inhH} \le V_{ss} - 0.6V$			±10	μΑ
V _{CEsatH}	Source Output Saturation Voltage	$I_0 = -1A$		1.4	1.8	V
V _{CEsatL}	Sink Output Saturation Voltage	$I_0 = 1A$		1.2	1.8	V
V _{SENS}	Sensing Voltage (pins 4, 7, 14, 17) (**)				2	>
t _r	Rise Time	0.1 to 0.9 V _o (*)		250		ns
t _f	Fall Time	0.9 to 0.1 V _o (*)		250		ns
t _{on}	Turn-on Delay	0.5 V _i to 0.5 V _o (*)		750		ns
toff	Turn-off Delay	0.5 V _i to 0.5 V _o (*)		200		ns

See figure 1

TRUTH TABLE

V _i (each channel)	Vo	V _{inh} (∞)
Н	Н	Н
L	L	Н
Н	X (°)	L
L	X (°)	L



Referred to L293E

^(*) High output impedance (**) Relative to the considerate channel

Figure 1: Switching Timers

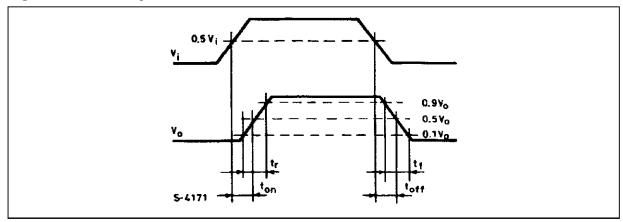


Figure 2: Saturation voltage versus Output Current

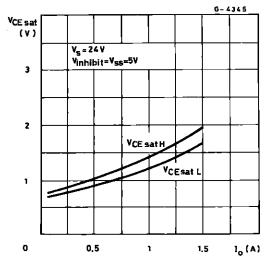


Figure 4: Sink Saturation Voltage versus Ambient Temperature

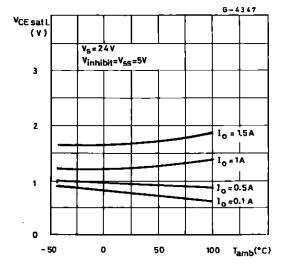


Figure 3: Source Saturation Voltage versus Ambient Temperature

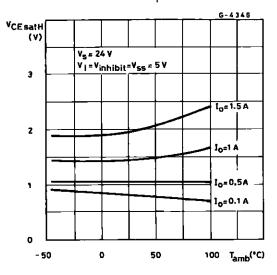


Figure 5: Quiescent Logic Supply Current versus Logic Supply Voltage

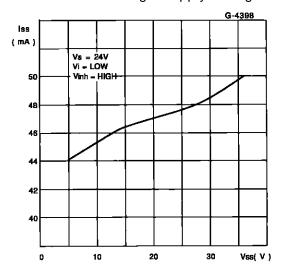


Figure 6: Output Voltage versus Input Voltage

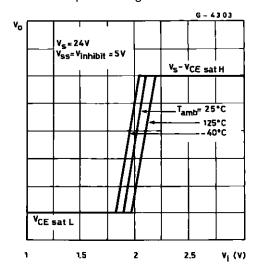
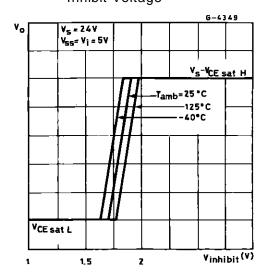
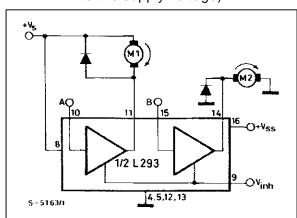


Figure 7: Output Voltage versus Inhibit Voltage



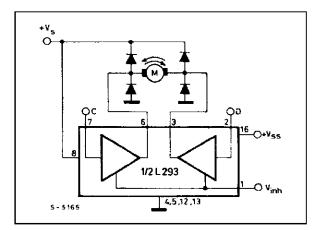
APPLICATION INFORMATION

Figure 8: DC Motor Controls (with connection to ground and to the supply voltage)



Vinh	Α	M1	В	M2
Н	Н	Fast Motor Stop	Н	Run
Н	L	Run	L	Fast Motor Stop
L	Χ	Free Running Motor Stop	Х	Free Running Motor Stop
L = L	_ow	H = High	High X = Don't Care	

Figure 9: Bidirectional DC Motor Control



Inputs	Function		
V _{inh} = H	C = H; D = L	Turn Right	
	C = L; D = H	Turn Left	
	C = D	Fast Motor Stop	
Vinh = L	C = X ; D = X	Free Running Motor Stop	
L = Low	H = High	X = Don't Care	

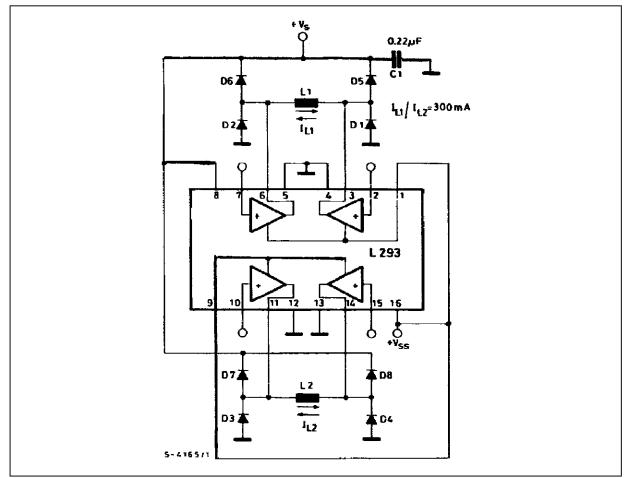


Figure 10 : Bipolar Stepping Motor Control

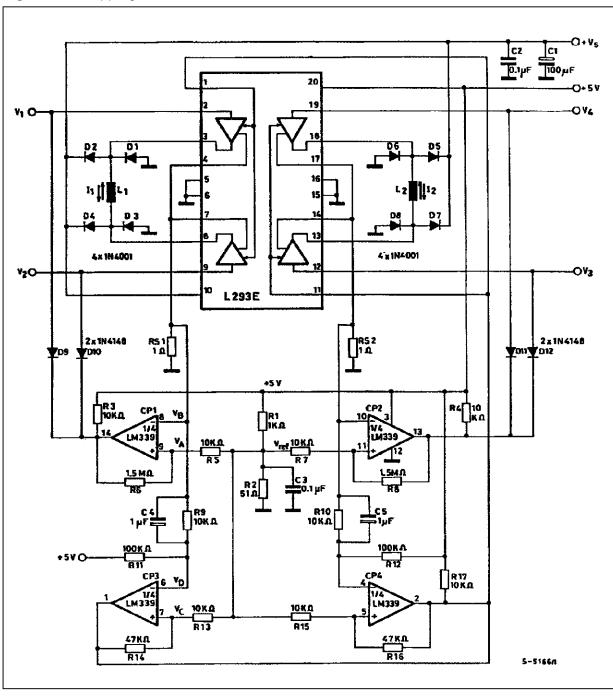
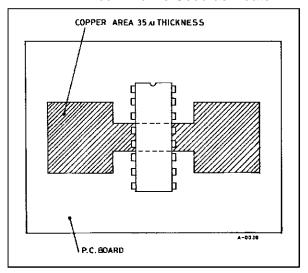


Figure 11 : Stepping Motor Driver with Phase Current Control and Short Circuit Protection

MOUNTING INSTRUCTIONS

The R_{th j-amb} of the L293B and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 12 or to an external heatsink (figure 13).

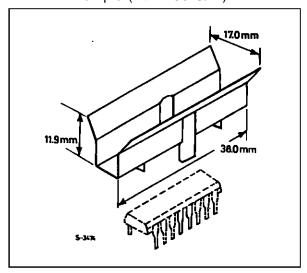
Figure 12 :Example of P.C. Board Copper Area which is Used as Heatsink



During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

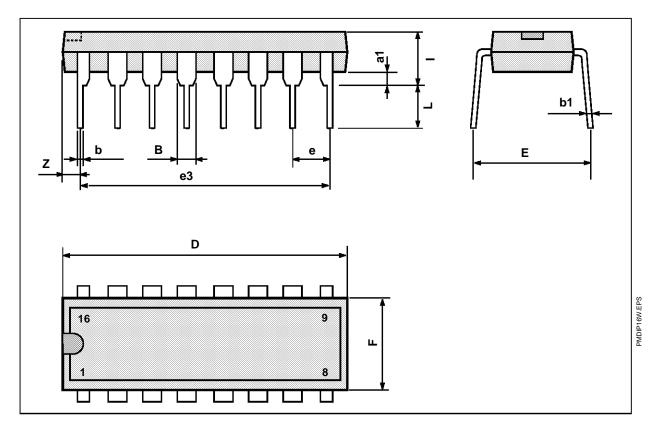
The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 13 :External Heatsink Mounting Example (Rth = 30°C/W)



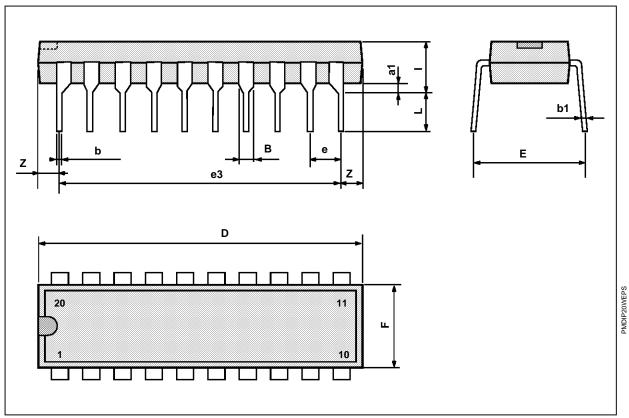
DIP16 PACKAGE MECHANICAL DATA

Dimensions		Millimeters			Inches		
Dimensions	Min.	Тур.	Max.	Min.	Тур.	Max.	
a1	0.51			0.020			
В	0.77		1.65	0.030		0.065	
b		0.5			0.020		
b1		0.25			0.010		
D			20			0.787	DIP16PW.TBL
E		8.5			0.335		DIP16
е		2.54			0.100		
e3		17.78			0.700		
F			7.1			0.280	
i			5.1			0.201	
L		3.3			0.130		
Z			1.27			0.050	



POWERDIP (16+2+2) PACKAGE MECHANICAL DATA

Dimensions		Millimeters			Inches		
Dimensions	Min.	Тур.	Max.	Min.	Тур.	Max.	
a1	0.51			0.020			
В	0.85		1.4	0.033		0.055	
b		0.5			0.020		
b1	0.38		0.5	0.015		0.020	
D			24.8			0.976	
E		8.8			0.346		
е		2.54			0.100		
e3		22.86			0.900		
F			7.1			0.280	
i			5.1			0.201	
L		3.3			0.130		
Z			1.27			0.050	



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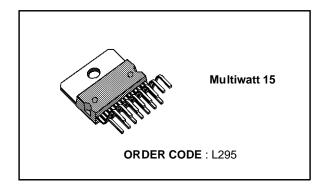
DUAL SWITCH-MODE SOLENOID DRIVER

PRELIMINARY DATA

- HIGH CURRENT CAPABILITY (up to 2.5A per channel)
- HIGH VOLTAGE OPERATION (up to 46V for power stage)
- HIGHEFFICIENCY SWITCHMODE OPERATION
- REGULATED OUTPUT CURRENT (adjustable)
- FEW EXTERNAL COMPONENTS
- SEPARATE LOGIC SUPPLY
- THERMAL PROTECTION

DESCRIPTION

The L295 is a monolithic integrated circuit in a 15-lead Multiwatt ® package; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels at the inputs and can drive 2 solenoids. The output current is completely controlled by means of a switch-



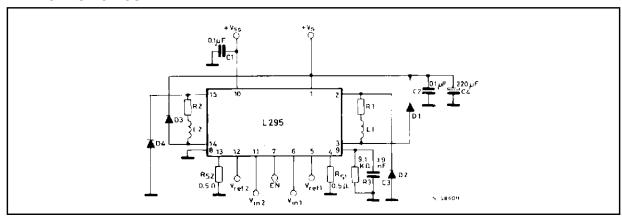
ing technique allowing very efficient operation. Furthermore, it includes an enable input and dual supplies (for interfacing with peripherals running at a higher voltage than the logic).

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.

ABSOLUTE MAXIMUM RATINGS

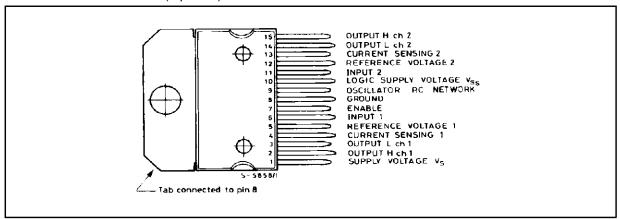
Symbol	Parameter	Value	Unit
Vs	Supply voltage	50	V
V _{ss}	Logic supply voltage	12	V
V_{EN}, V_{i}	Enable and input voltage	7	V
V_{ref}	Reference voltage	7	V
lo	Peak output current (each channel)		
	- non repetitive (t = 100 μsec)	3	Α
	- repetitive (80% on - 20% off; Ton = 10 ms)	2.5	Α
	- DC operation	2	Α
Ptot	Total power dissipation (at Tcase = 75 °C	25	W
Tstg, Tj	Storage and junction temperature	- 40 to 150	°C

APPLICATION CIRCUIT

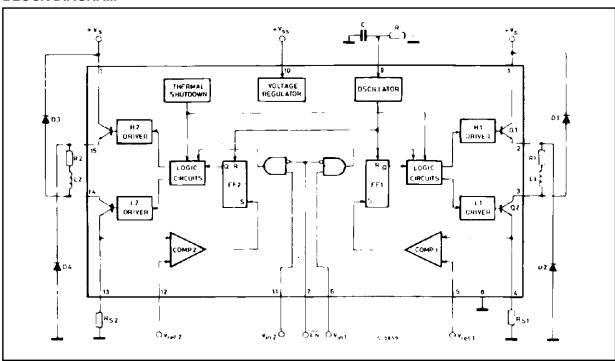


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CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th-j-case}	Thermal resistance junction-case max	3	°C/W
R _{th-j-amb}	Thermal resistance junction-ambient max	35	°C/W

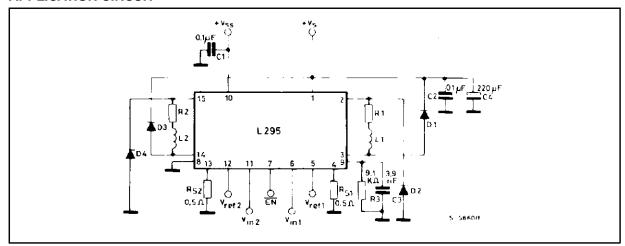


ELECTRICAL CHARACTERISTICS (Refer to the application circuit, $V_{ss} = 5V$, $V_s = 36V$; $T_j = 25^{\circ}C$; L = Low; H = High; unless otherwise specified)

Symbol	Parameter	Test	conditions	Min.	Тур.	Max.	Unit
Vs	Supply Voltage			12		46	V
V _{ss}	Logic Supply Voltage			4.75		10	V
I _d	Quiescent drain current (from VSS)	V _S = 46V; V _{i1} =	$V_{i2} = V_{EN} = L$			4	mA
I _{ss}	Quiescent drain current (from VS)	V _{SS} = 10 V				46	mA
V _{i1} ,,V _{i2}	Input Voltage		Low	-0.3		0.8	\ \ \
			High	2.2		7	ľ
V _{EN}	Enable Input Voltage		Low	-0.3		0.8	\ \
			High	2.2		7	,
l _{i1} , l _{i2}	Input Current		$V_{i1} = V_{i2} = L$			-100	μΑ
			$V_{i1} = V_{i2} = H$			10	
I _{EN}	Enable Input Current		V _{EN} = L			-100	μΑ
			V _{EN} = H			10	μπ
V _{ref1} , V _{ref2}	Input Reference Voltage			0.2		2	V
I _{ref1} , I _{ref2} m	Input Reference Voltage					-5	μА
Fosc	Oscillation Frequency	C = 3.9 nF;	R = 9.1 KΩ		25		KHz
Ip	Transconductance (each ch.)	V _{ref} = 1V		1.9	2	2.1	A/V
V _{ref}	Transcorradotarios (caon on.)	viei – i v		1.0	_	2.1	7,00
V _{drop}	Total output voltage drop (each channel) (*)	I ₀ = 2 A			2.8	3.6	V
V _{sens1} V _{sens2}	External sensing resistors voltage drop					2	V

^(*) V_{drop} = V_{CEsat Q1} + V_{CEsat Q2}.

APPLICATION CIRCUIT



D2, D4 = 2A High speed diodes D1, D3 = 1A High speed diodes

) trr ≤ 200 ns

 $R1 = R2 = 2\Omega$ L1 = L2 = 5 mH

FUNCTIONAL DESCRIPTION

The L295 incorporates two indipendent driver channals with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three micriprocessor compatible digital inputs and two analog inputs.

These inputs are:

EN chip enable (digital input, active low), enables both channels when in the low

state.

V_{in1}, V_{in2} channel inputs (digital inputs, active high), enable each channel independently. A channel is actived when

both EN and the appropriate channel input are active.

V_{ref1}, V_{ref2} referce voltages (analog inputs), used to program the peak load currents.

Peak load current is proportional to V_{ref}

Since the two channels are identical, only channel one will be described.

The following description applies also the channel two, replacing FF2 for FF1, V_{ref} for V_{ref1} etc.

When the channel is avtivated by low level on the EN input and a high level on the channel input, V_{in2} , the output transistors Q1 and Q2 switch on and

current flows in the load according to the exponential law:

$$I = \frac{V}{R1} \qquad (1 - e \frac{-R1 t}{L1})$$

where:

R1 and R2 are the resistance and inductance of the load and V is the voltage available on the load (V_s - V_{drop} - V_{sense}).

The current increases until the voltage on the external sensing resistor, R_{S1} , reaches the reference voltage, V_{ref1} . This peak current, I_{p1} , is given by:

$$I_{p1} = \frac{V_{ref1}}{R_{S1}}$$

At this point the comparator output, Vomp1, sete the RS flip-flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1}, decreases according to the law:

$$I = (\frac{V_A}{R_1} + I_{p1}) e \frac{-R1 t}{L1} - \frac{V_A}{R1}$$

where $V_A = V_{CEsat Q2} + V_{sense} + V_{D2}$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in fig. 1.

At this time t_2 the channel <u>1</u> is disabled, by taking the inputs V_{in1} low and/or \overline{EN} high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law:

$$I = (\frac{V_B}{R_1} + I_{T2}) e \frac{-R1 t}{L1} - \frac{V_B}{R1}$$

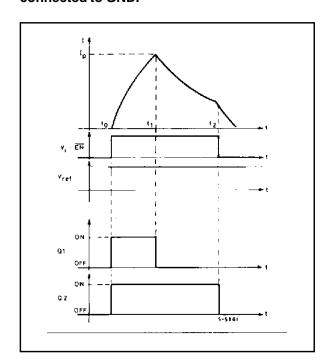
where $V_B = V_S + V_{D1} + V_{D2}$

 I_{T2} = current value at the time t_2 .

Fig. 2 in shows the current waveform obtained with an RC network connected between pin 9 and ground. From to t_1 the current increases as in fig. 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip.flop, FF1, and switches on the outout transistor, Q1. The current increases until the drop on the sensing resistor $R_{\rm S1}$ is equal to $V_{\rm ref1}$ (t_3) and the cycle repeats.

SIGNAL WAVEFORMS

Figure 1. Load current waveform with pin 9 connected to GND.



The switching frequency depends on the value R and C, as shown in fig. 4 and must be chosen in the range 10 to 30 KHz.

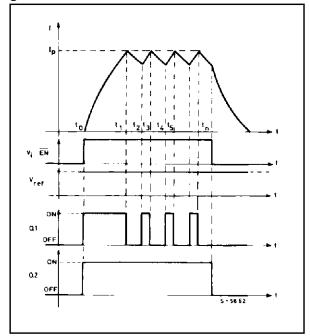
It is possible with external hardware to change the reference voltage V_{ref} in order to obtain a high peak current I_p and a lower holding current I_h (see fig. 3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150°C. The presence of a hysteresis circuit makes the IC workagain aftera fall of the junction temperature of about 20°C.

The analoginput pins (V_{ref1} , V_{ref2}) can be left open or connected to V_{ss} ; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_s :

$$I_p = \frac{2.5}{R_s}$$

Figure 2. Load current waveform with external R-C network connected between pin 9 and ground.



SIGNAL WAVEFORMS (continued)

Figure 3. With V_{ref} changed by hardware.

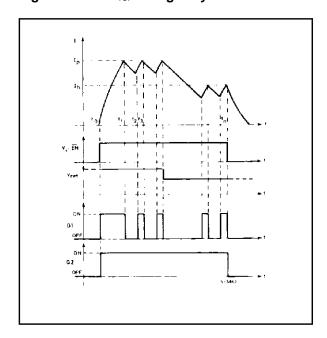
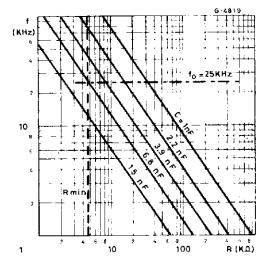
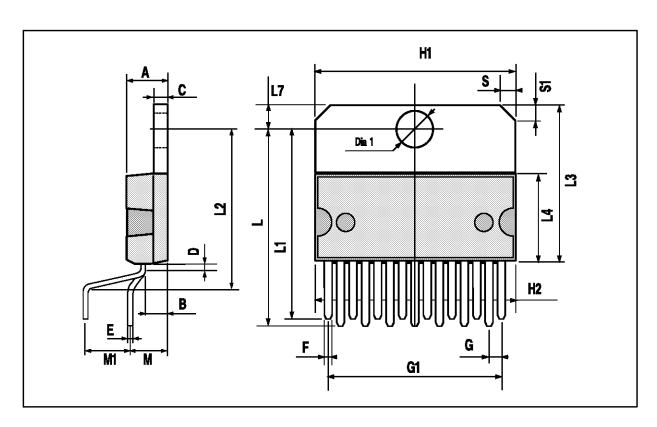


Figure 4. Switching frequency vs. values of R and C.



MULTIWATT15 PACKAGE MECHANICAL DATA

DIM.		mm			inch	
DINI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			5			0.197
В			2.65			0.104
С			1.6			0.063
D		1			0.039	
Е	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
М	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



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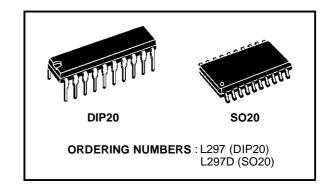
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STEPPER MOTOR CONTROLLERS

- NORMAL/WAWE DRIVE
- HALF/FULL STEP MODES
- CLOCKWISE/ANTICLOCKWISE DIRECTION
- SWITCHMODE LOAD CURRENT REGULA-TION
- PROGRAMMABLE LOAD CURRENT
- FEW EXTERNAL COMPONENTS
- RESET INPUT & HOME OUTPUT
- ENABLE INPUT



DESCRIPTION

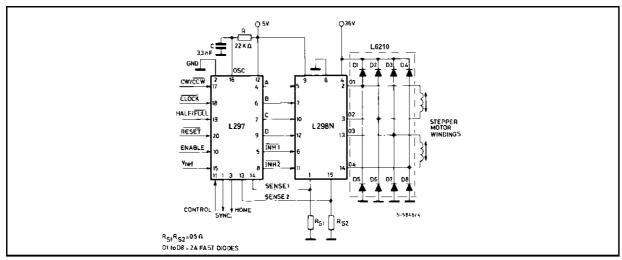
The L297/A/D Stepper Motor Controller IC generates four phase drive signals for two phase bipolar and four phase unipolar step motors in microcomputer-controlled applications. The motor can be driven in half step, normal and wawe drive modes and on-chip PWM chopper circuits permit switchmode control of the current in the windings. A

feature of this device is that it requires only clock, direction and mode input signals. Since the phase are generated internally the burden on the microprocessor, and the programmer, is greatly reduced. Mounted in DIP20 and SO20 packages, the L297 can be used with monolithic bridge drives such as the L298N or L293E, or with discrete transistors and darlingtons.

ABSOLUTE MAXIMUM RATINGS

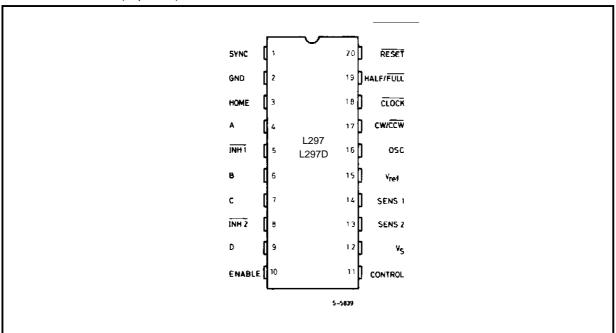
Symbol	Parameter	Value	Unit
Vs	Supply voltage	10	V
Vi	Input signals	7	V
P _{tot}	Total power dissipation (T _{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to + 150	°C

TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT

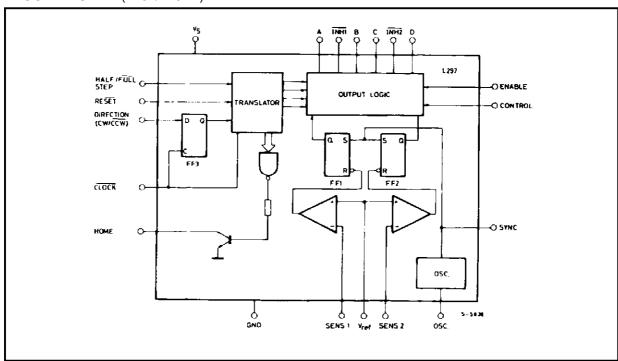


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PIN CONNECTION (Top view)



BLOCK DIAGRAM (L297/L297D)



PIN FUNCTIONS - L297/L297D

N°	NAME	FUNCTION
1	SYNC	Output of the on-chip chopper oscillator. The SYNC connections The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground connection.
3	НОМЕ	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	А	Motor phase A drive signal for power stage.
5	ĪNH1	Active low inhibit control for driver stage of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate load current if CONTROL input is low.
6	В	Motor phase B drive signal for power stage.
7	С	Motor phase C drive signal for power stage.
8	ĪNH2	Active low inhibit control for drive stages of C and D phases. Same functions as INH1.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) INH1, INH2, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on INH1 and INH2; when high chopper acts on phase lines ABCD.
12	Vs	5V supply input.
13	SENS ₂	Input for load current sense voltage from power stages of phases C and D.
14	SENS ₁	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC} , C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations f \cong 1/0.69 RC
17	cw/ ccw	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	CLOCK	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.



PIN FUNCTIONS - L297/L297D (continued)

N°	NAME	FUNCTION
19	HALF/ FULL	Half/full step select input. When high selects half step operation, when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designate state 1).
20	RESET	Reset input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

THERMAL DATA

Symbol	Parameter		SO20	Unit
R _{th-j-amb}	Thermal resistance junction-ambient max	80	100	°C/W

CIRCUIT OPERATION

The L297 is intended for use with a dual bridge driver, quad darlington array or discrete power devices in step motor driving applications. It receives step clock, direction and mode signals from the systems controller (usually a microcomputer chip) and generates control signals for the power stage.

The principal functions are a translator, which generates the motor phase sequences, and a dual PWM chopper circuit which regulates the current in the motor windings. The translator generates three different sequences, selected by the HALF/FULL input. These are normal (two phases energised), wave drive (one phase energised) and half-step (alternately one phase energised/two phases energised). Two inhibit signals are also generated by the L297 in half step and wave drive modes. These signals, which connect directly to the L298's enable inputs, are intended to speed current decay when a winding is de-energised. When the L297 is used to drive a unipolar motor the chopper acts on these lines.

An input called CONTROL determines whether the chopper will act on the phase lines ABCD or the inhibit lines INH1 and INH2. When the phase lines

are chopped the non-active phase line of each pair (AB or CD) is activated (rather than interrupting the line then active). In L297 + L298 configurations this technique reduces dissipation in the load current sense resistors.

A common on-chip oscillator drives the dual chopper. It supplies pulses at the chopper rate which set the two flip-flops FF1 and FF2. When the current in a winding reaches the programmed peak value the voltage across the sense resistor (connected to one of the sense inputs SENS1 or SENS2) equals V_{ref} and the corresponding comparator resets its flip flop, interrupting the drive current until the next oscillator pulse arrives. The peak current for both windings is programmed by a voltage divider on the V_{ref} input.

Ground noise problems in multiple configurations can be avoided by synchronising the chopper oscillators. This is done by connecting all the SYNC pins together, mounting the oscillator RC network on one device only and grounding the OSC pin on all other devices.



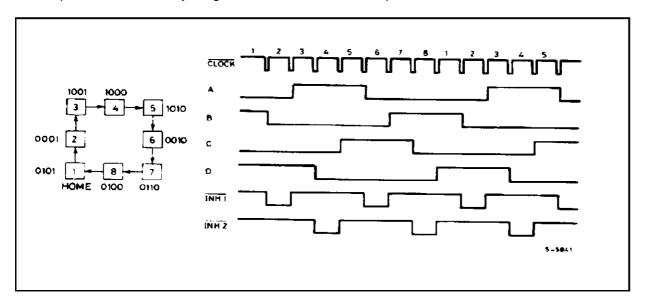
MOTOR DRIVING PHASE SEQUENCES

The L297's translator generates phase sequences for normal drive, wave drive and half step modes. The state sequences and output waveforms for these three modes are shown below. In all cases the translator advances on the low to high transistion of CLOCK.

Clockwise rotation is indicate; for anticlockwise rotation the sequences are simply reversed \overline{RESET} restores the translator to state 1, where ABCD = 0101.

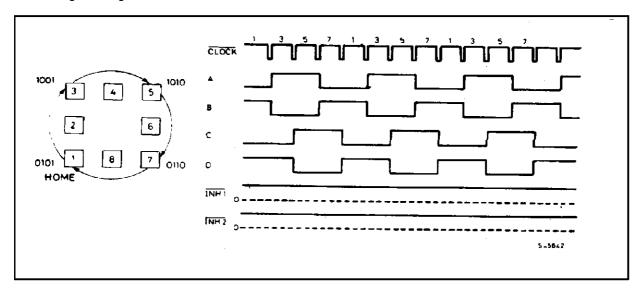
HALF STEP MODE

Half step mode is selected by a high level on the HALF/FULL input.



NORMAL DRIVE MODE

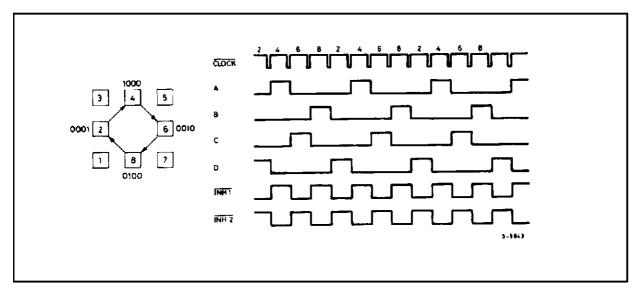
Normal drive mode (also called "two-phase-on" drive) is selected by a low level on the HALF/FULL input when the translator is at an odd numbered state (1, 3, 5 or 7). In this mode the INH1 and INH2 outputs remain high throughout.



MOTOR DRIVING PHASE SEQUENCES (continued)

WAVE DRIVE MODE

Wave drive mode (also called "one-phase-on" drive) is selected by a low level on the HALF/ $\overline{\text{FULL}}$ input when the translator is at an even numbered state (2, 4, 6 or 8).



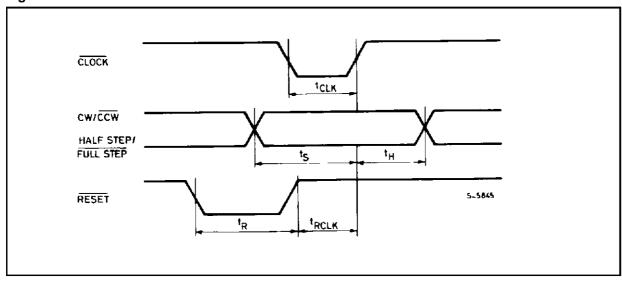
ELECTRICAL CHARACTERISTICS (Refer to the block diagram $T_{amb} = 25^{\circ}C$, $V_s = 5V$ unless otherwise specified)

Symbol	Parameter	Test co	onditions	Min.	Тур	Max.	Unit
Vs	Supply voltage (pin 12)			4.75		7	V
Is	Quiescent supply current (pin 12)	Outputs floating			50	80	mA
Vi	Input voltage		Low			0.6	V
	(pin 11, 17, 18, 19, 20)		High	2		Vs	V
l _i	Input current		$V_i = L$		100	μΑ	
	(pin 11, 17, 18, 19, 20)		V _i = H			10	μΑ
V _{en}	Enable input voltage (pin 10)		Low			1.3	V
			High	2		Vs	V
l _{en}	Enable input current (pin 10)		V _{en} = L			100	μΑ
			V _{en} = H			10	μΑ
Vo	Phase output voltage	I _o = 10mA	V _{OL}			0.4	V
	(pins 4, 6, 7, 9)	$I_0 = 5mA$	V _{OH}	3.9			V
V_{inh}	Inhibit output voltage (pins 5, 8)	I _o = 10mA	V _{inh L}			0.4	V
		I _o = 5mA	V _{inh H}	3.9			V
V _{SYNC}	Sync Output Voltage	I _o = 5mA	V _{SYNC H}	3.3			V
		I _o = 5mA	V _{SYNC} v			0.8	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Тур	Max.	Unit
I _{leak}	Leakage current (pin 3)	V _{CE} = 7 V			1	μΑ
V _{sat}	Saturation voltage (pin 3)	I = 5 mA			0.4	V
V _{off}	Comparators offset voltage (pins 13, 14, 15)	V _{ref} = 1 V			5	mV
lo	Comparator bias current (pins 13, 14, 15)		-100		10	μА
V _{ref}	Input reference voltage (pin 15)		0		3	V
tclk	Clock time		0.5			μs
t _S	Set up time		1			μs
t _H	Hold time		4			μs
t _R	Reset time		1			μs
t _{RCLK}	Reset to clock delay		1			μs

Figure 1.



APPLICATION INFORMATION

TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT

This circuit drives bipolar stepper motors with winding currents up to 2A. The diodes are fast 2A types.

Figure 2.

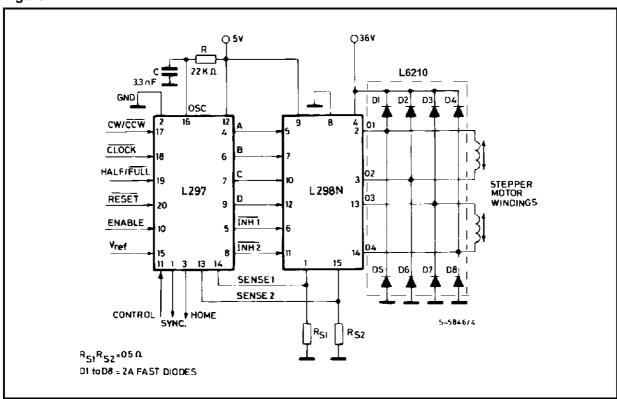
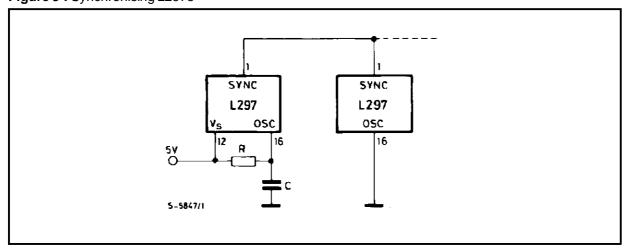
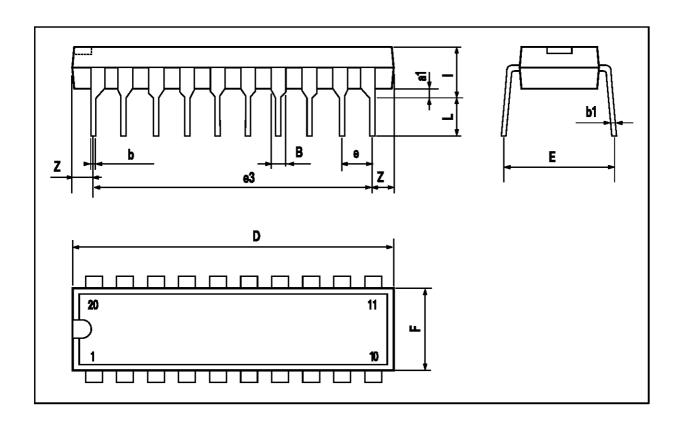


Figure 3: Synchronising L297s



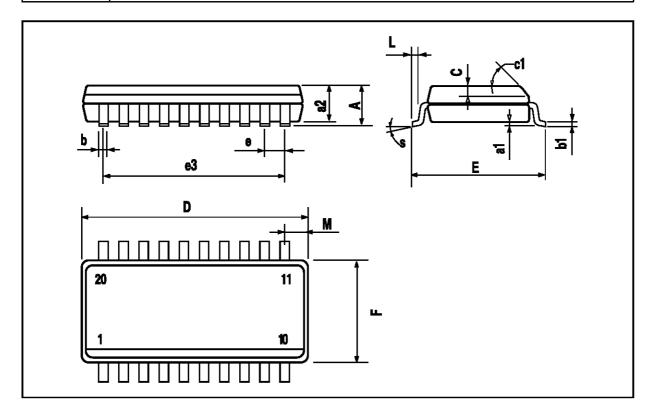
DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
В	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
е		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



SO20 PACKAGE MECHANICAL DATA

DIM.		mm			inch	
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
С		0.5			0.020	
c1			45	(typ.)		
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
е		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
М			0.75			0.030
S		•	8 (r	max.)	•	•



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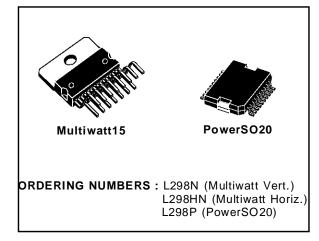


DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)

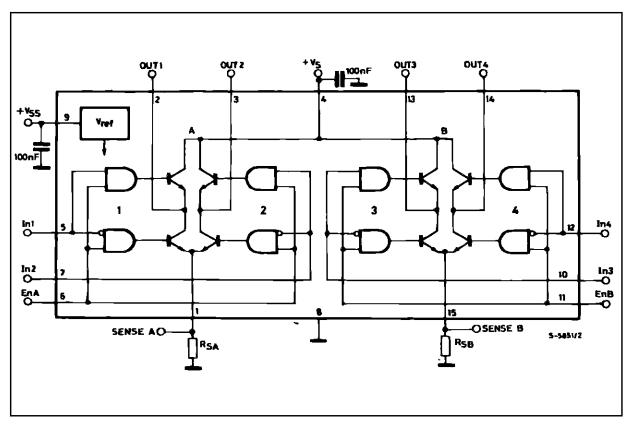
DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the con-



nection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

BLOCK DIAGRAM

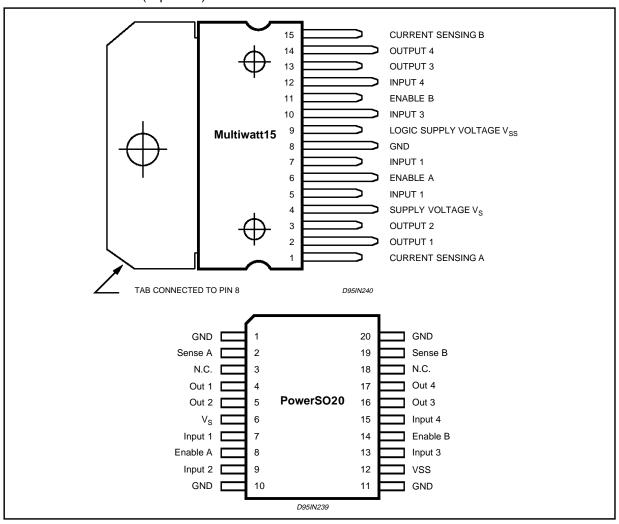


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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Power Supply	50	V
Vss	Logic Supply Voltage	7	V
V _I ,V _{en}	Input and Enable Voltage	-0.3 to 7	V
lo	Peak Output Current (each Channel) – Non Repetitive (t = 100μs) –Repetitive (80% on –20% off; ton = 10ms) –DC Operation	3 2.5 2	A A A
V _{sens}	Sensing Voltage	-1 to 2.3	V
P _{tot}	Total Power Dissipation (T _{case} = 75°C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
R _{th j-case}	Thermal Resistance Junction-case	Max.	ı	3	°C/W
R _{th j-amb}	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

^(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	Vs	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
_	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS ($V_S = 42V$; $V_{SS} = 5V$, $T_j = 25^{\circ}C$; unless otherwise specified)

Symbol	Parameter	Test Condition	ons	Min.	Тур.	Max.	Unit
Vs	Supply Voltage (pin 4)	Operative Condition		V _{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)			4.5	5	7	V
Is	Quiescent Supply Current (pin 4)	$V_{en} = H; I_L = 0$	$V_i = L$ $V_i = H$		13 50	22 70	mA mA
		$V_{en} = L$	$V_i = X$			4	mA
I _{SS}	Quiescent Current from V _{SS} (pin 9)	$V_{en} = H; I_L = 0$	$V_i = L$ $V_i = H$		24 7	36 12	mA mA
		V _{en} = L	$V_i = X$			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)			-0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)			2.3		VSS	V
l _{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	$V_i = L$				-10	μΑ
l _{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	$Vi = H \le V_{SS} - 0.6V$			30	100	μΑ
$V_{en} = L$	Enable Low Voltage (pins 6, 11)			-0.3		1.5	V
$V_{en} = H$	Enable High Voltage (pins 6, 11)			2.3		Vss	V
I _{en} = L	Low Voltage Enable Current (pins 6, 11)	V _{en} = L				-10	μΑ
I _{en} = H	High Voltage Enable Current (pins 6, 11)	$V_{en} = H \le V_{SS} - 0.6V$			30	100	μΑ
V _{CEsat (H)}	Source Saturation Voltage	I _L = 1A I _L = 2A			1.35 2	1.7 2.7	V V
V _{CEsat (L)}	Sink Saturation Voltage	I _L = 1A (5) I _L = 2A (5)			1.2 1.7	1.6 2.3	V V
V _{CEsat}	Total Drop	I _L = 1A (5) I _L = 2A (5)				3.2 4.9	V V
V _{sens}	Sensing Voltage (pins 1, 15)			-1 (1)		2	V



ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
T ₁ (V _i)	Source Current Turn-off Delay	0.5 V _i to 0.9 I _L (2); (4)		1.5		μs
T ₂ (V _i)	Source Current Fall Time	0.9 l _L to 0.1 l _L (2); (4)		0.2		μs
T ₃ (V _i)	Source Current Turn-on Delay	0.5 V _i to 0.1 I _L (2); (4)		2		μs
T ₄ (V _i)	Source Current Rise Time	0.1 l _L to 0.9 l _L (2); (4)		0.7		μs
T ₅ (V _i)	Sink Current Turn-off Delay	0.5 V _i to 0.9 I _L (3); (4)		0.7		μs
T ₆ (V _i)	Sink Current Fall Time	0.9 l _L to 0.1 l _L (3); (4)		0.25		μs
T ₇ (V _i)	Sink Current Turn-on Delay	0.5 V _i to 0.9 I _L (3); (4)		1.6		μs
T ₈ (V _i)	Sink Current Rise Time	0.1 l _L to 0.9 l _L (3); (4)		0.2		μs
fc (V _i)	Commutation Frequency	I _L = 2A		25	40	KHz
T ₁ (V _{en})	Source Current Turn-off Delay	0.5 V _{en} to 0.9 I _L (2); (4)		3		μs
T ₂ (V _{en})	Source Current Fall Time	0.9 l _L to 0.1 l _L (2); (4)		1		μs
T ₃ (V _{en})	Source Current Turn-on Delay	0.5 V _{en} to 0.1 I _L (2); (4)		0.3		μs
T ₄ (V _{en})	Source Current Rise Time	0.1 l _L to 0.9 l _L (2); (4)		0.4		μs
T ₅ (V _{en})	Sink Current Turn-off Delay	0.5 V _{en} to 0.9 I _L (3); (4)		2.2		μs
T ₆ (V _{en})	Sink Current Fall Time	0.9 l _L to 0.1 l _L (3); (4)		0.35		μs
T ₇ (V _{en})	Sink Current Turn-on Delay	0.5 V _{en} to 0.9 I _L (3); (4)		0.25		μs
T ₈ (V _{en})	Sink Current Rise Time	0.1 l _L to 0.9 l _L (3); (4)		0.1		μs
fc (V _{en})	Commutation Frequency	I _L = 2A		1		KHz

^{1) 1)}Sensing voltage can be –1 V for t \leq 50 µsec; in steady state V_{sens} min \geq – 0.5 V.

Figure 1: Typical Saturation Voltage vs. Output Current.

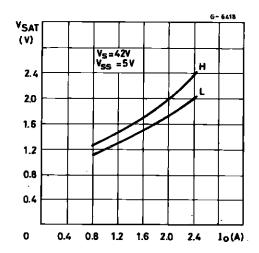
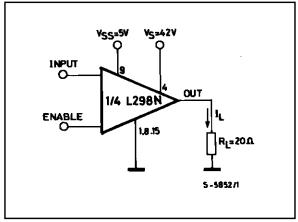


Figure 2: Switching Times Test Circuits.



Note: For INPUT Switching, set EN = HFor ENABLE Switching, set IN = H



²⁾ See fig. 2.

³⁾ See fig. 4.

⁴⁾ The load must be a pure resistor.5) PIN 1 and PIN 15 connected to GND.

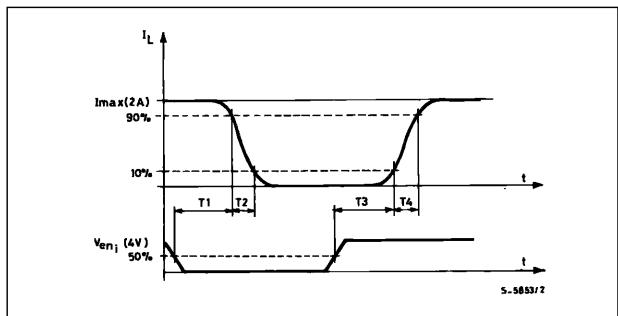
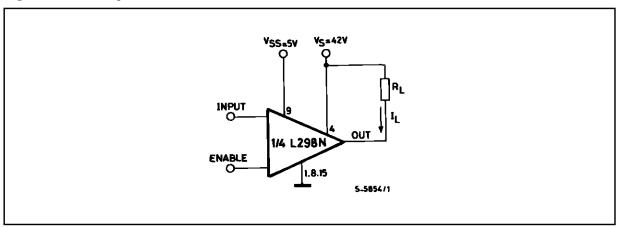
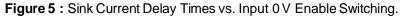


Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

Figure 4: Switching Times Test Circuits.



Note: For INPUT Switching, set EN = H For ENABLE Switching, set IN = L



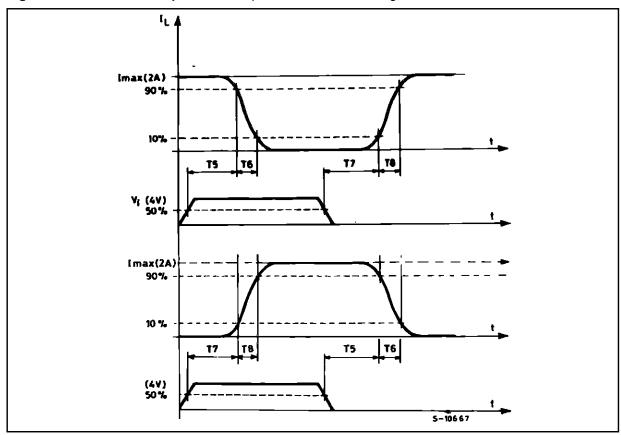
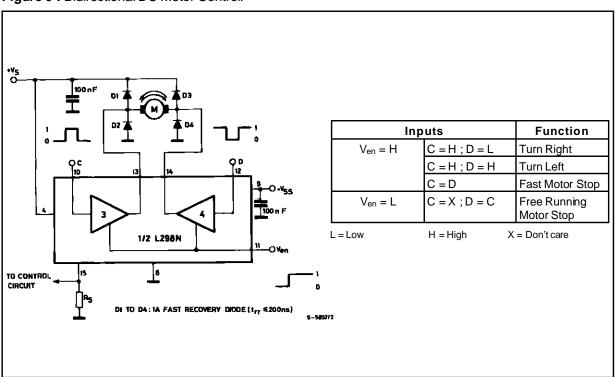


Figure 6: Bidirectional DC Motor Control.



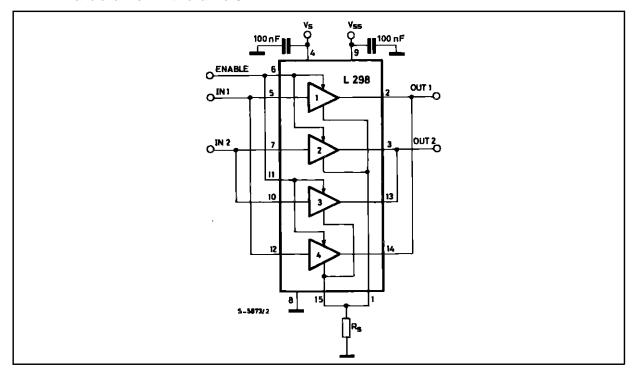


Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.

APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298 integrates two power output stages (A; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output: an external resistor (R_{SA} ; R_{SB} .) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1; In2; EnA and In3; In4; EnB. The In inputs set the bridge state when The En input is high; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to GND pin. When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C. Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off: Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements (trr \leq 200 nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the IC are chopped; Shottky diodes would be preferred.



This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

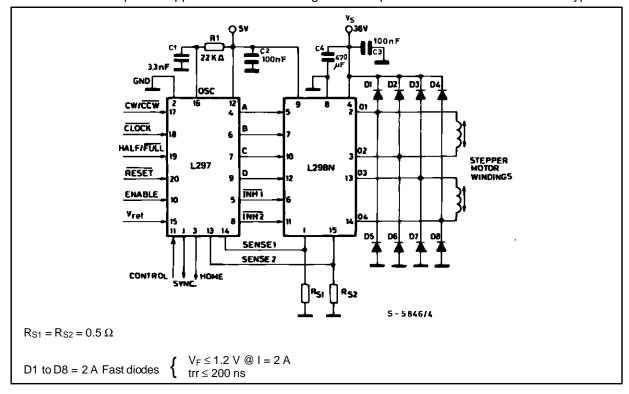
On Fig 8 it is shown the driving of a two phase bipolar stepper motor; the needed signals to drive the inputs of the L298 are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Figure 8: Two Phase Bipolar Stepper Motor Circuit.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



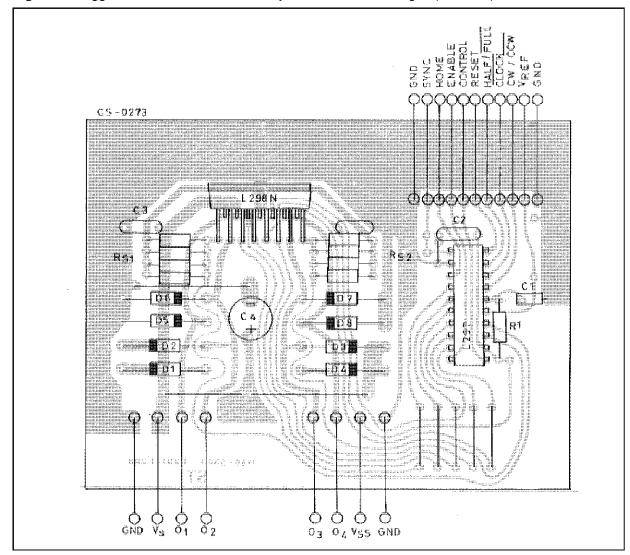
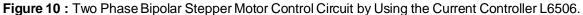
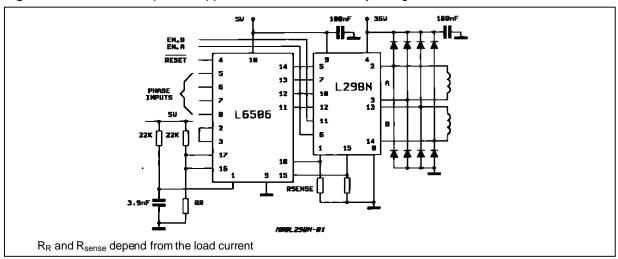


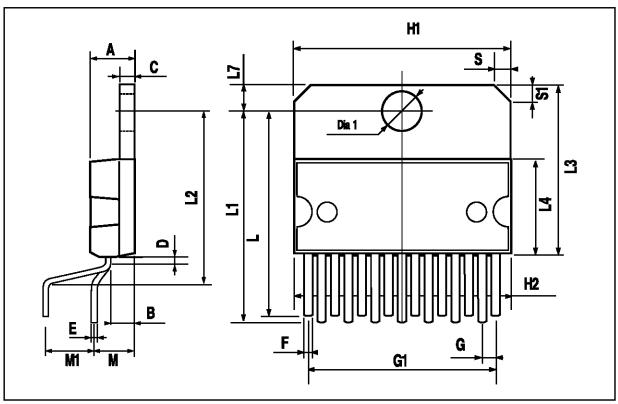
Figure 9: Suggested Printed Circuit Board Layout for the Circuit of fig. 8 (1:1 scale).





MULTIWATT15 (VERTICAL) PACKAGE MECHANICAL DATA

DIM.		mm			inch	
DIIVI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			5			0.197
В			2.65			0.104
С			1.6			0.063
D		1			0.039	
Е	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
М	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

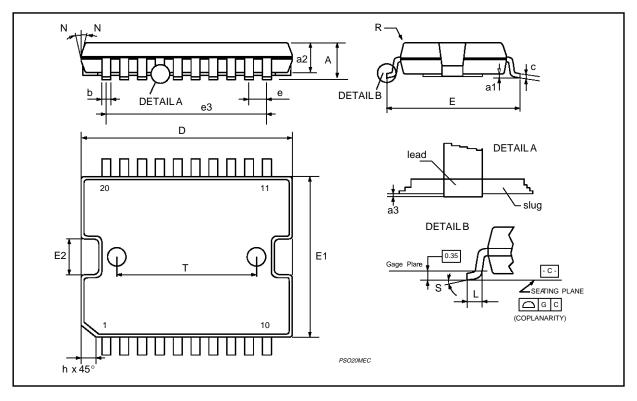


PowerSO20 PACKAGE MECHANICAL DATA

DIM.		mm			inch		
DIW.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α			3.60			0.1417	
a1	0.10		0.30	0.0039		0.0118	
a2			3.30			0.1299	
а3	0		0.10	0		0.0039	
b	0.40		0.53	0.0157		0.0209	
С	0.23		0.32	0.009		0.0126	
D (1)	15.80		16.00	0.6220		0.6299	
E	13.90		14.50	0.5472		0.570	
е		1.27			0.050		
e3		11.43			0.450		
E1 (1)	10.90		11.10	0.4291		0.437	
E2			2.90			0.1141	
G	0		0.10	0		0.0039	
h			1.10				
L	0.80		1.10	0.0314		0.0433	
N		10° (max.)					
S			8° (max.)			
Т		10.0			0.3937		

(1) "D and E1" do not include mold flash or protrusions

- Mold flash or protrusions shall not exceed 0.15mm (0.006")



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L6201 - L6201P L6202 - L6203

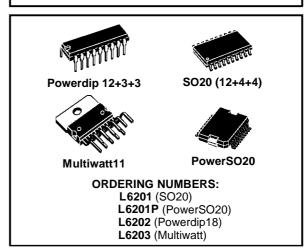
DMOS FULL BRIDGE DRIVER

- SUPPLY VOLTAGE UP TO 48V
- 5A MAX PEAK CURRENT (2A max. for L6201)
- TOTAL RMS CURRENT UP TO L6201: 1A; L6202: 1.5A; L6203/L6201P:4A
- R_{DS (ON)} 0.3 Ω (typical value at 25 °C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100 KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY

DESCRIPTION

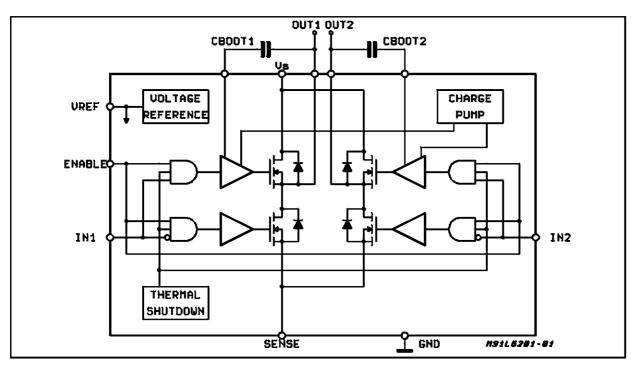
The I.C. is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can operate at supply voltages up to 42V and efficiently at high switch-

MULTIPOWER BCD TECHNOLOGY



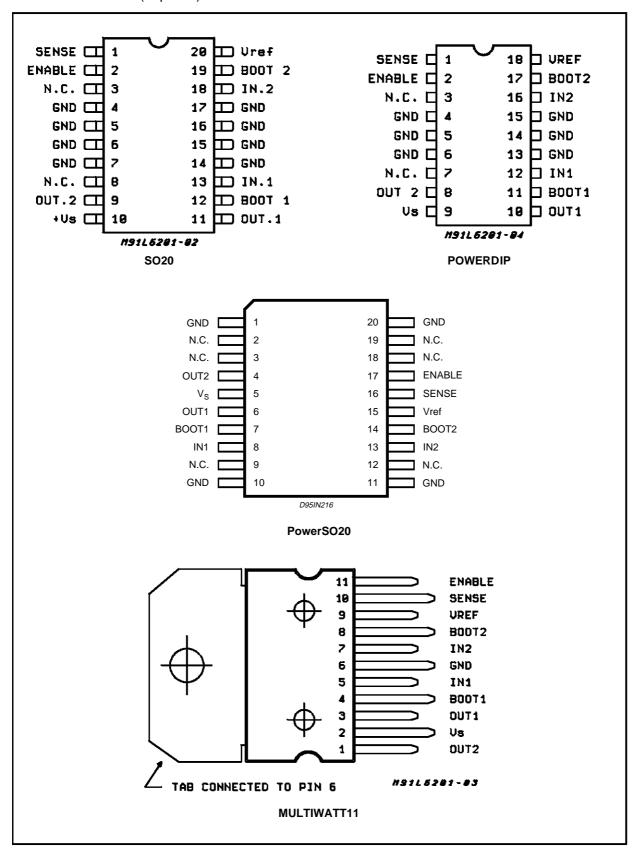
ing speeds. All the logic inputs are TTL, CMOS and μ C compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The I.C. is mounted in three different packages.

BLOCK DIAGRAM



July 1996 1/20

PIN CONNECTIONS (Top view)



PINS FUNCTIONS

	Dev	rice			
L6201	L6201P	L6202	L6203	Name	Function
1	16	1	10	SENSE	A resistor R_{sense} connected to this pin provides feedback for motor current control.
2	17	2	11	ENAB LE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.
3	2,3,9,12, 18,19	3		N.C.	Not Connected
4,5	_	4		GND	Common Ground Terminal
_	1, 10	5	6	GND	Common Ground Terminal
6,7	_	6		GND	Common Ground Terminal
8	_	7		N.C.	Not Connected
9	4	8	1	OUT2	Ouput of 2nd Half Bridge
10	5	9	2	Vs	Supply Voltage
11	6	10	3	OUT1	Output of first Half Bridge
12	7	11	4	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor.
13	8	12	5	IN1	Digital Input from the Motor Controller
14,15	_	13		GND	Common Ground Terminal
_	11, 20	14	6	GND	Common Ground Terminal
16,17	_	15		GND	Common Ground Terminal
18	13	16	7	IN2	Digital Input from the Motor Controller
19	14	17	8	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor.
20	15	18	9	V _{ref}	Internal voltage reference. A capacitor from this pin to GND is recommended. The internal Ref. Voltage can source out a current of 2mA max.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Power Supply	52	V
V _{OD}	Differential Output Voltage (between Out1 and Out2)	60	V
V _{IN} , V _{EN}	Input or Enable Voltage	- 0.3 to + 7	V
l _o	Pulsed Output Current for L6201P/L6202/L6203 (Note 1) - Non Repetitive (< 1 ms) for L6201 for L6201P/L6202/L6203 DC Output Current for L6201 (Note 1)	5 5 10 1	A A A
V _{sense}	Sensing Voltage	- 1 to + 4	V
V _b	Boostrap Peak Voltage	60	V
P _{tot}	Total Power Dissipation: T _{pins} = 90°C for L6201 for L6202 T _{case} = 90°C for L6201P/L6203 T _{amb} = 70°C for L6201 (Note 2) for L6202 (Note 2) for L6201P/L6203 (Note 2)	4 5 20 0.9 1.3 2.3	W W W W W
T _{stg} , T _j	Storage and Junction Temperature	- 40 to + 150	°C

Note 1: Pulse width limited only by junction temperature and transient thermal impedance (see thermal characteristics) **Note 2:** Mounted on board with minimized dissipating copper area.



THERMAL DATA

Symbol	Parameter			Val	ue		Unit
Syllibol	r ai ailietei		L6201	L6201P	L6202	L6203	Ollit
Rt _{h j-pins}	Thermal Resistance Junction-pins	max	15	_	12	-	
Rt _{h i-case}	Thermal Resistance Junction Case	max.	_	_	_	3	°C/W
Rt _{h j-amb}	Thermal Resistance Junction-ambient	max.	85	13 (*)	60	35	

^(*) Mounted on aluminium substrate.

ELECTRICAL CHARACTERISTICS (Refer to the Test Circuits; $T_j = 25^{\circ}C$, $V_S = 42V$, $V_{sens} = 0$, unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Vs	Supply Voltage		12	36	48	V
V_{ref}	Reference Voltage	I _{REF} = 2mA		13.5		V
I _{REF}	Output Current				2	mA
Is	Quiescent Supply Current			10 10 8	15 15 15	mA mA mA
fc	Commutation Frequency (*)			30	100	KHz
Tj	Thermal Shutdown			150		∘C
T _d	Dead Time Protection			100		ns

TRANSISTORS

OFF							
I _{DSS}	Leakage Current	Fig. 11 V _s = 52 V			1	mA	
ON	ON						
R _{DS}	On Resistance	Fig. 4,5		0.3	0.55	Ω	
V _{DS(ON)}	Drain Source Voltage	Fig. 9 I _{DS} = 1A I _{DS} = 1.2A I _{DS} = 3A L6201 L6202 L6201P/03		0.3 0.36 0.9		>>>	
V _{sens}	Sensing Voltage		– 1		4	V	

SOURCE DRAIN DIODE

V _{sd}	Forward ON Voltage	Fig. 6a and b I _{SD} = 1A	0.9 (**) 0.9 (**) 1.35(**)	>>>
t _{rr}	Reverse Recovery Time	$\begin{aligned} \frac{dif}{dt} &= 25 \text{ A/}\mu\text{s} \\ I_F &= 1A & L6201 \\ I_F &= 1.2A & L6202 \\ I_F &= 3A & L6203 \end{aligned}$	300	ns
t _{fr}	Forward Recovery Time		200	ns

LOGIC LEVELS

V _{IN L} , V _{EN L}	Input Low Voltage		- 0.3		0.8	V
V _{IN H} , V _{EN H}	Input High Voltage		2		7	V
I _{IN L} , I _{EN L}	Input Low Current	$V_{IN}, V_{EN} = L$			-10	μΑ
I _{IN H} , I _{EN H}	Input High Current	$V_{IN}, V_{EN} = H$		30		μΑ

ELECTRICAL CHARACTERISTICS (Continued)

LOGIC CONTROL TO POWER DRIVE TIMING

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t ₁ (V _i)	Source Current Turn-off Delay	Fig. 12		300		ns
t ₂ (V _i)	Source Current Fall Time	Fig. 12		200		ns
t ₃ (V _i)	Source Current Turn-on Delay	Fig. 12		400		ns
t ₄ (V _i)	Source Current Rise Time	Fig. 12		200		ns
t ₅ (V _i)	Sink Current Turn-off Delay	Fig. 13		300		ns
t ₆ (V _i)	Sink Current Fall Time	Fig. 13		200		ns
t ₇ (V _i)	Sink Current Turn-on Delay	Fig. 13		400		ns
t ₈ (V _i)	Sink Current Rise Time	Fig. 13		200		ns

Figure 1: Typical Normalized Is vs. Tj

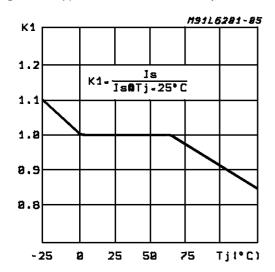


Figure 3: Typical Normalized Is vs. Vs

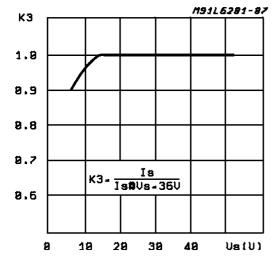


Figure 2: Typical Normalized Quiescent Current

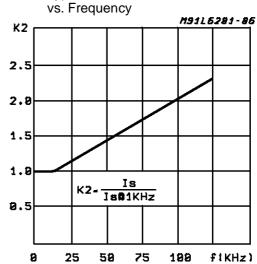
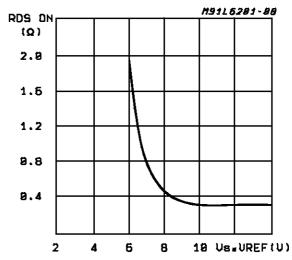


Figure 4: Typical R_{DS (ON)} vs. V_S ~ V_{ref}



^(*) Limited by power dissipation (**) In synchronous rectification the drain-source voltage drop VDS is shown in fig. 4 (L6202/03); typical value for the L6201 is of 0.3V.

Figure 5: Normalized R_{DS} (ON)at 25°C vs. Temperature Typical Values

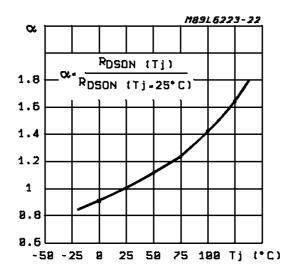


Figure 6a: Typical Diode Behaviour in Synchronous Rectification (L6201)

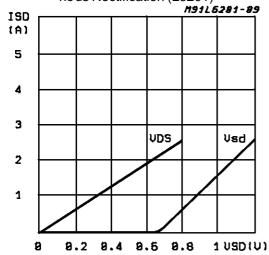


Figure 6b: Typical Diode Behaviour in Synchronous Rectification (L6201P/02/03)

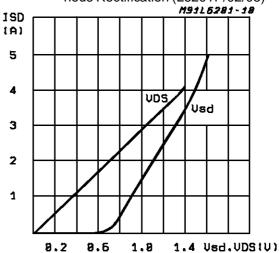


Figure 7a: Typical Power Dissipation vs IL (L6201)

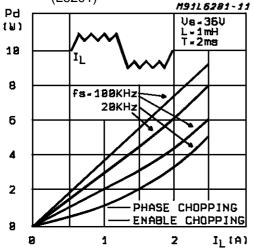


Figure 7b: Typical Power Dissipation vs IL

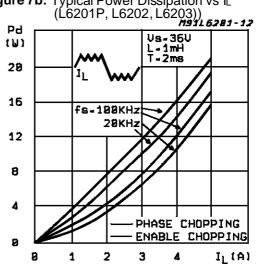


Figure 8a: Two Phase Chopping

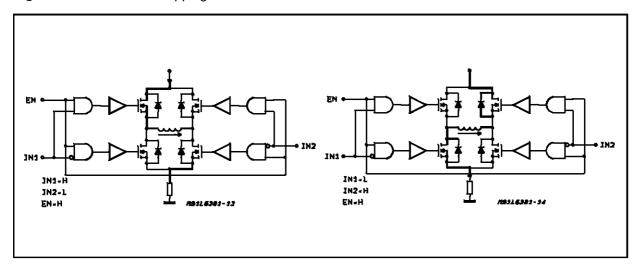


Figure 8b: One Phase Chopping

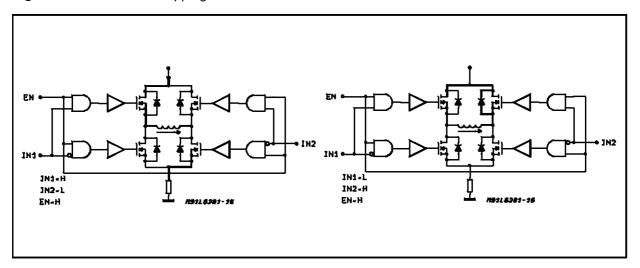
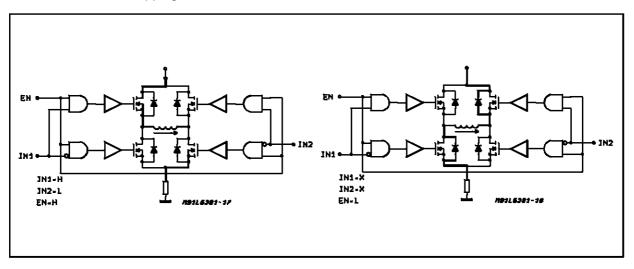


Figure 8c: Enable Chopping



TEST CIRCUITS

Figure 9: Saturation Voltage

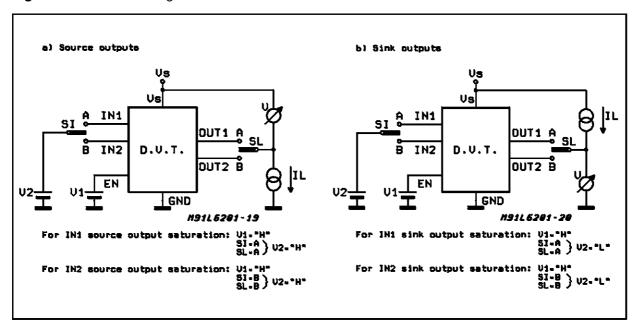


Figure 10: Quiescent Current

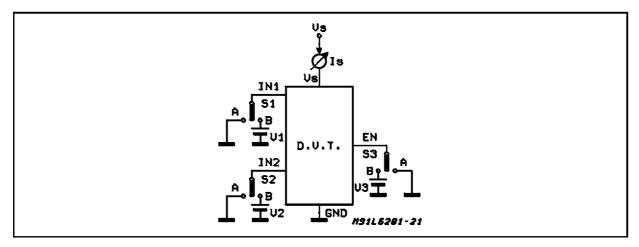


Figure 11: Leakage Current

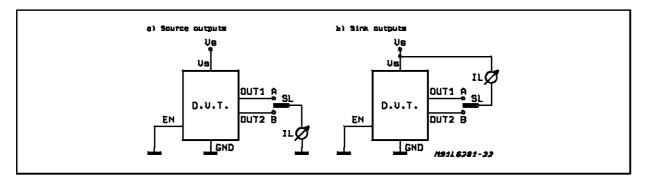


Figure 12: Source Current Delay Times vs. Input Chopper

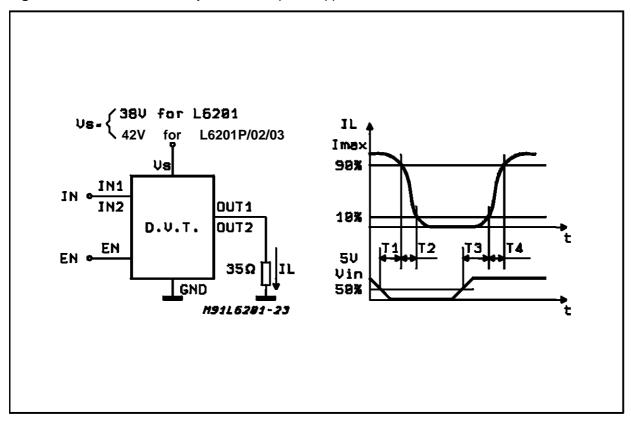
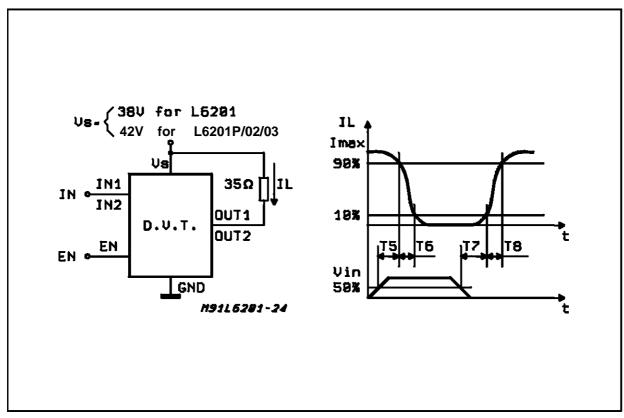


Figure 13: Sink Current Delay Times vs. Input Chopper



CIRCUIT DESCRIPTION

The L6201/1P/2/3 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components. The Logic Drive is shown in table 1.

Table 1

In	puts		
	IN1	IN2	Output Mosfets (*)
V _{EN} = H		LHLH	Sink 1, Sink 2 Sink 1, Source 2 Source 1, Sink 2 Source 1, Source 2
$V_{EN} = L$	Х	Х	All transistors turned oFF

 $\label{eq:Lagrangian} \begin{array}{ll} L = Low & H = High & X = DON't \ care \\ (*) \ Numbers \ referred \ to \ INPUT1 \ or \ INPUT2 \ controlled \ output \ stages \end{array}$

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor (fig. 15).

Figure 14: Intrinsic Structures in the POWER DMOS Transistors

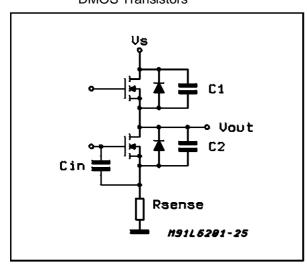
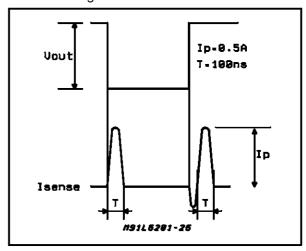


Figure 15: Current Typical Spikes on the Sensing Pin



TRANSISTOR OPERATION

ON State

When one of the POWER DMOS transistor is ON it can be considered as a resistor R_{DS} (ON) throughout the recommended operating range. In this condition the dissipated power is given by :

$$P_{ON} = R_{DS}(ON) \cdot I_{DS}^2(RMS)$$

The low R_{DS} (ON) of the Multipower-BCD process can provide high currents with low power dissipation.

OFF State

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by :

The power dissipation is very low and is negligible in comparison to that dissipated in the ON STATE.

Transitions

As already seen above the transistors have an intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is RDS (ON) · ID and when it reaches the diode forward voltage it is clamped. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage-current waveforms and in the driving mode. (see Fig. 7ab and Fig. 8abc).

 $P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$

Boostrap Capacitors

To ensure that the POWER DMOS transistors are driven correctly gate to source voltage of typ. 10 V must be guaranteed for all of the N-channel DMOS transistors. This is easy to be provided for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. This is achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1 nF. It is recommended that a capacitance of at least 10 nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher RDS (ON). On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

Reference Voltage

To by-pass the internal Ref. Volt. circuit it is recommended that a capacitor be placed between its pin and ground. A value of 0.22 μ F should be sufficient for most applications. This pin is also protected against a short circuit to ground: a max. current of 2mA max. can be sinked out.

Dead Time

To protect the device against simultaneous conduction in both arms of the bridge resulting in a rail to rail short circuit, the integrated logic control provides a dead time greater than 40 ns.

Thermal Protection

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150 °C. When the temperature has fallen to a safe level the device restarts the input and enable signals under control.

APPLICATION INFORMATION

Recirculation

During recirculation with the ENABLE input high, the voltage drop across the transistor is RDS (ON)- IL, clamped at a voltage depending on the characteristics of the source-drain diode. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problem because the voltage spike generated on the sense resistor is masked by the current controller circuit.

Rise Time T_r (See Fig. 16)

When a diagonal of the bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r . The dissipated energy $E_{OFF/ON}$ is in this case :

$$EOFF/ON = [RDS(ON) \cdot IL^2 \cdot T_r] \cdot 2/3$$

Load Time T_{LD} (See Fig.16)

During this time the energy dissipated is due to the ON resistance of the transistors (E_{LD}) and due to commutation (E_{COM}). As two of the POWER DMOS transistors are ON, E_{ON} is given by :

$$E_{LD} = I_L^2 \cdot R_{DS} (ON) \cdot 2 \cdot T_{LD}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_S \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{LD}$$

Where:

 $T_{COM} = T_{TURN-ON} = T_{TURN-OFF}$

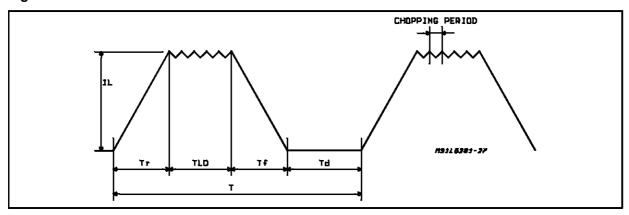
fswitch = Chopping frequency.

Fall Time T_f (See Fig. 16)

It is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time :

$$E_{ON/OFF} = [R_{DS}(ON) \cdot I_L^2 \cdot T_f] \cdot 2/3$$

Figure 16.



Quiescent Energy

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

Equiescent = Iquiescent $\cdot V_s \cdot T$

Total Energy Per Cycle

ETOT = EOFF/ON + ELD + ECOM + + EON/OFF + EQUIESCENT

The Total Power Dissipation PDIS is simply:

 $P_{DIS} = E_{TOT}/T$

 T_r = Rise time

 T_{LD} = Load drive time

 $T_f = Fall time$

 $T_d = Dead time$

T = Period

 $T = T_r + T_{LD} + T_f + T_d$

DC Motor Speed Control

Since the I.C. integrates a full H-Bridge in a single package it is idealy suited for controlling DC motors. When used for DC motor control it performs the power stage required for both speed and direction control. The device can be combined with a current regulator like the L6506 to implement a transconductance amplifier for speed control, as shown in figure 17. In this particular configuration only half of the L6506 is used and the other half of the device may be used to control a second

motor.

The L6506 senses the voltage across the sense resistor R_S to monitor the motor current: it compares the sensed voltage both to control the speed and during the brake of the motor.

Between the sense resistor and each sense input of the L6506 a resistor is recommended; if the connections between the outputs of the L6506 and the inputs of the L6203 need a long path, a resistor must be added between each input of the L6203 and ground.

A snubber network made by the series of R and C must be foreseen very near to the output pins of the I.C.; one diode (BYW98) is connected between each power output pin and ground as well.

The following formulas can be used to calculate the snubber values:

 $R \cong V_S/I_D$

 $C = I_p/(dV/dt)$ where:

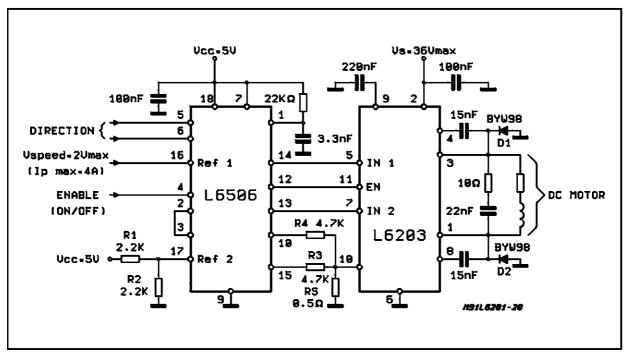
Vs is the maximum Supply Voltage foreseen on the application;

Ip is the peak of the load current;

dv/dt is the limited rise time of the output voltage (200V/µs is generally used).

If the Power Supply Cannot Sink Current, a suitable large capacitor must be used and connected near the supply pin of the L6203. Sometimes a capacitor at pin 17 of the L6506 let the application better work. For motor current up to 2A max., the L6202 can be used in a similar circuit configuration for which a typical Supply Voltage of 24V is recommended.

Figure 17: Bidirectional DC Motor Control



BIPOLAR STEPPER MOTORS APPLICATIONS

Bipolar stepper motors can be driven with one L6506 or L297, two full bridge BCD drivers and very few external components. Together these three chips form a complete microprocessor-to-stepper motor interface is realized.

As shown in Fig. 18 and Fig. 19, the controller connect directly to the two bridge BCD drivers. External component are minimalized: an R.C. network to set the chopper frequency, a resistive divider (R1; R2) to establish the comparator reference voltage and a snubber network made by R and C in series (See DC Motor Speed Control).

Figure 18: Two Phase Bipolar Stepper Motor Control Circuit with Chopper Current Control

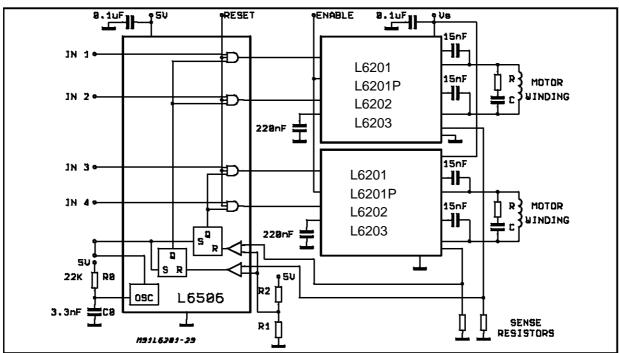
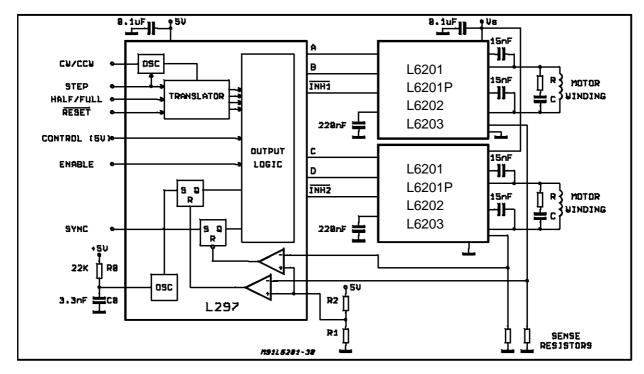
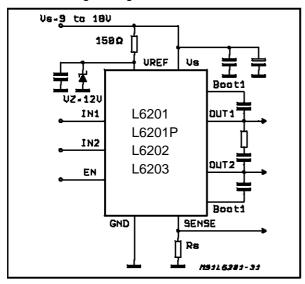


Figure 19: Two Phase Bipolar Stepper Motor Control Circuit with Chopper Current Control and Translator



It could be requested to drive a motor at V_S lower than the minimum recommended one of 12V (See Electrical Characteristics); in this case, by accepting a possible small increas in the RDS (ON) resistance of the power output transistors at the lowest Supply Voltage value, may be a good solution the one shown in Fig. 20.

Figure 20: L6201/1P/2/3Used at a Supply Voltage Range Between 9 and 18V



THERMAL CHARACTERISTICS

Thanks to the high efficiency of this device, often a true heatsink is not needed or it is simply obtained by means of a copper side on the P.C.B. (L6201/2).

Under heavy conditions, the L6203 needs a suitable cooling.

By using two square copper sides in a similar way as it shown in Fig. 23, Fig. 21 indicates how to choose the on board heatsink area when the L6201 total power dissipation is known since:

$$R_{Th j-amb} = (T_{j max.} - T_{amb max}) / P_{tot}$$

Figure 22 shows the Transient Thermal Resistance vs. a single pulse time width.

Figure 23 and 24 refer to the L6202.

For the Multiwatt L6203 addition information is given by Figure 25 (Thermal Resistance Junction-Ambient vs. Total Power Dissipation) and Figure 26 (Peak Transient Thermal Resistance vs. Repetitive Pulse Width) while Figure 27 refers to the single pulse Transient Thermal Resistance.

Figure 21: Typical RTh J-amb vs. "On Board" Heatsink Area (L6201)

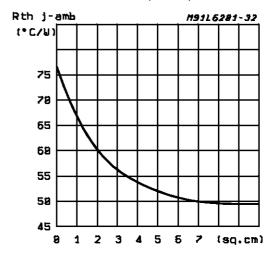
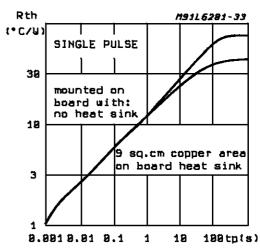


Figure 22: Typical Transient R_{TH} in Single Pulse Condition (L6201)



Figurre 23: Typical R_{Th J-amb} vs. Two "On Board" Square Heatsink (L6202)

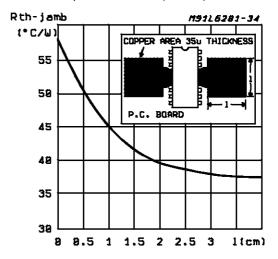


Figure 24: Typical Transient Thermal Resistance for Single Pulses (L6202)

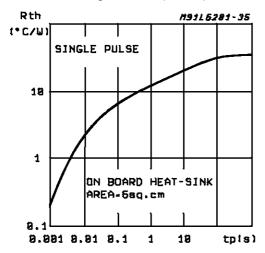


Figure 26: Typical Transient Thermal Resistance for Single Pulses with and without Heatsink (L6203)

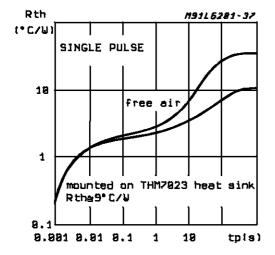


Figure 25: Typical R_{Th J-amb} of Multiwatt Package vs. Total Power Dissipation

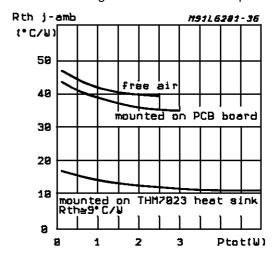
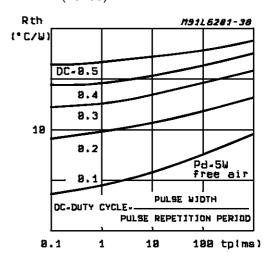
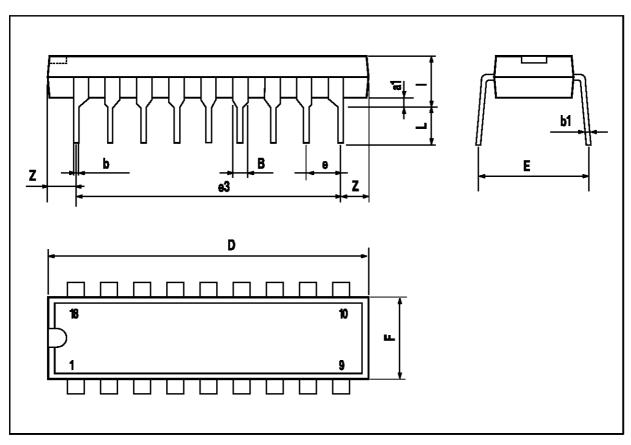


Figure 27: Typical Transient Thermal Resistance versus Pulse Width and Duty Cycle (L6203)



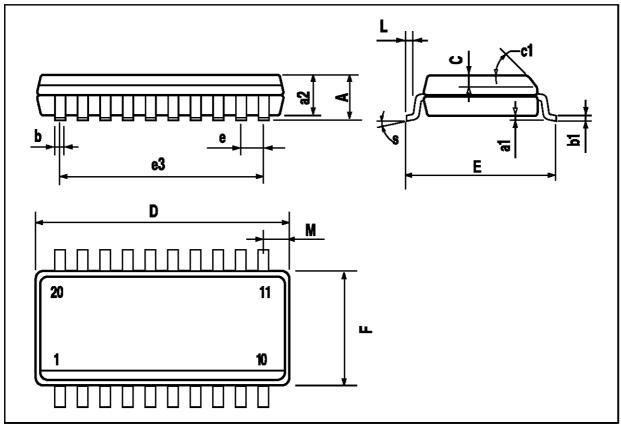
POWERDIP18 PACKAGE MECHANICAL DATA

DIM.		mm		inch		
J	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
Е		8.80			0.346	
е		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100



SO20 PACKAGE MECHANICAL DATA

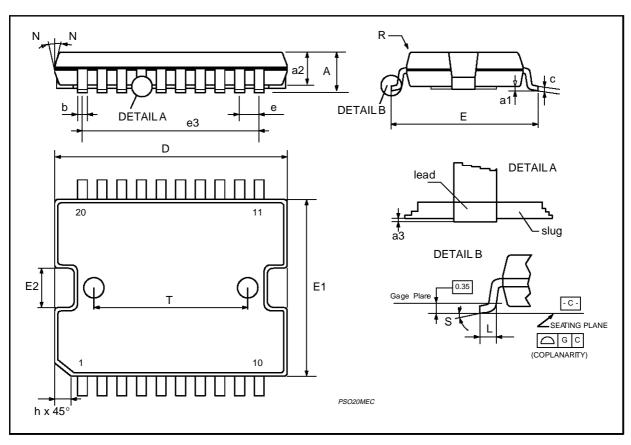
DIM.		mm		inch		
DIW.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
С		0.5			0.020	
c1			45 ((typ.)		
D	12.6		13.0	0.496		0.512
Е	10		10.65	0.394		0.419
е		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
М			0.75			0.030
S			8 (n	nax.)		



PowerSO20 PACKAGE MECHANICAL DATA

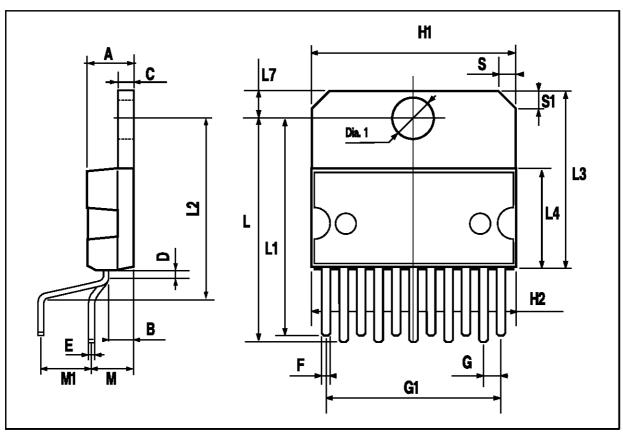
DIM.	mm			inch		
DIW.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
а3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
С	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.6220		0.6299
Е	13.90		14.50	0.5472		0.570
е		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.90		11.10	0.4291		0.437
E2			2.90			0.1141
G	0		0.10	0		0.0039
h			1.10			
L	0.80		1.10	0.0314		0.0433
N	10° (max.)					
S		8° (max.)				
Т		10.0			0.3937	

^{(1) &}quot;D and E1" do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (0.006")



MULTIWATT11 PACKAGE MECHANICAL DATA

DIM	mm			inch		
DIM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			5			0.197
В			2.65			0.104
С			1.6			0.063
D		1			0.039	
Е	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.57	1.7	1.83	0.062	0.067	0.072
G1	16.87	17	17.13	0.664	0.669	0.674
H1	19.6			0.772		
H2			20.2			0.795
L	21.5		22.3	0.846		0.878
L1	21.4		22.2	0.843		0.874
L2	17.4		18.1	0.685		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.1	4.3	4.5	0.161	0.169	0.177
M1	4.88	5.08	5.3	0.192	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



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STEPPER MOTOR DRIVER

ADVANCE DATA

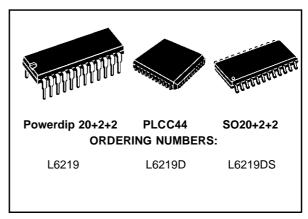
- ABLE TO DRIVE BOTH WINDINGS OF BIPO-LAR STEPPER MOTOR
- OUTPUT CURRENT UP TO 750mA EACH WINDING
- WIDE VOLTAGE RANGE 10V TO 46V
- HALF-STEP, FULL-STEP AND MICROSTEPP-ING MODE
- BUILT-IN PROTECTION DIODES
- INTERNAL PWM CURRENT CONTROL
- LOW OUTPUT SATURATION VOLTAGE
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- INTERNAL THERMAL SHUTDOWN

DESCRIPTION

The L6219 is a bipolar monolithic integrated circuits intended to control and drive both winding of a bipolar stepper motor or bidirectionally control two DC motors.

The L6219 with a few external components form a complete control and drive circuit for LS-TTL or microprocessor controlled stepper motor system. The power stage is a dual full bridge capable of sustaining 46V and including four diodes for current recirculation.

A cross conduction protection is provided to avoid



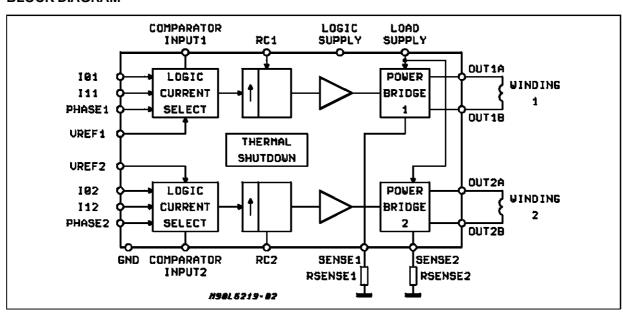
simultaneous cross conduction during switching current direction.

An internal pulse-width-modulation (PWM) controls the output current to 750mA with peak start-up current up to 1A.

Wide range of current control from 750mA (each bridge) is permitted by means of two logic inputs and an external voltage reference. A phase input to each bridge determines the load current direction.

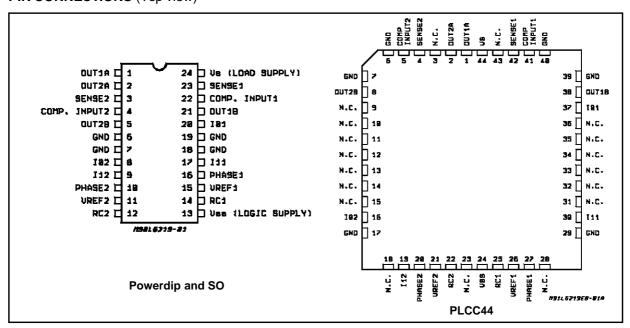
A thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

BLOCK DIAGRAM



September 1995 1/10

PIN CONNECTIONS (Top view)



PIN FUNCTIONS

PLCC (*)	PDIP & SO	Name	Function
1;2	1;2	OUTPUT A	See pins 5;21
4;42	3;23	SENSE RESISTOR	Connection to Lower Emitters of Output Stage for Insertion of Current Sense Resistor
5;41	4;22	COMPARATOR INPUT	Input connected to the comparators. The voltage across the sense resistor is feedback to this input throught the low pass filter RC CC. The higher power transistors are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by $R_T C_T$ ($t_{off} = 1.1 R_T C_T$). See fig. 1.
8;38	5;21	OUTPUT B	Output Connection. The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
6;7;17	6;19	GROUND	See pins 7;18
29;39; 40	7;18	GROUND	Ground Connection. With pins 6 and 19 also conducts heat from die to printed circuit copper.
16;37	8;20	INPUT 0	See INPUT 1 (pins 9;17)
19;30	9;17	INPUT 1	These pins and pins 8;20 (INPUT 0) are logic inputs which select the outputs of the comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See Funcional Description.
20;27	10;16	PHASE	This TTL-compatible logic inputs sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
21;26	11;15	REFERENCE VOLTAGE	A voltage applied to this pin sets the reference voltage of the comparators, this determining the output current (also thus depending on R_s and the two inputs INPUT 0 and INPUT 1).
22;25	12;14	RC	A parallel RC network connected to this pin sets the OFF time of the higher power transistors. The pulse generator is a monostable triggered by the output of the comparators ($t_{off} = 1.1 R_T C_T$).
24	13	V _{ss} - LOGIC SUPPLY	Supply Voltage Input for Logic Circuitry
44	24	Vs - LOAD SUPPLY	Supply Voltage Input for the Output Stages.

(*) Pins: 3, 9,10,11,12,13,14,15,1823,28,31,32,3334,35,36,43 are Not Connected. Note: ESD on GND, V_S , V_{SS} , OUT 1A and OUT 2A is guaranteed up to 1.5KV (Human Body Model, 1500 Ω , 100pF).



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage	50	V
Io	Output Current (peak)	±1	Α
Io	Output Current (continuous)	±0.75	Α
Vss	Logic Supply Voltage	7	V
V _{IN}	Logic Input Voltage Range	-0.3 to +7	V
V _{sense}	Sense Output Voltage	1.5	V
TJ	Junction Temperature	+150	°C
T _{op}	Operating Temperature Range	0 to 70	°C
T _{stg}	Storage Temperature Range	-55 to +150	°C

THERMAL DATA

Symbol	Description		PDIP	so	Unit
R _{thj-case}	Thermal Resistance Junction-case Max. Thermal Resistance Junction-ambient Max.	12	14	15	°C/W
R _{thj-amb}		45 (*)	60 (*)	75 (*)	°C/W

^(*) With minimized copper area.

ELECTRICAL CHARACTERISTICS ($T_j = 25$ °C, $V_S = 46$ V, $V_{SS} = 4.75$ V to 5.25V, $V_{REF} = 5$ V; unless otherwise specified) See fig. 3.

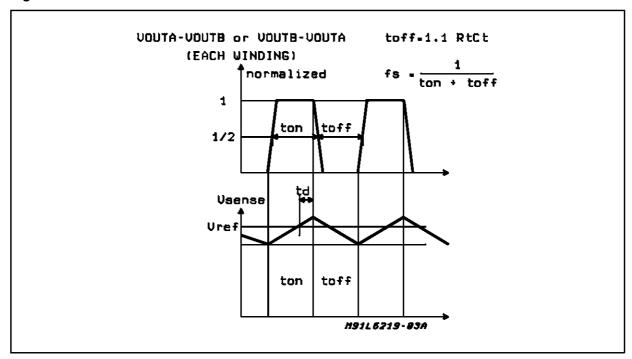
Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Unit
OUTPUT D	RIVERS (OUT _A or OUT _B)					
Vs	Motor Supply Range		10		46	V
I _{CEX}	Output Leakage Current	V _{OUT} = Vs V _{OUT} = 0	-	<1 <-1	50 -50	μA μA
V _{CE(sat)}	Output Saturation Voltage	Sink Driver, IouT = +500mA Sink Driver, IouT = +750mA Source Driver, IouT = -500mA Source Driver, IouT = -750mA		0.3 0.7 1.1 1.3	0.6 1 1.4 1.6	V V V
I_R	Clamp Diode Leakage Current	VR = 50V	-	<1	50	μΑ
V _F	Clamp Diode Forward Voltage	Sink Diode Source Diode IF =750mA		1 1	1.5 1.5	V
I _{S(on)}	Driver Supply Current	Both Bridges ON, No Load	-	8	15	mA
I _{S(off)}	Driver Supply Current	Both Bridges OFF	-	6	10	mA
CONTROL	LOGIC					
V _{IN(H)}	Input Voltage	All Inputs	2.4	-	-	V
$V_{IN(L)}$	Input Voltage	All Inputs	-	-	0.8	V
I _{IN(H)}	Input Current	VIN = 2.4V	-	<1	20	μΑ
I _{IN(L)}	Input Current	VIN = 0.84V	-	-3	-200	μΑ
V_{REF}	Reference Voltage	Operating	1.5	-	7.5	V
I _{SS(ON)}	Total Logic Supply Current	$I_0 = I_1 = 0.8V$, No Load	-	64	74	mA
I _{SS(OFF)}	Total Logic Supply Current	$I_0 = I_1 = 2.4V$, No Load	-	10	14	mA
COMPARA	TORS					
V _{REF} / V _{sense}	Current Limit Threshold (at trip	$I_0 = I_1 = 0.8V$	9.5	10	10.5	-
	point	I ₀ = 2.4V, I ₁ = 0.8V	13.5	15	16.5	
		$I_0 = 0.8V, I_1 = 2.4V$	25.5	30	34.5	-
t _{off}	Cutoff Time	Rt = $56K\Omega$ C _t = $820pF$	-	50		μς
t _d	Turn Off Delay	Fig. 1	-	1		μs



ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter Test Condition		Min.	Тур.	Max.	Unit	
PROTECTION	PROTECTION						
TJ	Thermal Shutdown Temperature		-	170	-	°C	

Figure 1



FUNCTIONAL DESCRIPTION

The circuit is intended to drive both windings of a bipolar stepper motor.

The peak current control is generated through switch mode regulation.

There is a choice of three different current levels with the two logic inputs I_{01} - I_{11} for winding 1 and I_{02} - I_{12} for winding 2.

The current can also be switched off completely

Input Logic (I₀ and I₁)

The current level in the motor winding is selected with these inputs. (See fig. 2)

If any of the logic inputs is left open, the circuit will treat it has a high level input.

I _o	I ₁	Current Level
ГІГІ	H L	No Current Low Current 1/3 I _o max Medium Current 2/3 I _o max Maximum Current I _o max

Phase

This input determines the direction of current flow

in the windings, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift.

High level on the PHASE input causes the motor current flow from Out A through the winding to Out B

Current Sensor

This part contains a current sensing resistor (R_S), a low pass filter (R_C , C_C) and three comparators.

Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals l_0 and l_1 .

The motor current flows through the sensing resistor R_S .

When the current has increased so that the voltage across R_{S} becomes higher than the reference voltage on the other comparator input, the comparator goes high, which triggers the pulse generator.

The max peak current I_{max} can be defined by:

$$I_{max} = \frac{V_{ref}}{10 \text{ Rs}}$$

STAND BY WITH HALFSTEP MOTOR DRIVE FULL STEP HOLDING TORQUE MOTOR DRIVE 1m = 167mA Im - 333mA 1,2,3,4,5,5,7,8, Im - 500mA 191 -111 - Ph1 -Ph2 -192 -**I12** -MOTOR CURRENT PHASE1 500mA --500mA MOTOR CURRENT PHASE2 500mA --500mA M91L6219-84A

Figure 2: Principle Operating Sequence

Single-pulse Generator

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, t_{off} , which is determined by the time components R_t and C_t .

$$t_{off} = 1.1 \bullet R_tC_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during toff.

If a new trigger signal should occur during t_{off} , it is ignored.

Output Stage

The output stage contains four Darlington transistors (source drivers) four saturated transistors (sink drivers) and eight diodes, connected in two H bridge.

The source transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.

It should be noted however, that is not permitted to short circuit the outputs.

Internal circuitry is added in order to increase the accuracy of the motor current particularly with low current levels.

Vs, Vss, VRef

The circuit will stand any order of turn-on or turn-off the supply voltages Vs and Vss. Normal dV/dt values are then assumed.

Preferably, V_{Ref} should be tracking V_{SS} during power-on and power-off if V_{S} is established.

APPLICATION INFORMATIONS (Note 1)

Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.

Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.

Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity.

As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 100nF capacitor, located near the package between power line and ground.

The ground lead between R_s, and circuit GND should be kept as short as possible.

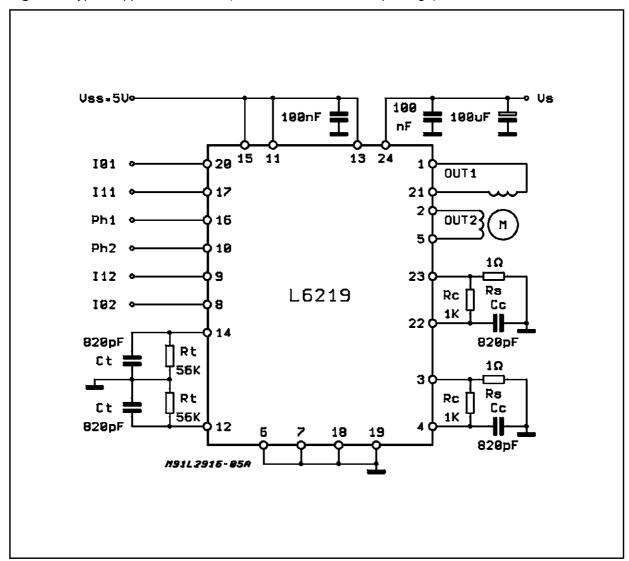
A typical Application Circuit is shown in Fig. 3. Note that C_t must be NPO type or similar else.

To sense the winding current, paralleled metal film resistors are recommended (R_s)

Note 1 - Other information is available as "Smart Power Development System":

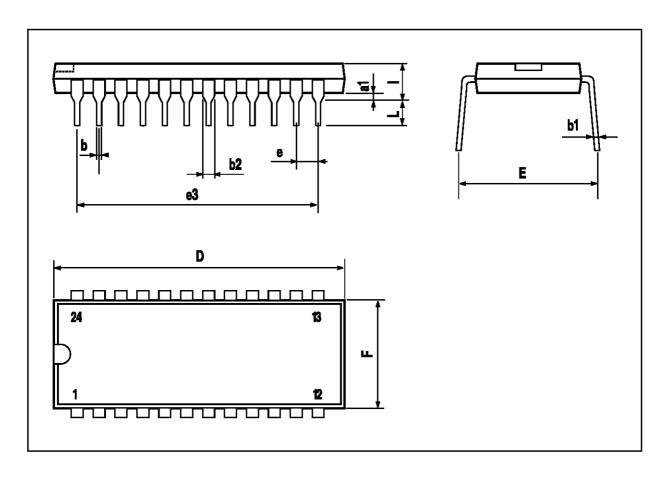
Test board HWL6219 (Stepper driver) Software SWL6219 (Floppy disc)

Figure 3: Typical Application Circuit. (Pin out referred to DIP24 package)



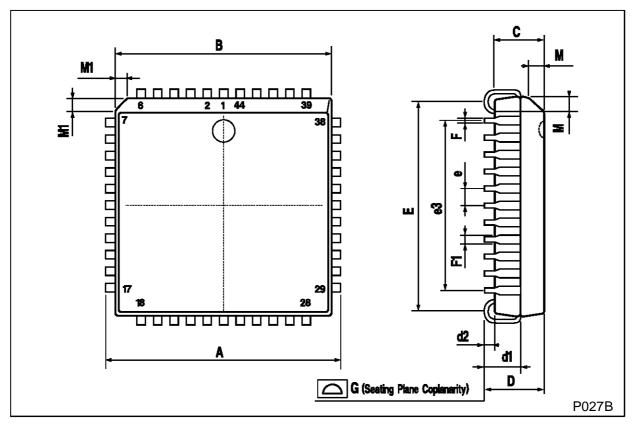
DIP24 PACKAGE MECHANICAL DATA

DIM.		mm			inch	
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
е		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



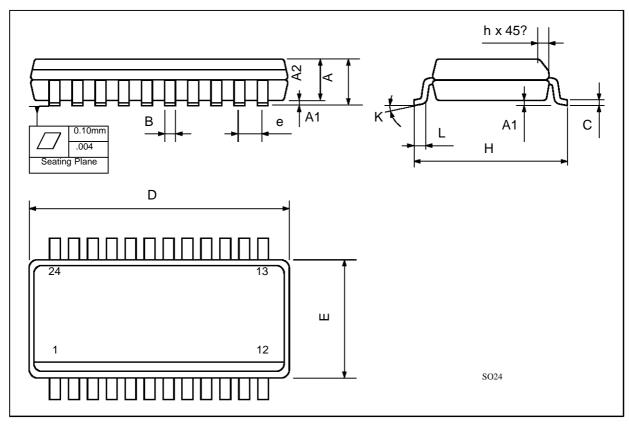
PLCC44 PACKAGE MECHANICAL DATA

DIM.		mm			inch	
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	17.4		17.65	0.685		0.695
В	16.51		16.65	0.650		0.656
С	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
е		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
М		1.16			0.046	
M1		1.14			0.045	



SO24 PACKAGE MECHANICAL DATA

DIM.		mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
А	2.35		2.65	0.093		0.104	
A1	0.10		0.30	0.004		0.012	
A2			2.55			0.100	
В	0.33		0.51	0.013		0.0200	
С	0.23		0.32	0.009		0.013	
D	15.20		15.60	0.598		0.614	
E	7.40		7.60	0.291		0.299	
е		1.27			0,050		
Н	10.0		10.65	0.394		0.419	
h	0.25		0.75	0.010		0.030	
k		0° (min.), 8° (max.)					
L	0.40		1.27	0.016		0.050	



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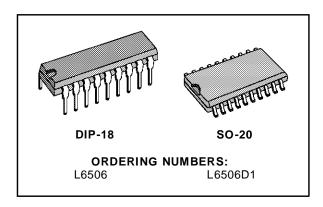
CURRENT CONTROLLER FOR STEPPING MOTORS

ADVANCE DATA

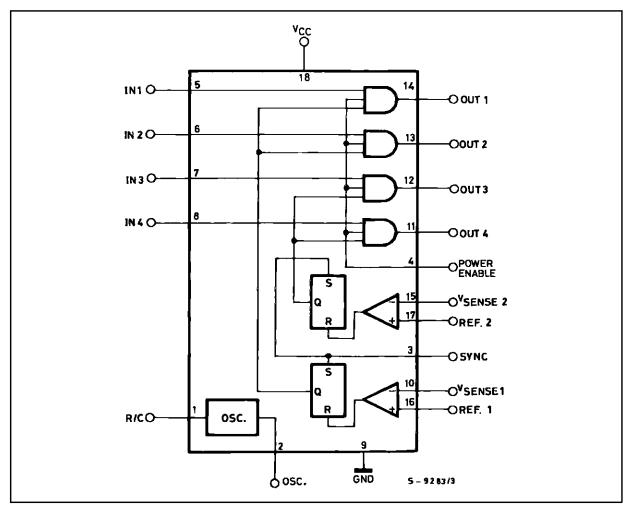
DESCRIPTION

The L6506/D is a linear integrated circuit designed to sense and control the current in stepping motors and similar devices. When used in conjunction with the L293, L298, L7150, L6114/L6115, the chip set forms a constant current drive for an inductive load and performs all the interface function from the control logic thru the power stage.

Two or more devices may be synchronized using the sync pin. In this mode of operation the oscillator in the master chip sets the operating frequency in all chips.

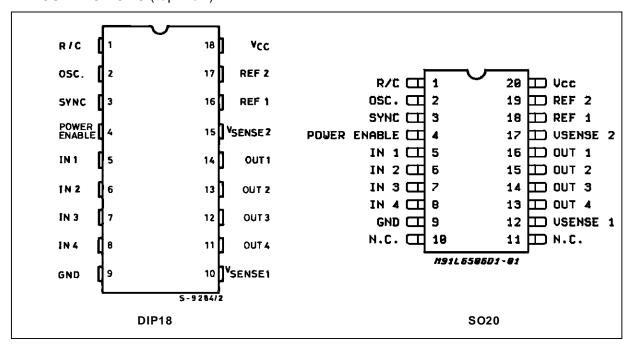


BLOCK DIAGRAM (pin's number referred to DIP-18)



January 1991 1/8

PIN CONNECTIONS (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	10	V
Vi	Input Signals	7	V
P _{tot}	Total Power Dissipation (T _{amb} = 70°C) for DIP18	1	W
	for SO20	0.8	W
Tj	Junction Temperature	150	ပ္
T _{stg}	Storage Temperature	-40 to 150	Ŝ

THERMAL DATA

Sym	Symbol Parameter		DIP18	SO20	Unit	
R _{th j}	-amb	Thermal Resistance Junction-ambient	Max.	80	100	°C/W

ELECTRICAL CHARACTERESTICS (V_{CC} = 5.0V, T_{amb} = 25°C; unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{CC}	Supply Voltage		4.5		7	V
Icc	Quiescent Supply Current	V _{CC} = 7V			25	mA

COMPARATOR SECTION

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{IN}	Input Voltage Range	V _{sense} Inputs	-0.3		3	V
Vio	Input Offset Voltage	V _{IN} = 1.4V			±5.0	mV
I _{IO}	Input Offset Current				±200	nA
I _{IB}	Input Bias Current				1	μΑ
	Response time	$V_{REF} = 1.4V V_{SENS} = 0 \text{ to } 5V$		0.8	1.5	μs



ELECTRICAL CHARACTERISTICS (continued)

COMPARATOR SECTION PERFORMANCE (Over Operating Temperature Range)

Symbol	Parameter	Test Condtions	Min.	Тур.	Max.	Unit
V _{IO}	Input Offset Voltage	$V_{IN} = 1.4V$			±20	mV
I _{IO}	Input Offset Curent				±500	nA

LOGIC SECTION (Over Operating Temperature Range - TTL compatible inputs & outputs)

Symbol	Parameter	Test Condtions	Min.	Тур.	Max.	Unit
V _{IH}	Input High Voltage		2		Vs	V
V _{IL}	Input Low Voltage				0.8	V
Voн	Output High Voltage	V _{CC} = 4.75V I _{OH} = 400μA	2	3.5		٧
Vol	Ouptut Low Voltage	$V_{CC} = 4.75V$ $I_{OH} = 4mA$		0.25	0.4	V
Іон	Ouput Source Current - Outputs 1 - 4	V _{CC} = 4.75V	2.75			mA

OSCILLATOR

Symbol	Parameter	Test Condtions	Min.	Тур.	Max.	Unit
fosc	Frequency Range		5		70	KHz
V_{thL}	Lower Threshold Voltage			0.33 V _{CC}		V
V_{thH}	Higher Threshold Voltage			0.66 V _{CC}		V
R _i	Internal Discharge Resistor		0.7	1	1.3	kΩ

CIRCUIT OPERATION

The L6506 is intended for use with dual bridge drivers, such as the L298, quad darlington arrays, such as the L7150, quad DMOS array such as L6114-L6115, or discrete power transistors to drive stepper motors and other similar loads. The main function of the device is to sense and control the current in each of the load windings.

A common on-chip oscillator drives the dual chopper and sets the operating frequency for the pulse width modulated drive. The RC network on pin 1 sets the operating frequency which is given by the equation

$$f = \frac{1}{0.69 \, RC}$$
 for R > 10 K

The oscillator provides pulses to set the two flip-flops which in turn cause the outputs to activate the drive. When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to V_{ref} and the corresponding comparator resets its flip-flop interrupting the drive current until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resis-

tor and $V_{ref.}$ Since separate inputs are provided for each chopper, each of the loads may be programmed independently allowing the device to be used to implement microstepping of the motor. Lower threshold of L6506's oscillator is 1/3 $V_{CC.}$ Upper threshold is 2/3 $V_{CC.}$ and internal discharge resistor is 1 $K\Omega~\pm~30~\%.$

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground.

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can be found by looking at the figure 1 and are:

$$T2 = 0.69 \text{ C1 } \frac{\text{R1 R}_{\text{IN}}}{\text{R1 + R}_{\text{IN}}} \tag{1}$$

$$T1 = 0.69 R1 C1$$
 (2)

$$DC = \frac{T2}{T1 + T2} \tag{3}$$



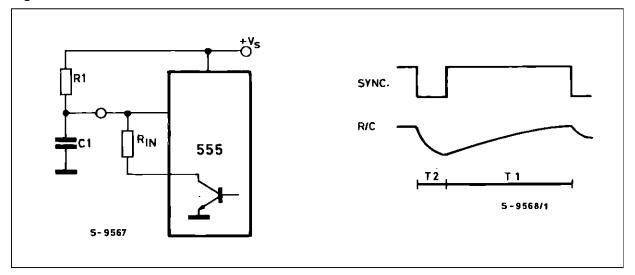
By substituting equations 1 and 2 into equation 3 and solving for the value of R1 the following equations for the external components can be derived:

$$R1 = (\frac{1}{DC} - 2) R_{IN}$$
 (4)

$$C1 = \frac{T1}{0.69 R1}$$
 (5)

Figure 1: Oscillator Circuit and Waveforms.

Looking at equation 1 it can easily be seen that the minimum pulse width of T2 will occur when the value of R1 is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 4 the minimum value for R1 of 700Ω (1 $K\Omega-30$ %) should be used to guarantee the required pulse width.



APPLICATIONS INFORMATION

The circuits shown in figure 2 use the L6506 to implement constant current drives for stepper motors. Figure 2 shows the L6506 used with the L298 to drive a 2 phase bipolar motor. The peak current can be calculated using the equation:

$$I_{peak} = \frac{V_{ref}}{R_{sense}}$$

The circuit of Fig.2 can be used in applications requiring different peak and hold current values by modifying the reference voltage.

The L6506 may be used to implement either full step or half step drives. In the case of 2 phase bipolar stepper motor applications, if a half step drive is used, the bridge requires an additional input to disable the power stage during the half step. If used in conjunction with the L298 the enable inputs may be used for this purpose.

For quad darlington array in 4 phase unipolar motor applications half step may be implemented using the 4 phase inputs.

The L6506 may also be used to implement microstepping of either bipolar or unipolar motors.

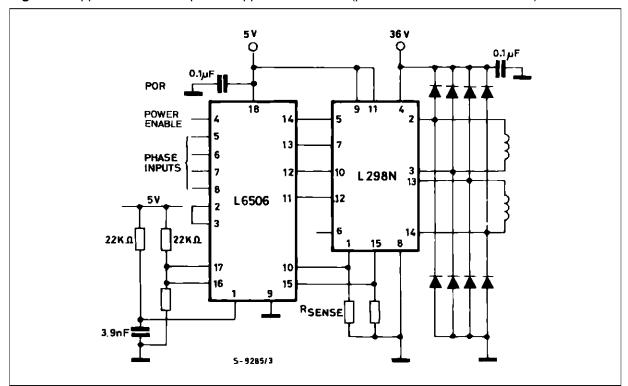
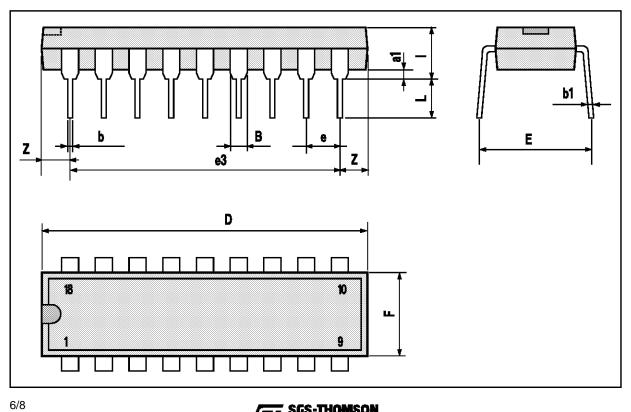


Figure 2: Application Circuit Bipolar Stepper Motor Driver. (pin's number referred to DIP18)

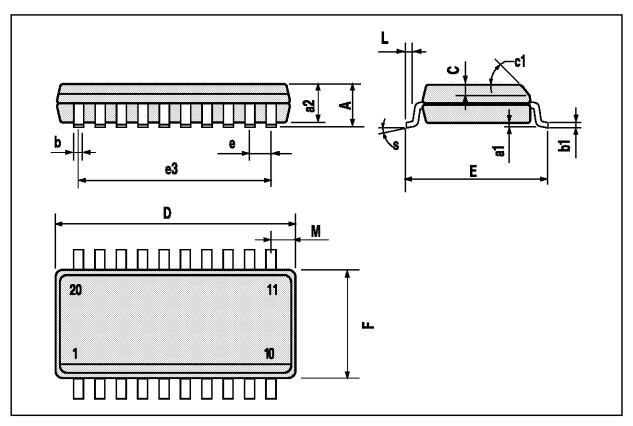
DIP18 PACKAGE MECHANICAL DATA

DIM.	mm					
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
В	1.39		1.65	0.055		0.065
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.915
Е		8.5			0.335	
е		2.54			0.100	
еЗ		20.32			0.800	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.063



SO20 PACKAGE MECHANICAL DATA

DIM.		mm			inch		
Din.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Α			2.65			0.104	
a1	0.1		0.3	0.004		0.012	
a2			2.45			0.096	
b	0.35		0.49	0.014		0.019	
b1	0.23		0.32	0.009		0.013	
С		0.5			0.020		
c1			45 ((typ.)			
D	12.6		13.0	0.496		0.512	
E	10		10.65	0.394		0.419	
е		1.27			0.050		
e3		11.43			0.450		
F	7.4		7.6	0.291		0.299	
L	0.5		1.27	0.020		0.050	
М			0.75			0.030	
S			8 (n	nax.)			



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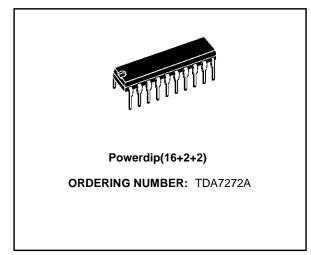


HIGH PERFORMANCE MOTOR SPEED REGULATOR

- TACHIMETRIC SPEED REGULATION WITH NO NEED FOR AN EXTERNAL SPEED PICK-UP
- V/I SUPPLEMENTARY PREREGULATION
- DIGITAL CONTROL OF DIRECTION AND MOTOR STOP
- SEPARATE SPEED ADJUSTMENT
- 5.5V TO 18V OPERATING SUPPLY VOLT-AGE
- 1A PEAK OUTPUT CURRENT
- OUTPUT CLAMP DIODES INCLUDED
- SHORT CIRCUIT CURRENT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION (40V)
- ESD PROTECTION

DESCRIPTION

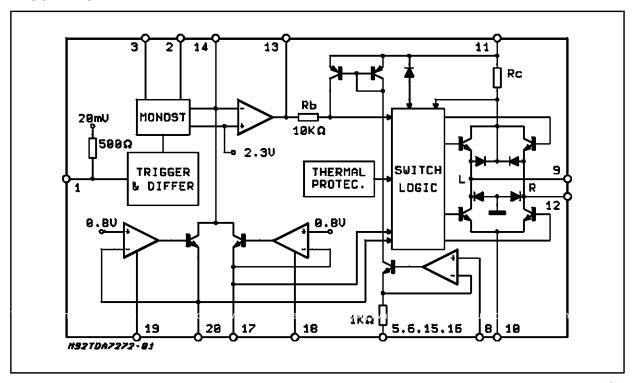
TDA7272A are high performance motor speed controller for small power DC motors as used in cassette players.



Using the motor as a digital tachogenerator itself the performance of true tacho controlled systems is reached.

A dual loop control circuit provides long term stability and fast settling behaviour.

BLOCK DIAGRAM

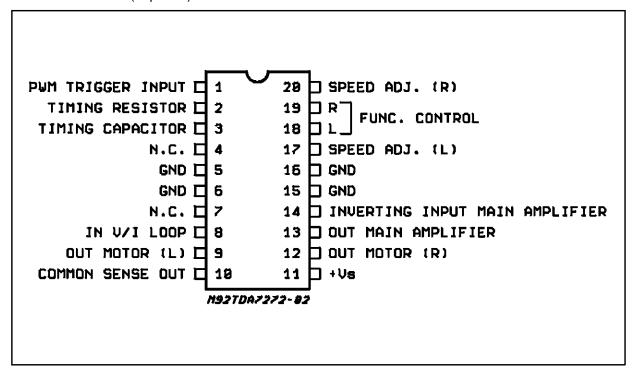


June 1992 1/16

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	DC Supply Voltage	24	V
Vs	Dump Voltage (300ms)	40	V
lo	Output Current	Internally limited	
P _{tot}	Power Dissipation at T _{pins} = 90°C at T _{amb} = 70°C	4.3 1	W W
T_op	Operating Temperature Range	-40 to 85	°C
T _{stg}	Storage Temperature	-40 to 150	°C

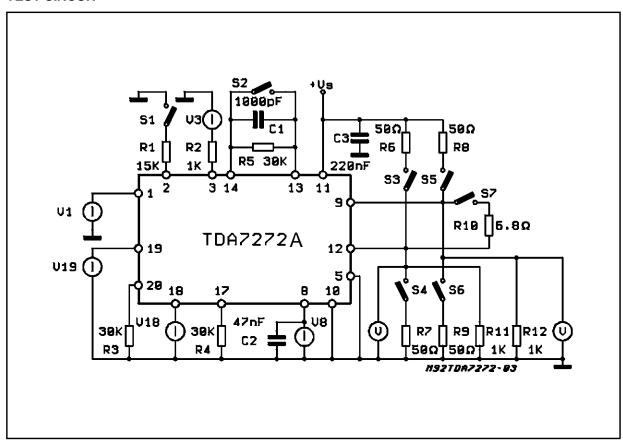
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Symbol Parameter		Unit
R _{th j-amb}	Thermal Resistance Junction-ambient max.	80	°C/W
R _{th j-pins}	Thermal Resistance Junction-pins max.	14	°C/W

TEST CIRCUIT



ELCTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = 13.5V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Vs	Operating Supply Voltage		5.5		18	V
Is	Supply Current	No load		5	12	mA
OUTPUT	STAGE					
Io	Output Currente Pulse		1			Α
Io	Output Currente Continuous		250			mA
V _{10,9,12}	Voltage Drop	I _O = 250mA		1.2	1.5	V
V _{11,9,12}	Voltage Drop	I _O = 250mA		1.7	2	V
MAIN AM	PLIFIER					
R ₁₄	Input Resistance		100			ΚΩ
I _b	Bias Current			50		nA
V _{OFF}	Offset Voltage			1	5	mV
V _R	Reference Voltage	Internal at non inverting input		2.3		V

ELECTRICAL	. CHARACTERISTICS	(Continued))
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Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit				
CURRENT	RRENT SENSE AMPLIFIER									
R ₈	Input Resistance		100			ΚΩ				
GL	Loop Gain			9						
TRIGGER	AND MONOSTABLE STAGE									
V _{IN1}	Input Allowed Voltage		-0.7		3	V				
R _{IN1}	Input Resistance			500		Ω				
V _T Low	Trigger Level			0		V				
V _{TB}	Bias Voltage (pin 1)		15	20	25	mV				
V _{T H}	Trigger Histeresis			10		mV				
V _{2 REF}	Reference Voltage		750	800	850	mV				
SPEED P	ROGRAMMING, DIRECTION CONT	ROL LOGIC AND CURRENT SOU	RCE PRO	GRAMN	IING					
V _{18,19 Low}	Input Low Level				0.7	V				
V _{18,19 High}	Input High Level		2			V				
I _{18,19}	Input Current	0 < V _{18,19} < V _S		2		μΑ				
V _{17,20 REF}	Reference Voltage		735	800	865	mV				

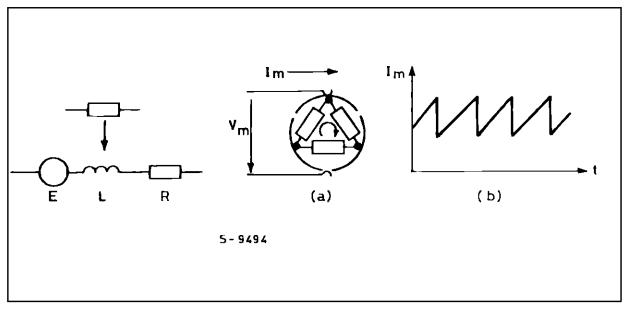
The TDA7272A novel applied solution is based on a tachometer control system without using such extra tachometer system. The information of the actual motor speed is extracted from the motor itself. A DC motor with an odd number of poles generates a motor current which contains a fixed number of discontinuities within each rotation. (6 for the 3 pole motor example on fig. 1)

Deriving this inherent speed information from the motor current, it can be used as a replacement of a low resolution AC tachometer system. Because the settling time of the control loop is limited on principle by the resolution in time of the tachome-

ter, this control principle offers a poor reaction time for motors with a low number of poles. The realized circuit is extended by a second feed forward loop in order to improve such system by a fast auxiliary control path.

This additional path senses the mean output current and varies the output voltage according to the voltage drop across the inner motor resistance. Apart from a current averaging filter, there is no delay in such loop and a fast settling behaviour is reached in addition to the long term speed motor accuracy.

Figure 1: Equivalent of a 3 Pole DC Motor (a) and Typical motor Current Waveform (b).



BLOCK DESCRIPTION

The principle structure of the element is shown in fig. 2. As to be seen, the motor speed information is derived from the motor current sense drop across the resistors $R_{\rm S}$; capacitor CD together with the input impedance of 500 $\,\Omega$ at pin 1 realizes a high pass filter.

This pin is internally biased at 20 mV, each negative zero transition switches the input comparator. A 10 mV hysteresis improves the noise immunity.

The trigger circuit is followed by an internal delay time differentiator.

Thus, the system becomes widely independent of the applied waveform at pin 1, the differentiator triggers a monostable circuit which provides a constant current duration. Both, output current magnitude and duration T, are adjustable by ex-

Figure 2: Application Circuit.

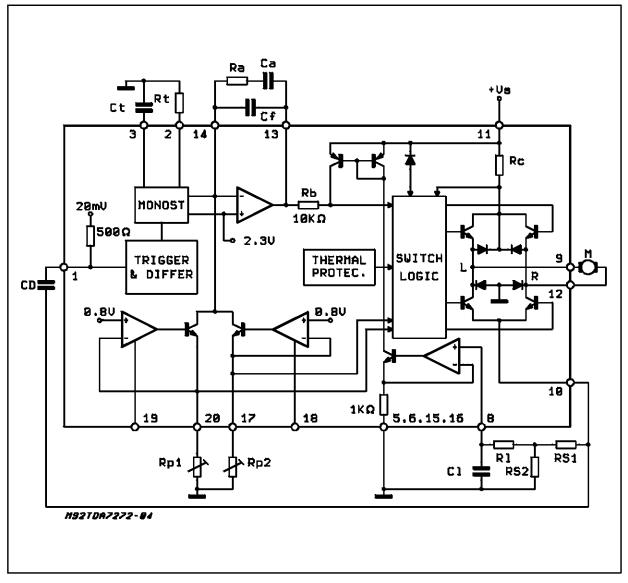
ternal elements CT and RT.

The monostable is retriggerable; this function prevents the system from fault stabilization at higher harmonics of the nominal frequency.

The speed programming current is generated by two separate external adjustable current sources. A corresponding digital input signal enables each current source for left or right rotation direction. Resistor RP1 and RP2 define the speed, the logical inputs are at pin 18 and 19.

At the inverting input (pin 14) of the main amplifier the reference current is compared with the pulsed monostable output current.

For the correct motor speed, the reference current matches the mean value of the pulsed monostable current. In this condition the charge of the feedback capacitor becomes constant.



The speed n of a k pole motor results:

$$n = \frac{10.435}{C_T k R_P}$$

and becomes independent of the resistor RT which only determines the current level and the duty cycle which should be 1:1 at the nominal speed for minimum torque ripple.

The second fast loop consists of a voltage to current converter which is driven at pin 8 by the low pass filter R_L , C_L . The output current at this stage is injected by a PNP current mirror into the inner resistor R_B . So the driving voltage of the output stage consists of the integrator output voltage plus the fast loop voltage contribution across R_B .

The power output stage realizes different modes depending on the logic status at pin 18 and 19.

- Normal operation for left and right mode: each upper TR of the bridge is used as voltage follower whereas the lower acts as a switch.
- Stop mode where the upper half is open and the lower is conductive.
- High impedance status where all power elements are switched-off.

The high impedance status is also generated when the supply voltage overcomes the 5 V to 20 V operating range or when the chip temperature exceeds 150 $^{\circ}$ C.

A short circuit protection limits the output current at 1.5 A. Integrated diodes clamp spikes from the inductive load both at V_{CC} and ground.

The reference voltages are derived from a common bandgap reference. All blocks are widely supplied by an internal 3.5 V regulator which provides a maximum supply voltage rejection.

PIN FUNCTION AND APPLICATION INFORMATION

PIN 1

Trigger input. Receives a proper voltage which contains the information of the motor speed. The waveform can be derived directly by the motor current (fig. 3). The external resistor generates a proper voltage drop. Together with the input resistance at pin 1 [R_{IN}(1) = 500 Ω] the external capacitor C_D realize a high pass filter which differentiates the commutation spikes of the motor current. The trigger level is 0V.

The biasing of the pin 1 is 20 mV with a hysteresis of 10 mV. So the sensing resistance must be chosen high enough in order to obtain a negative spike of the least 30 mV on pin 1, also with minimum variation of motor current:

$$R_S \ge \frac{30\text{mV}}{\Delta I_{MOT} \text{ min.}}$$

Such value can be too much high for the preregulation stage V-I and it could be necessary to split

Figure 3.

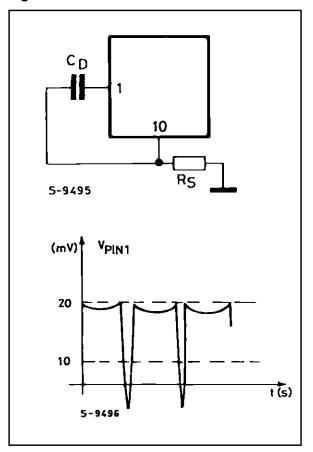
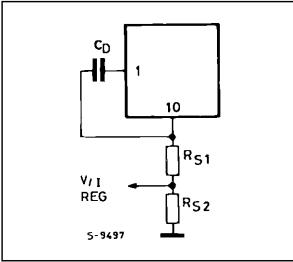


Figure 4.

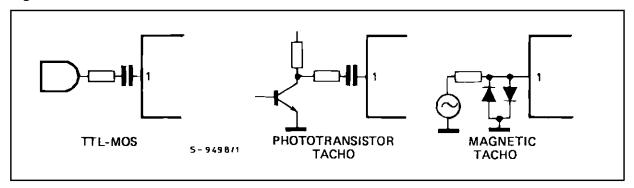


them into 2 series resistors $Rs = Rs_1 + Rs_2$ (see fig. 4) as explained on pin 8 section.

The information can be taken also from an external tachogenerator. Fig. 5 shows various sources connections:

the input signal mustn't be lower than 0.7 V.

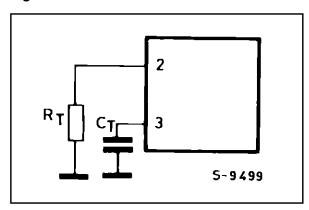
Figure 5.



Pin 2

Timing resistor. An internal reference voltage (V2 = 0.8 V) gives possibility to fix by an external resistor (R_T), from this pin and ground, the output current amplitude of the monostable circuit, which will be reflected into the timing capacitor (pin 3); the typical value would be about 50 μ A.

Figure 6.



Pin 3

Timing capacitor. A constant current, determined by the pin 2 resistor, flowing into a capacitor between pin 3 and ground provides the output pulse width of the monostable circuit, the max voltage at pin 3 is fixed by an internal threshold: after reaching this value the capacitor is rapidly discharged and the pulse width is fixed to the value:

$$T_{on} = 2.88 R_T C_T$$
(fig. 6)

Pin 4

Not connected.

Pin 5

Ground. Connected with pins 6, 15, 16.

Pin 6

Ground. Connected with pins 5, 15, 16.

Pin 7

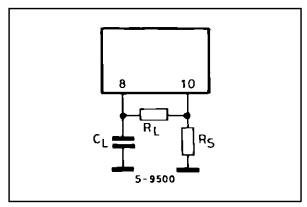
Not connected.

Pin 8

Input V/I loop. Receives from pin 10, through a low pass filter, the voltage with the information of the current flowing into the motor and produces a negative resistance output:

$$R_{out} = -9 R_{S}$$
 (fig. 7)

Figure 7.



For compensating the motor resistance and avoiding instability:

$$R_{S} \leq \frac{R_{MOTOR}}{9}$$

The optimization of the resistor Rs for the tachometric control must not give a voltage too high for the V/I stage: one solution can be to divide in two parts, as shown in fig. 8, with:

$$R_{S2} = \frac{R_M}{10}$$
 and $R_{S1} + R_{S2} \ge \frac{30mV}{\Delta \text{ I mot min.}}$

(see pin 1 sect.)

The low pass filter R_L , C_L must be calculated in order to reduce the ripple of the motor commutation at least 20 dB. Another example of possible pins 10-8 connections is showed on fig. 9. A choke can be used in order to reduce the radiation.

Figure 8.

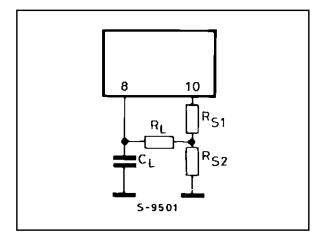
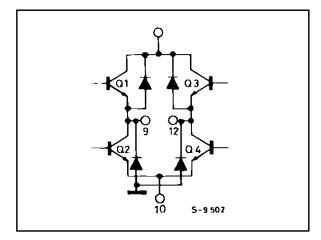


Figure 9.



Pin 9

Output motor left. The four power transistors are realized as darlington structures. The arrangement is controlled by the logic status at pins 18

As before explained (see block description), in the normal left or right mode one of the lower darlington becomes saturated whereas the other remains open. The upper half of the bridge operates in the linear mode.

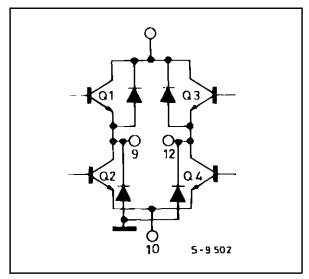
In stop condition both upper bridge darlingtons are off and both lower are on. In the high output impedance state the bridge is switched completely off.

Connecting the motor between pins 9 and 12 both left or right rotation can be obtained. If only one rotation sense is used the motor can be connected at only one output, by using only the upper bridge half. Two motors can be connected each at the each output: in such case they will work alternatively (see application section).

The internal diodes, together with the collector

substrate diodes, protect the output from inductive vol-tage spikes during the transition phase (fig. 10)

Figure 10.



Pin 10

Common sense output. From this pin the output current of the bridge configuration (motor current) is fed into Rs external resistor in order to generate a proper voltage drop.

The drop is supplied into pin 1 for tachometric control and into pin 8 for V/I control (see pin 1 and pin 8 sections).

Pin 11

Supply voltage.

Pin 12

Output motor right. (see pin 9 section)

Pin 13

Output main amplifier. The voltage on this pin results from the tachometric speed control and feeds the output stage.

The value of the capacitor CF (fig. 11), connected from pins 13 and 14, must be chosen low enough in order to obtain a short reaction time of the tachometric loop, and high enough in order to reduce the output ripple.

A compromise is reached when the ripple voltage (peak-to-peak) V_{ROP} is equal to 0.1 V_{MOTOR} : $C_F = 2.3 \; \frac{C_T}{V_{RIP}} \, (\; 1 - \frac{R_T}{R_P} \,)$

$$C_F = 2.3 \frac{C_T}{V_{RIP}} (1 - \frac{R_T}{R_P})$$

with $V_{RIP} = \frac{V_{FEM} + I_{MOT} \cdot R_{MOT}}{(\text{see pin } 29 \text{ section})}$ and with duty cycle = 50 %.

Figure 11.

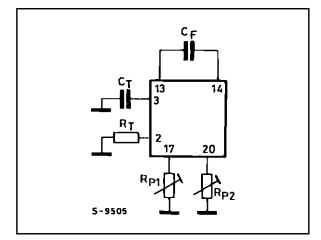
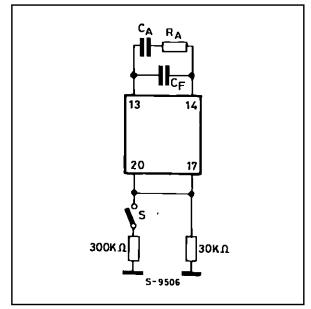


Figure 12.



In order to compensate the behaviour of the whole system regulator-motor-load (considering axis friction, load torque, inertias moment of the motor of the load. etc.) a RC series network is also connected between pins 13 and 14 (fig. 12). The value of C_A and R_A must been chosen experimentally as follows:

- Increase of 10 % the speed with respect to the nominal value by connecting in parallel to R_{p} a resistor with value about 10 time larger.
- Vary the R_A and C_A values in order to obtain at pin 13 a voltage signal with short response time and without oscillations. Fig. 13 shows the step response at pin 13 versus R_A and C_A values.

Pin 14

Figure 13.

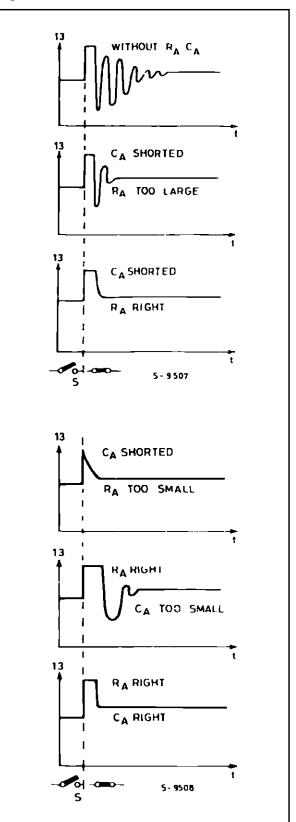
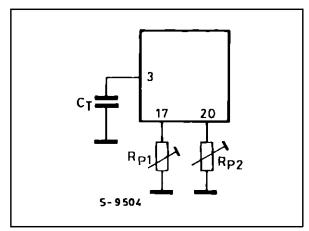


Figure 14.



Inverting input of main amplifier. In this pin the current reference programmed at pins 20, 17 is compared with the current from the monostable (stream of rectangular pulses).

In steady-state condition (constant motor speed) the values are equal and the capacitor C_{F} voltage is constant.

This means for the speed n (min 1):

$$n = \frac{10.435}{C_T k R_P}$$

where "k" is the number of collector segments. (poles)

The non inverting input of the main amplifier is internally connected to a reference voltage (2.3 V).

Pin 15

Ground.

Pin 16

Ground.

Pin 17

Left speed adjustment. The voltage at this pin is fixed to a reference value of 0.8 V. A resistor from this pin and ground (fig. 14) fixes the reference current which will be compared with the medium output current of the monostable in order to fix the speed of the motor at the programmed value. The correct value of R_{P} would be :

$$R_P = \frac{10.435}{C_T \text{ k n}}$$

n = motor speed, (min -1)

k = poles number

The control of speed can be done in different way:

- speed separately programmed in two senses of rotation (fig. 14-15);
- only one speed for the two senses of rotation (fig. 16);

Figure 15.

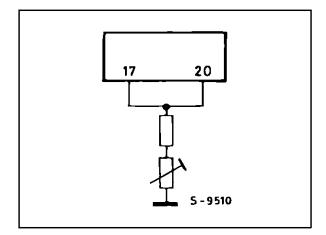


Figure 16.

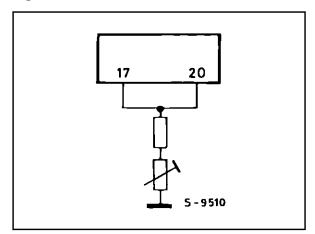
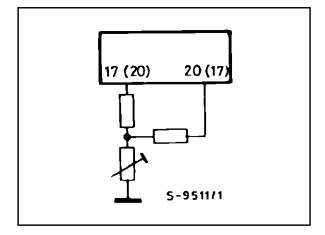


Figure 17.

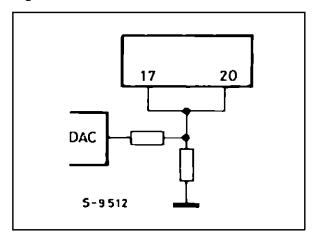


- speeds of the two senses a bit different (i.e. for compensating different pulley effects) (fig. 17);
- speed programmed with a DC voltage (fig. 18) i.e. with DA converter;

 fast forward, by putting a resistor. In this case it is necessary that also at the higher speed for the duty cycle to be significately less than 1 (see value of R_T, C_T on pin 2, pin 3 sections).

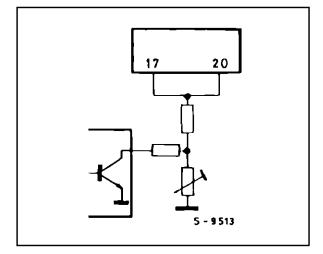
Fig. 19 shows the function controlled with a μP .

Figure 18.



Pin 18Right function control. The voltages applied to this pin and to pin 19 determine the function, as showed in the table.

Figure 19.



The typical value of the threshold (L-H) is 1.2 V.

Pin 19

Left function control. (see pin 18 sect).

Pin 20

Right speed adjustment. (see pin 17 sect).

COND	CONDITION OUTPUT FUNCTION O		OUTPUT	VOLTAGE
Pin 18	Pin 19	COTFOLLONGLION	Pin 12	Pin 9
L	L	STOP	LOW	LOW
H	L	LEFT	LOW	REG
L	Н	RIGHT	REG	LOW
H	Н	OPEN	HIGH IMP.	HIGH IMP.

Figure 20: Typical application.

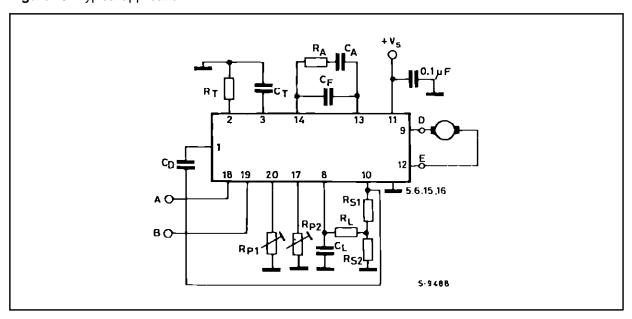


Figure 21: Tacho only speed regulation.

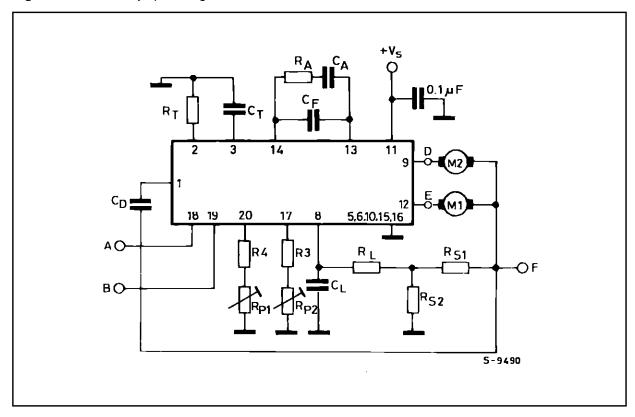
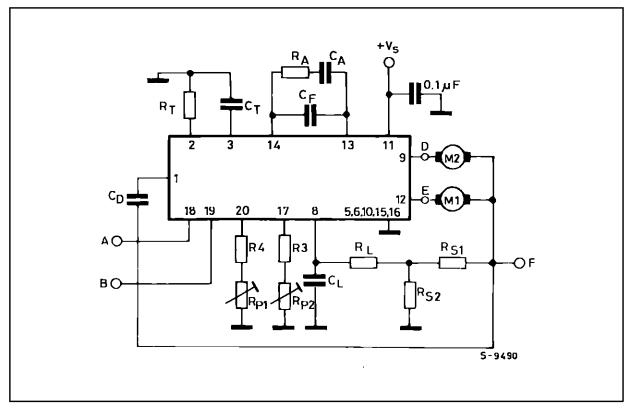


Figure 22: One direction regulator of one motor, or alternatively of two motors.



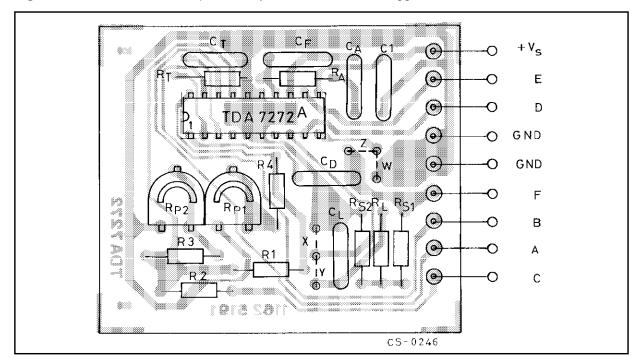


Figure 23: P.C. board and components layout of the circuits of Figg. 20, 21, 22.

APPLICATION SUGGESTION (Fig. 20,21,22) - (For a 2000 r.p.m. 3 pole DC motor with $R_M = 16\Omega$)

Components	Recommended	Purpose	If larger	If smaller	Allowe	d range
Components	value	Fulpose	ii laigei	ii Silialiei	Min.	Max.
R _{S1}	1Ω	Current sensing tacho loop.		Tacho loop do not regulate	0	
R _{S2}	1.5Ω	Current sensing V/I loop.	Instability may occur.	Motor regulator; undercompens.	0	R _{MOT} /9
R _L ; C _L	22KΩ - 68nF	Spike filtering.	Slow V/I regulator response.	High output ripple.		
C_{D}	68nF	Pulse transf.			33nF	100nF
R _T ; C _T	15KΩ - 47nF	Current source programming to obtain a 50% duty cycle			67ΚΩ	30KW
R _{P1} ; R _{P2}	47KΩ trim.	Set of speed.	Low speed.	High speed	0	
C_{F}	Polyester 100nF	Optimization of integrator ripple and loop response time.	Lower ripple, slower tacho regulator response.	Higher ripple, faster response.	10nF	470nF
R _A ; C _A	220KΩ - 220nF	Fast response with no overshoot.	Depending on electrmechanical system.		10nF	470nF

Figure 24: Speed regulation vs. supply voltage (circuit of fig. 20).

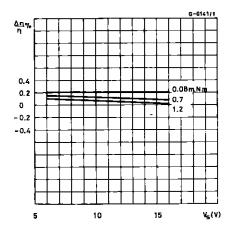
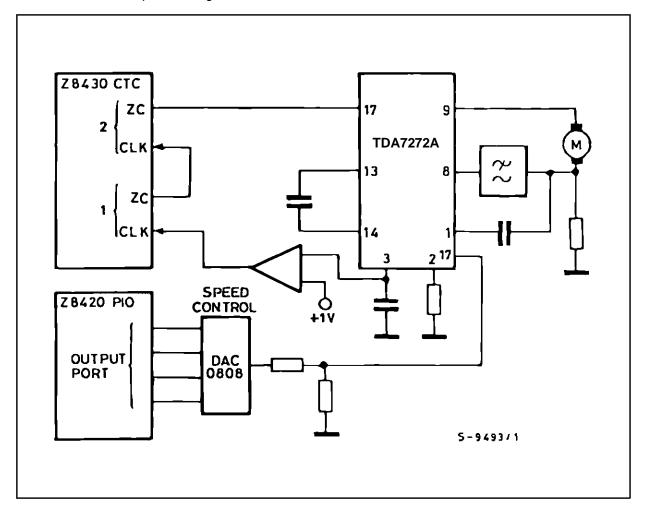
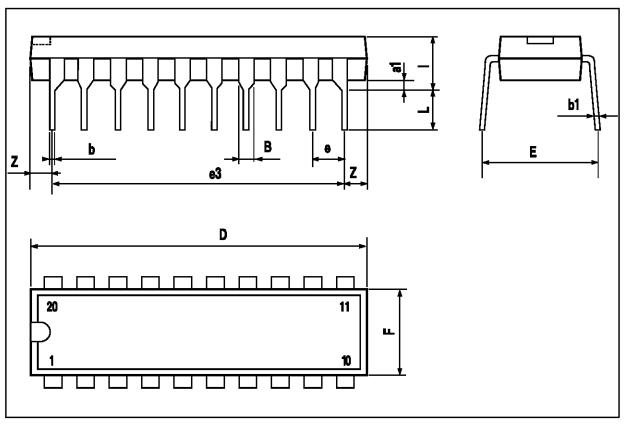


Figure 26: In connection with a Presettable Counter and I/O peripheral the TDA7271A/TDA7272A controls the speed through a D/A Converter.



POWERDIP 20 PACKAGE MECHANICAL DATA

DIM.		mm inch			inch	
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
В	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
е		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



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TEA3718 TEA3718S

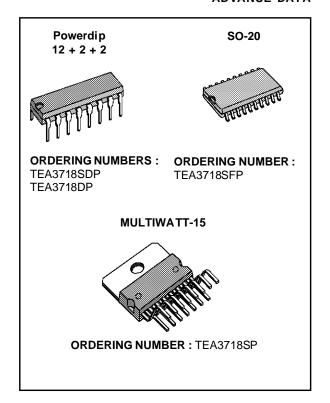
STEPPER MOTOR DRIVER

ADVANCE DATA

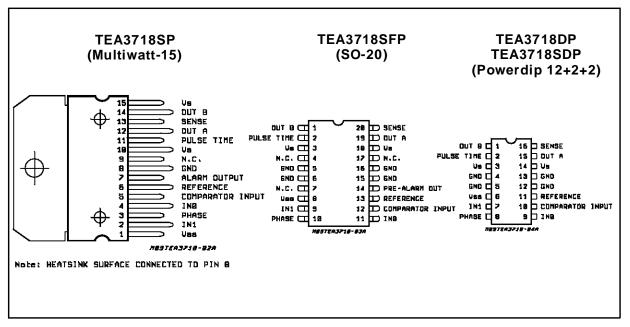
- HALF-STEP AND FULL-STEP MODE
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL 5 TO 1500 mA
- WIDE VOLTAGE RANGE 10 TO 50 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CAN BE SELECTED IN STEPS OR VARIED CONTINUOUSLY
- THERMAL OVERLOAD PROTECTION
- ALARM OUTPUT OR PRE-ALARM OUTPUT (see internal table)

DESCRIPTION

The TEA3718 and TEA3718S are bipolar monolithic integrated circuits intended to control and drive the current in one winding of a bipolar stepper motor. The circuits consist of an LS-TTL compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEA3718 or TEA3718S and a few external components form a complete control and drive unit for LS-TTL or microprocessor-controlled stepper motor systems.

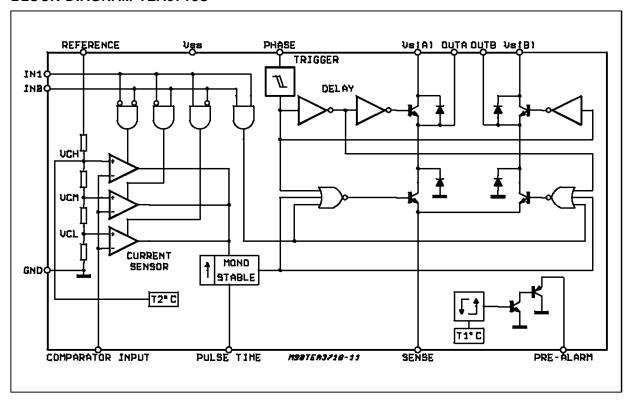


PIN CONNECTIONS (top views)

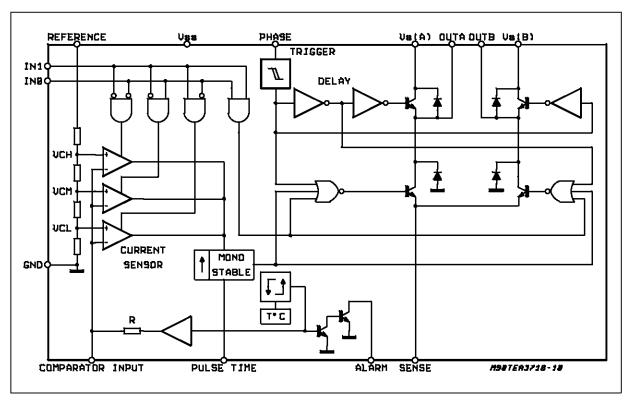


December 1991 1/16

BLOCK DIAGRAM TEA3718S



BLOCK DIAGRAM TEA3718



PIN FUNCTIONS

Name	Function
OUT B	Output Connection (with pin OUTA). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators ($t_{off} = 0.69 R_T C_T$).
V _S (B)	Supply Voltage Input for Half Output Stage
GND	Ground Connection. In SO-20L and Powerdip these pins also conduct heat from die to printed circuit copper.
V _{SS}	Supply Voltage Input for Logic Circuitry
IN1	This pin and pin INO are logic inputs which select the outputs of three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUT A (source) to OUT B (sink). A Schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
IN0	See INPUT 1
COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter R _C C _C . The lower power transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by R _T C _T , T _{off} = 0.69 R _T C _T .
REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators. Reference voltage with the value of $R_{\rm S}$ and the two inputs IN0 and IN1 determines the output current.
V _S (A)	Supply voltage input for half output stage
OUT A	See pin OUT B
SENSE RESISTOR	Connection to lower emitters of output stage for insertion of current sense resistor
ALARM	When T _j reaches T1°C the alarm output becomes low (TEA3718SP)
PRE-ALARM	When T _j reaches T2°C the prealarm output becomes low (T2 <t1) (tea3718sfp)<="" td=""></t1)>

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Value	Unit
Vss	Supply Voltage	7	V
Vs		50	V
VI	Input Voltage:		
	Logic Inputs	6	V
	Analog Inputs	V_{SS}	V
	Reference Input	15	V
iį	Input Current		
	Logic Inputs	-10	mA
	Analog Inputs	-10	mA
lo	Output Current	±1.5	Α
TJ	Junction Temperature	+150	°C
Top	Operating Ambient Temperature Range	0 to 70	°C
T _{stg}	Storage Temperature Range	-55 to +150	°C

THERMAL DATA

Symbol	Parameter	SO-20L	Powerdip	Multiwatt	Unit
R _{th} (j-c)	Maximum Junction-case Thermal Resistance	16	11	3	°C/W
R _{th} (j-a)	Maximum Junction-ambient Thermal Resistance	60 *	45 *	40	°C/W

 $^{^{\}ast}$ Soldered on a 35 μm thick 4 cm^2 PC board copper area.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Тур.	Max.	Unit
V _{SS}	Supply Voltage	4.75	5	5.25	V
Vs	Supply Voltage	10	ı	45	V
i _m	Output Current	0.020	1	1.2	Α
T _{amb}	Ambient Temperature	0		70	°C
t _r	Rise Time Logic Inputs	_	_	2	μs
t _f	Fall Time Logic Inputs	_	_	2	μs

COMPARISON TABLE

Device	Current	Package	Alarm	Pre-Alarm
TEA3718SDP	1.5A	Powerdip 12+2+2		not connected
TEA3718SFP	1.5A	SO-20L		х
TEA3718SP	1.5A	Multiwatt-15	Х	
TEA3718DP	1.5A	Powerdip 12+2+2	not connected	



MAXIMUM POWER DISSIPATION

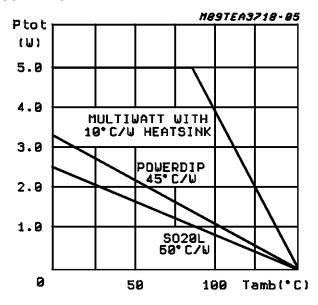


Figure 1.

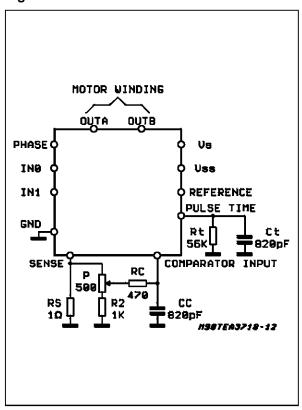
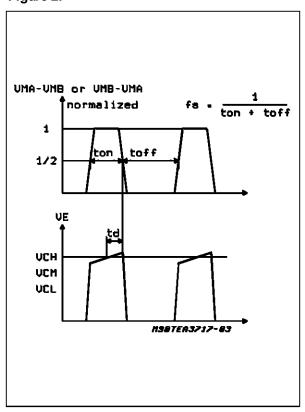


Figure 2.



 $R_S = 1 \Omega$ INDUCTANCE FREE

 $R_C = 470 \: \Omega$

C_C = 820 pF CERAMIC

 $R_t = 56 \text{ k}\Omega$

 $C_t = 820 \text{ pF CERAMIC}$

 $P = 500 \Omega$

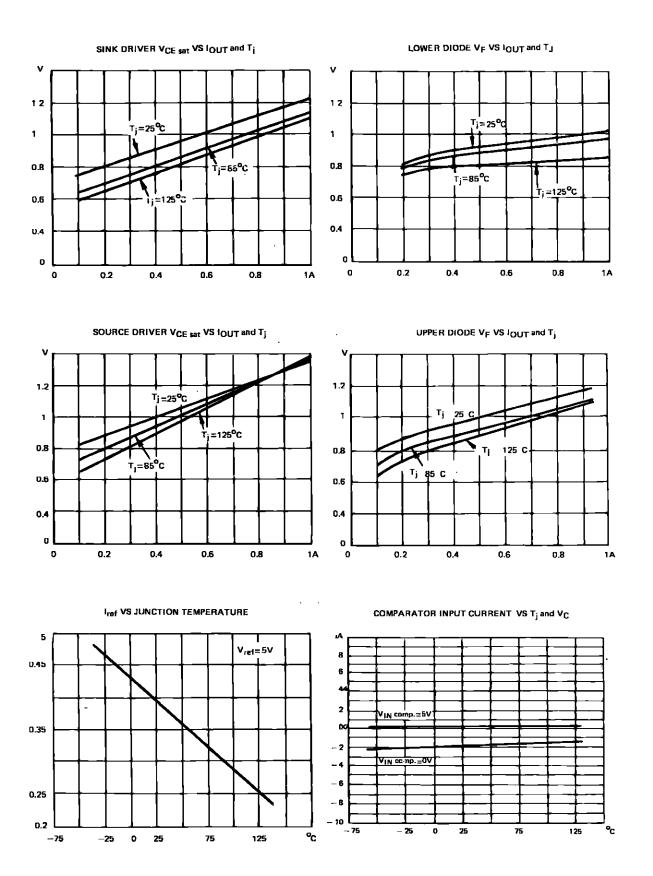
 $R_2 = 1 K$

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V,\pm5\%,\,V_{mm}=10V$ to 45V, $T_{amb}=0$ to 70°C ($T_{amb}=25$ °C for TEA3718FP/SFP) unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit		
Icc	Supply Current	-	-	25	mA		
V _{IH}	High Level Input Voltage - Logic Inputs	2	-	-	V		
V_{IL}	Low Level Input Voltage - Logic Inputs			-	-	0.8	V
I _{IH}	High Level Input Current - Logic Inputs			-	-	20	μΑ
I _{IL}	Low Level Input Current - Logic Inputs (VI =	0.4V)		-0.4	-	-	mA
V _{CH} V _{CM} V _{CL}	Comparator Thershold Voltage (VR = 5V)	390 230 65	420 250 80	440 270 90	mV mV mV		
Ico	Comparator Input Current	-20	-	20	μΑ		
l _{off}	Output Leakage Current (I _O = 0, I ₁ = 1 T _{amb}	₀ = 25°C		-	-	100	μΑ
V _{sat}	Total Saturation Voltage Drop (Im = 1A)		1 1	2.8 3.2	> >		
P_{tot}	Total Power Disssipation - I _m = 1A, f _s = 30K	-	3.1	3.6	W		
$t_{\rm off}$	Cut off Time (see figure 1 and 2, V _{mm} = 10V	25	30	35	ms		
t _d	Turn off Delay (see fig. 1 and 2, T _{amb} = 25°0	-	1.6	-	μs		
V_{sat}	Alarm Output Saturation Voltage - I _O = 2mA	-	0.8	-	V		
I _{ref}	Reference Input Current, V _R = 5V	-	0.4	1	mA		
V_{sat}	Source Diode Transistor Pair Saturation Powerdip $I_m = 0.5A$ Voltage Powerdip $I_m = 1A$				1.05 1.35	1.2 (1.3) 1.5 (1.7)	V V
				-	-	1.3 1.7	V V
V _f	Diode Forward Voltage				1.1 1.25	1.5 (1.6) 1.7 (1.9)	V V
I _{sub}	Substrate Leakage Current $I_f = 1A$				-	5	mA
V_{sat}	V _{sat} Sink Diode Transistor Pair Saturation Voltage		$I_{m} = 0.5A$ $O I_{m} = 1A$	-	1 1.2	1.2 (1.3) 1.3 (1.5)	V V
			Multiwatt $I_m = 0.5A$ Multiwatt $I_m = 1A$		-	1.3 1.5	V V
V _f	Diode Forward Voltage			-	1 1.1	1.4 (1.6) 1.5 (1.9)	V V

Notes

(...) Only for TEA3718SFP mounted in SO-20L package.



FUNCTIONAL BLOCKS

Figure A: ALARM OUTPUT (TEA3718SP - TEA3718DP)

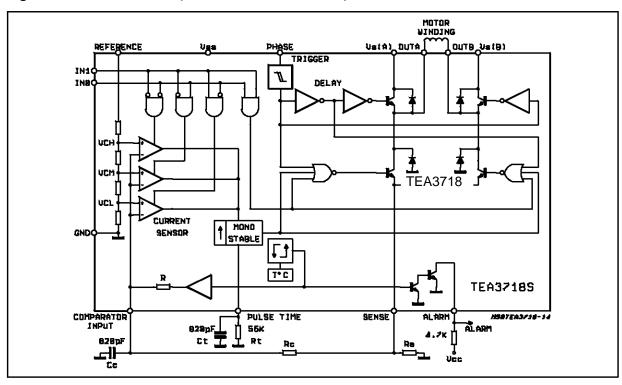
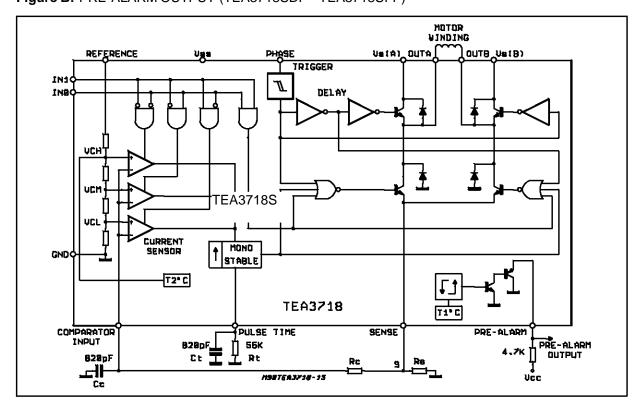


Figure B: PRE-ALARM OUTPUT (TEA3718SDP - TEA3718SFP)



ALARM OUTPUTS (TEA3718SP - TEA3718DP) The alarm output becomes low when the junction temperature reaches T°C.

When an alarm condition occours, parts of the supply voltage (dividing bridge R - R_C) is fed to the comparator input pin (Fig. A)

the comparator input pin (Fig. A)
Depending of the R_CC value the behaviour of the circuit is different on alarm condition:

1) $R_C > 80\Omega \Rightarrow$ the output stage is switched off

2) $R_C > 60\Omega \Rightarrow$ the current in the motor windings is reduced according to the approximate formula: (see also fig. E and F)

$$I_m = \frac{V_{TH}}{R_S} - \frac{V_{CC}}{R + R_C} \bullet \frac{R_C}{R_S}$$

with V_{TH} = Threshold of the comparator (V_{CH} , V_{CM} , V_{CL}) R = 700 Ω (typical)

For several Multiwatt packages a common detection can be obtained as in Fig. D

PRE-ALARM OUTPUT

When the junction temperature reaches T1°C (typ. = 170°C) a prealarm signal is generated.

Soft thermal protection occours when function temperature reaches T2 (T2 > T1)

Figure C: Alarm Detection for Powerdip Package

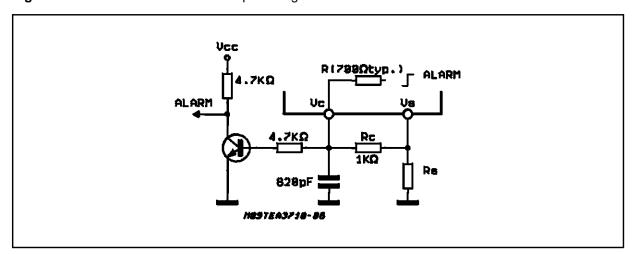


Figure D: CommonDetection for Several Multiwatt Package

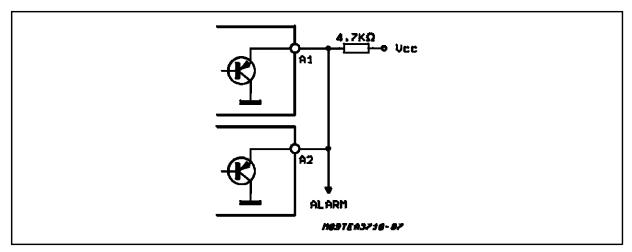


Figure E: (typical curve) Current Reduction in the Motor on Alarm Condition.

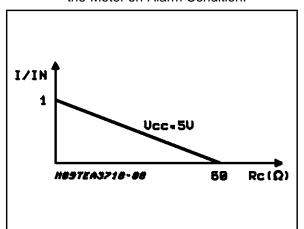
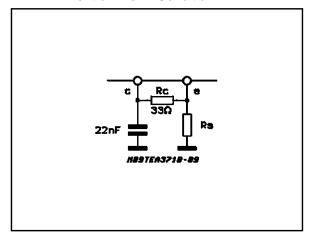
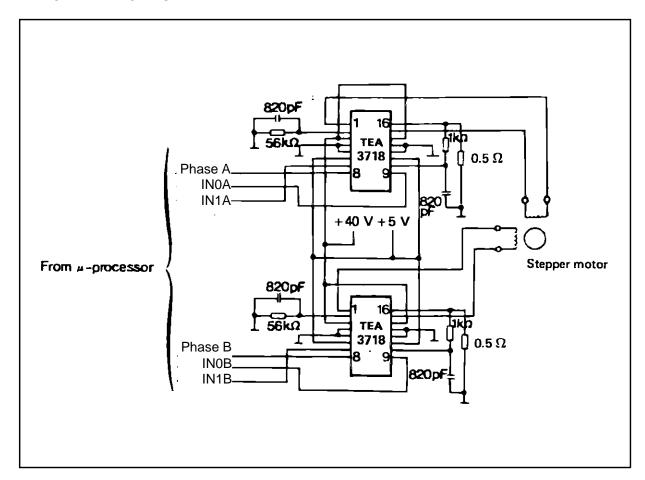


Figure F: (V_{ref} 5V) Block Diagram for Half Current on Alarm Condition.



Notes: 1. Resistance values given here are for the V_{ch} threshold. They should be adjusted using other comparators threshold or other V_{ref} value.

TYPICAL APPLICATION



FUNCTIONAL DESCRIPTION

The circuit is intended to drive a bipolar constant current through one motor winding. The constant current is generated through switch mode regulation.

There is a choice of three different current levels with the two logic inputs IN0 and IN1. The current can also be switched off completely.

INPUT LOGIC

If any of the logic inputs is left open, the circuit will treat it as a high level input.

IN0	IN1	Current Level				
Н		No Current				
L	Н	Low Current				
Н	L	Medium Current				
L	L	Maximum Current				

PHASE - This input determines the direction of current flow in the winding, depending on the motor connections. The signal is fed through a Schmidttrigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift. High level on the PHASE input causes the motor current flow from Out A through the winding to Out B.

 l_{H0} and l_{H1} - The current level in the motor winding is selected with these inputs. The values of the different current levels are determined by the reference voltage V_R together with the value of the sensing resistor $R_S.$

CURRENT SENSOR

This part contains a current sensing resistor (R_S), a low pass filter (R_C , C_C) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals INO and IN1. The motor current flows through the sensing resistor R_S . When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator output goes high, which triggers the pulse generator and its output goes high during a fixed pulse time (t_{off}), thus switching off the power feed to the motor winding, and causing the motor current to decrease during t_{off} .

SINGLE-PULSE GENERATOR

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, $t_{\rm off}$, which is determined by the timing components R_t and C_t .

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during toff.

If a new trigger signal should occur during toff, it is ignored.

OUTPUT STAGE

The output stage contains four Darlington transistors and four diodes, connected in an H-bridge. The two sinking transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.

It should be noted however, that it is not permitted to short circuit the outputs.

Vss, Vs, VR

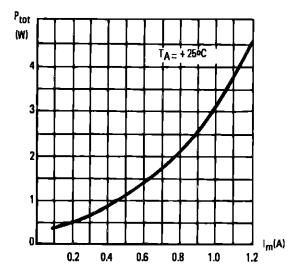
The circuit will stand any order of turn-on or turn-off the supply voltages V_{SS} and V_{S} . Normal dV/dt values are then assumed.

Preferably, V_R should be tracking V_{SS} during power-on and power-off if V_S is established.

ANALOG CONTROL

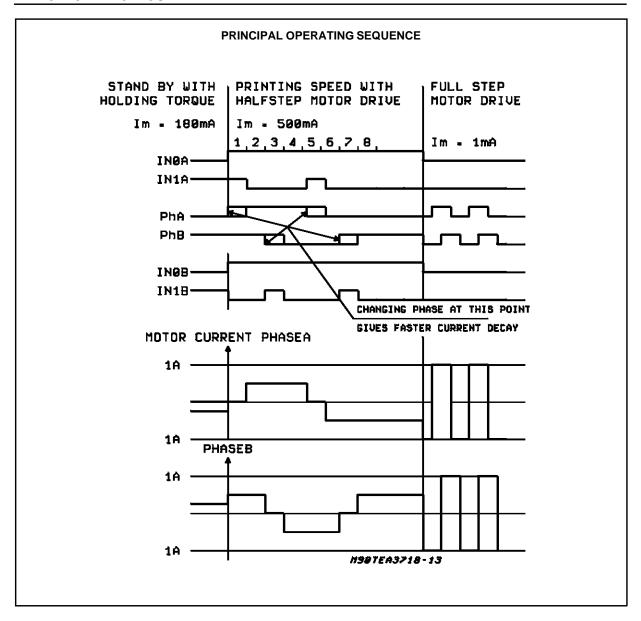
The current levels can be varied continuously if V_R is varied with a circuit varying the voltage on the comparator terminal.

POWER LOSSES VS OUTPUT CURRENT



 $t_{off} = 0.69 \cdot R_t C_t$





APPLICATION NOTES

MOTOR SELECTION

Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.

Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.

UNUSED INPUTS

Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity.

INTERFERENCE

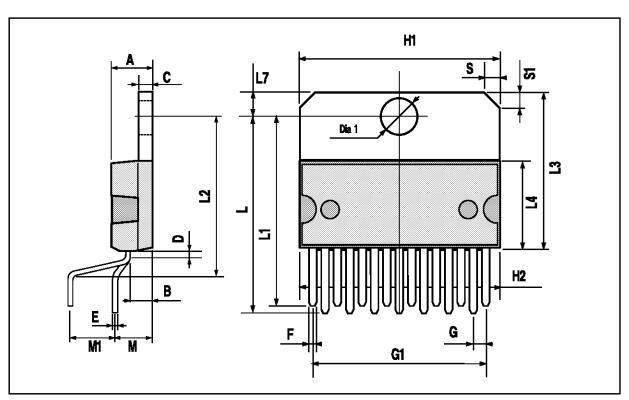
As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 15 nF ceramic capacitor, located near the package between power line V_S and ground.

The ground lead between R_S , C_C and circuit GND should be kept as short as possible. This applies also to the lead between the sensing resistor R_S and point S, see FUNCTIONAL BLOCKS.



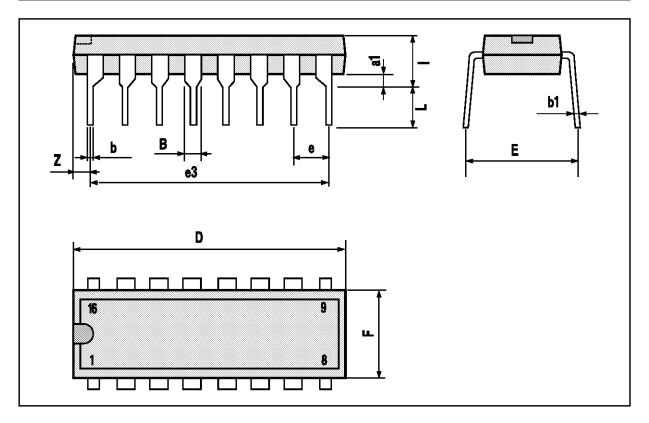
MULTIWATT15 PACKAGE MECHANICAL DATA

DIM.		mm				
DIM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			5			0.197
В			2.65			0.104
С			1.6			0.063
D		1			0.039	
Е	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
М	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



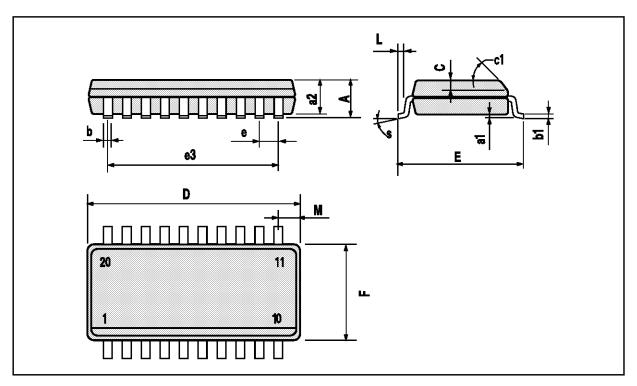
POWERDIP 16 PACKAGE MECHANICAL DATA

DIM.	mm			inch			
 	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
a1	0.51			0.020			
В	0.85		1.40	0.033		0.055	
b		0.50			0.020		
b1	0.38		0.50	0.015		0.020	
D			20.0			0.787	
E		8.80			0.346		
е		2.54			0.100		
e3		17.78			0.700		
F			7.10			0.280	
I			5.10			0.201	
L		3.30			0.130		
Z			1.27			0.050	



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch				
Dim.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
А			2.65			0.104		
a1	0.1		0.3	0.004		0.012		
a2			2.45			0.096		
b	0.35		0.49	0.014		0.019		
b1	0.23		0.32	0.009		0.013		
С		0.5			0.020			
c1		45 (typ.)						
D	12.6		13.0	0.496		0.512		
E	10		10.65	0.394		0.419		
е		1.27			0.050			
e3		11.43			0.450			
F	7.4		7.6	0.291		0.299		
L	0.5		1.27	0.020		0.050		
М			0.75			0.030		
S	8 (max.)							



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