TEXAS INSTRUMENTS

RC4558

SLOS073G – MARCH 1976 – REVISED OCTOBER 2014

RC4558 Dual General-Purpose Operational Amplifier

1 Features

- Continuous Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth: 3 MHz Typ
- Gain and Phase Match Between Amplifiers
- Low Noise: 8 nV/$\sqrt{\text{Hz}}$ Typ at 1 kHz

2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

3 Description

The RC4558 device is a dual general-purpose operational amplifier, with each half electrically similar to the μA741, except that offset null capability is not provided.

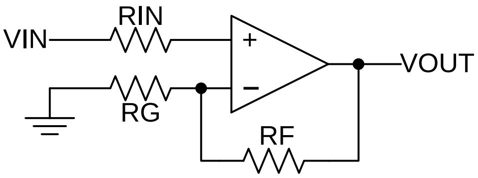
The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected, and the internal frequency compensation ensures stability without external components.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE
RC4558	SOIC (8)	4.90 mm × 3.91 mm
	SOIC (8)	3.00 mm × 3.00 mm
	PDIP (8)	9.81 mm × 6.35 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	SOP (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Noninverting Amplifier Schematic



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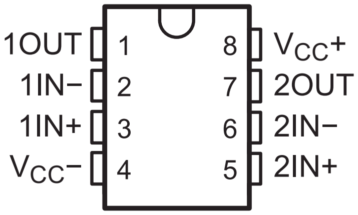
4 Revision History

Changes from Revision F (September 2010) to Revision G **Page**

- Added *Applications*, *Device Information* table, *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Removed *Ordering Information* table. 1

5 Pin Configuration and Functions

D, DGK, P, PS, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN-	2	I	Inverting Input
1OUT	1	O	Output
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting Input
2OUT	7	O	Output
V_{CC}+	8	—	Positive Supply
V_{CC}-	4	—	Negative Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)		18	V
$V_{CC–}$			–18	
V_{ID}	Differential input voltage(3)		±30	V
V_I	Input voltage (any input)(2)(4)		±15	V
	Duration of output short circuit to ground, one amplifier at a time(5)	Unlimited		
T_J	Operating virtual junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	0	500	V
		Charged device model (CDM), per AEC Q100-011 (2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$			–5	–15	
T_A	Operating free-air temperature	RC4558	0	70	°C
		RC4558I	–40	85	

6.4 Thermal Information

THERMAL METRIC(1)		RC4558					UNIT
		D	DGK	P	PS	PW	
		8 PINS					
$R_{θJA}$	Junction-to-ambient thermal resistance	97	172	85	95	149	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = –15 V

PARAMETER			TEST CONDITIONS(1)	T_A (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		V_O = 0	25°C		0.5	6	mV
				Full range			7.5	
I_{IO}	Input offset current		V_O = 0	25°C		5	200	nA
				Full range			300	
I_{IB}	Input bias current		V_O = 0	25°C		150	500	nA
				Full range			800	
V_{ICR}	Common-mode input voltage range			25°C	±12	±14		V
V_{OM}	Maximum output voltage swing		R_L = 10 kΩ	25°C	±12	±14		V
			R_L = 2 kΩ	25°C	±10	±13		
				Full range	±10			
A_{VD}	Large-signal differential voltage amplification		R_L ≥ 2 kΩ, V_O = ±10 V	25°C	20	300		V/mV
				Full range	15			
B_1	Unity-gain bandwidth			25°C		3		MHz
r_i	Input resistance			25°C	0.3	5		MΩ
CMRR	Common-mode rejection ratio			25°C	70	90		dB
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)		V_{CC} = ±15 V to ±9 V	25°C		30	150	μV/V
V_n	Equivalent input noise voltage (closed loop)		A_{VD} = 100, R_S = 100 Ω, f = 1 kHz, BW = 1 Hz	25°C		8		nV/√Hz
I_{CC}	Supply current (both amplifiers)		V_O = 0, No load	25°C		2.5	5.6	mA
				T_A min		3	6.6	
				T_A max		2.3	5	
P_D	Total power dissipation (both amplifiers)		V_O = 0, No load	25°C		75	170	mW
				T_A min		90	200	
				T_A max		70	150	
V_{O1}/V_{O2}	Crosstalk attenuation	Open loop	R_S = 1 kΩ, f = 10 kHz	25°C		85		dB
		A_{VD} = 100				105		

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified.
(2) Full range is 0°C to 70°C for RC4558 and –40°C to 85°C for RC4558I.

6.6 Operating Characteristics

V_{CC+} = 15 V, V_{CC-} = –15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF		0.13		ns
	Overshoot	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF		5%		
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,	C_L = 100 pF	1.1	1.7		V/μs

6.7 Typical Characteristics

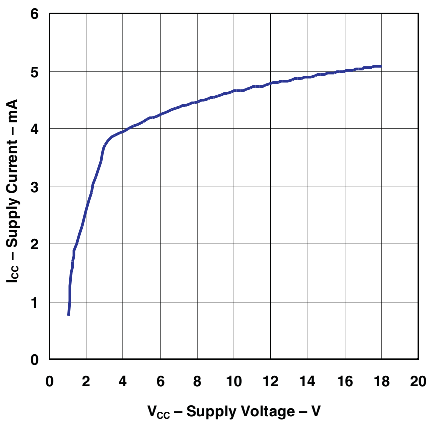


Figure 1. Supply Current vs Supply Voltage
(T_A = 25°C)

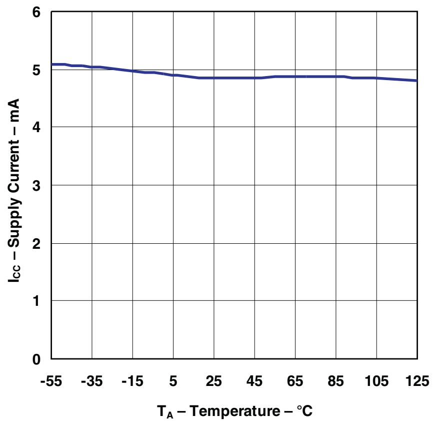


Figure 2. Supply Current vs Temperature
(V_{CC} = ±15 V)

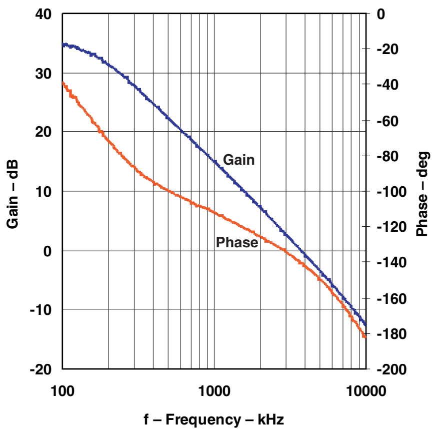


Figure 3. Gain and Phase vs Frequency
(V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 22 pF)

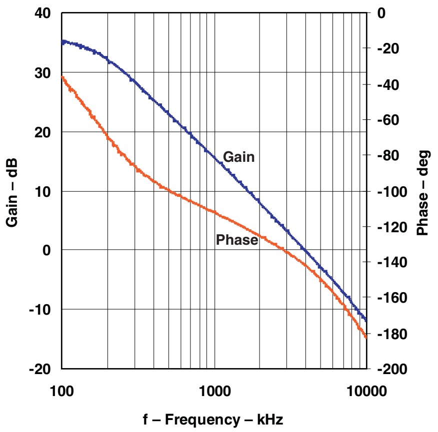


Figure 4. Gain and Phase vs Frequency
(V_{CC} = ±15 V, R_L = 10 kΩ, C_L = 22 pF)

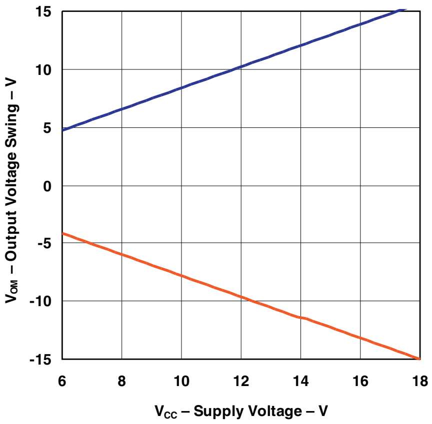


Figure 5. Output Voltage Swing vs Supply Voltage
(R_L = 2 kΩ, T_A = 25°C)

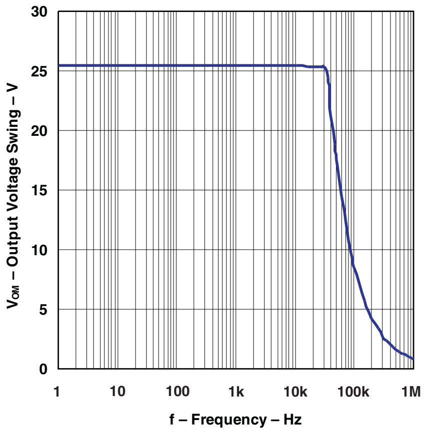


Figure 6. Output Voltage Swing vs Frequency
(V_{CC} = ±15 V, R_L = 2 kΩ, T_A = 25°C)

Typical Characteristics (continued)

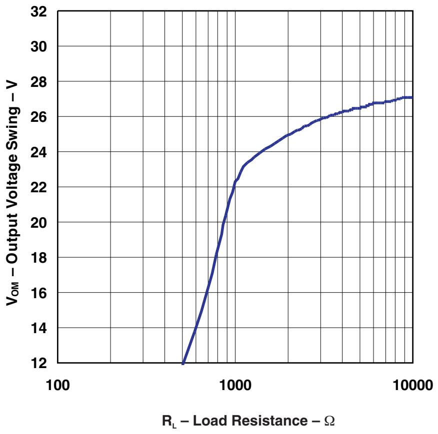


Figure 7. Output Voltage Swing vs Load Resistance (V_{CC} = ±15 V, T_A = 25°C)

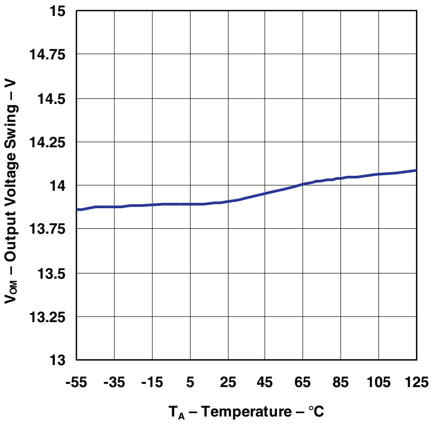


Figure 8. Output Voltage Swing vs Temperature (V_{CC} = ±15 V, R_L = 10 kΩ)

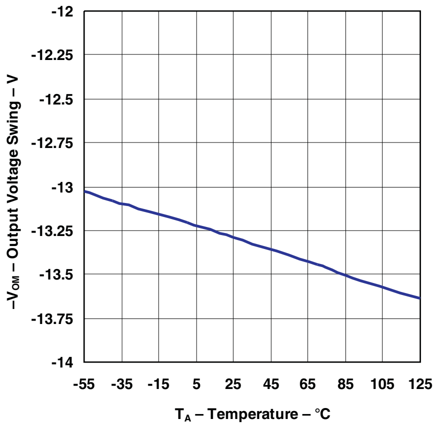


Figure 9. Negative Output Voltage Swing vs Temperature (V_{CC} = ±15 V, R_L = 10 kΩ)

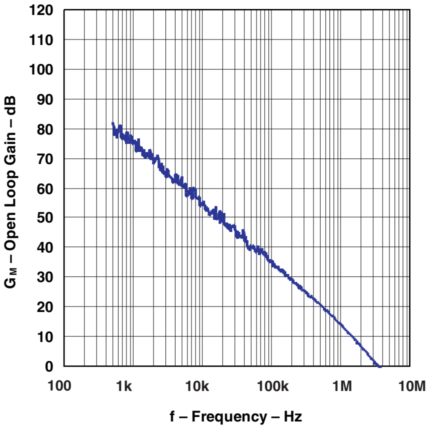


Figure 10. Open Loop Gain vs Frequency (V_{CC} = ±15 V, R_L = 2 kΩ, C_L = 22 pF, T_A = 25°C)

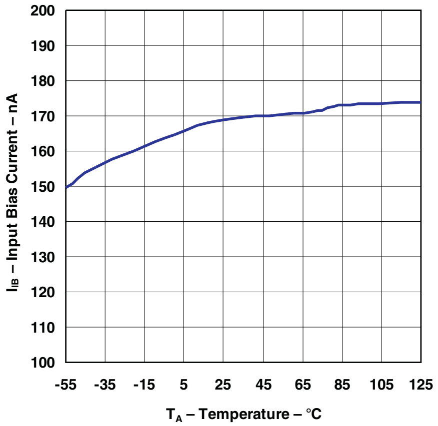


Figure 11. Input Bias Current vs Temperature (V_{CC} = ±15 V)

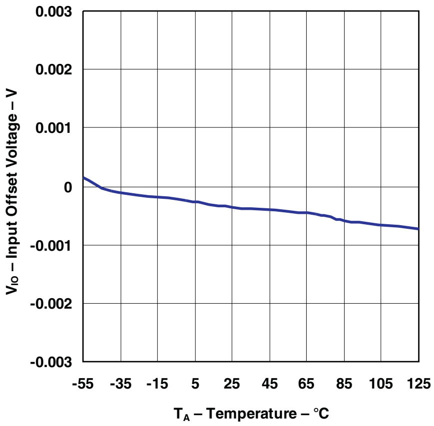


Figure 12. Input Offset Voltage vs Temperature (V_{CC} = ±15 V)

Typical Characteristics (continued)

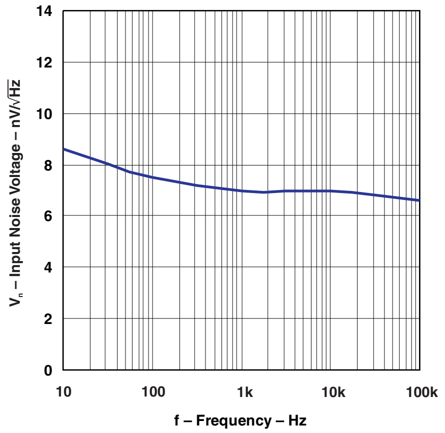


Figure 13. Input Noise Voltage vs Frequency
(V_{CC} = ±15 V, T_A = 25°C)

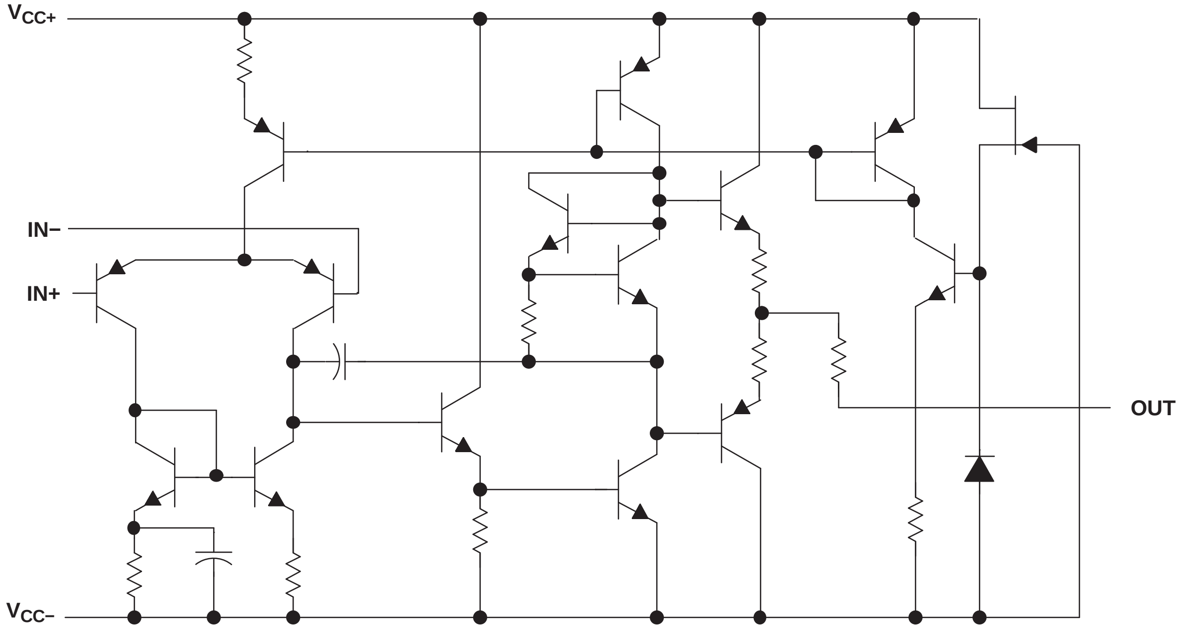
7 Detailed Description

7.1 Overview

The RC4558 device is a dual general-purpose operational amplifier, with each half electrically similar to the µA741, except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected, and the internal frequency compensation ensures stability without external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The RC4558 device has a 3-MHz unity-gain bandwidth.

7.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage, then converting to decibels. Ideally the CMRR is infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the RC4558 device is 90 dB.

7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The RC4558 device has a 1.7 V/µs slew rate.

7.4 Device Functional Modes

The RC4558 device is powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

Some applications require differential signals. Figure 14 shows a simple circuit to convert a single-ended input of 2 V to 10 V into differential output of ±8 V on a single 15-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 2 V to 10 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$.

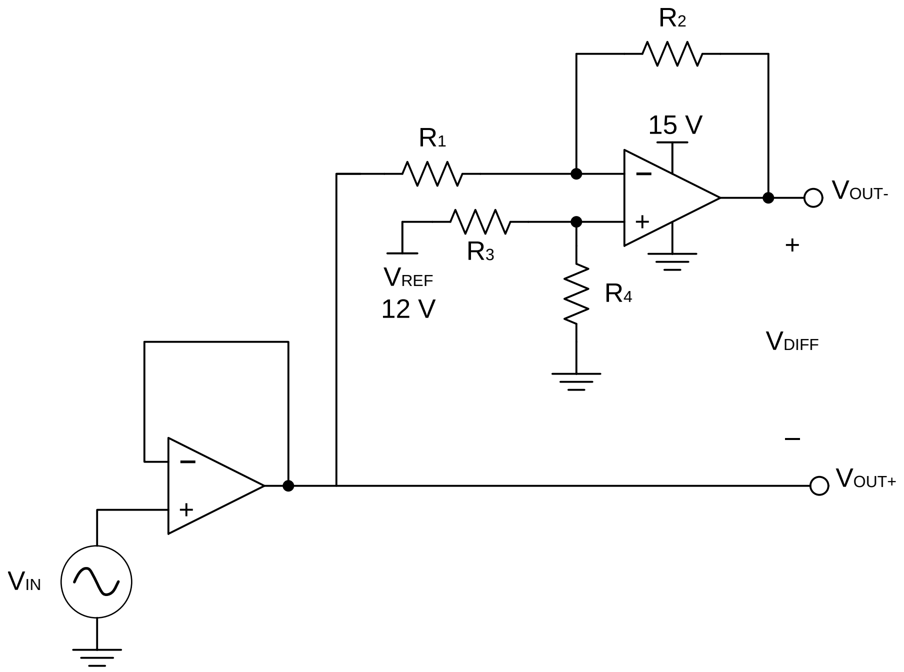


Figure 14. Schematic for Single-Ended Input to Differential Output Conversion

Typical Application (continued)

8.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15 V
- Reference voltage: 12V
- Input: 2 V to 10 V
- Output differential: ±8 V

8.1.2 Detailed Design Procedure

The circuit in Figure 14 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see Equation 1). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

8.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because RC4558 has a bandwidth of 3 MHz, this circuit will only be able to process signals with frequencies of less than 3 MHz.

8.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

Typical Application (continued)

8.1.3 Application Curves

The measured transfer functions in Figure 15, Figure 16, and Figure 17 were generated by sweeping the input voltage from 0 V to 12 V. However, this design should only be used between 2 V and 10 V for optimum linearity.

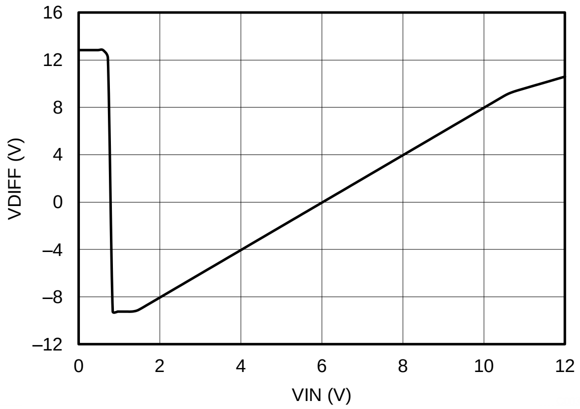


Figure 15. Differential Output Voltage Node vs Input Voltage

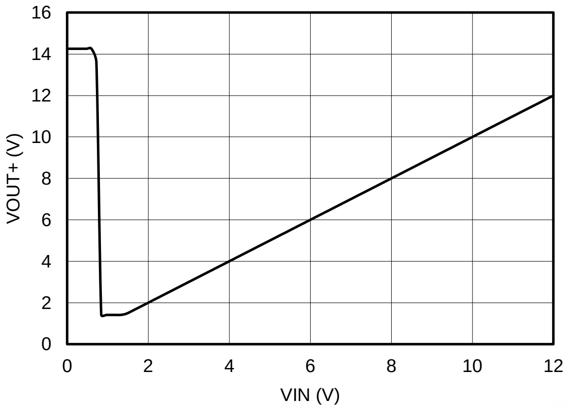


Figure 16. Positive Output Voltage Node vs Input Voltage

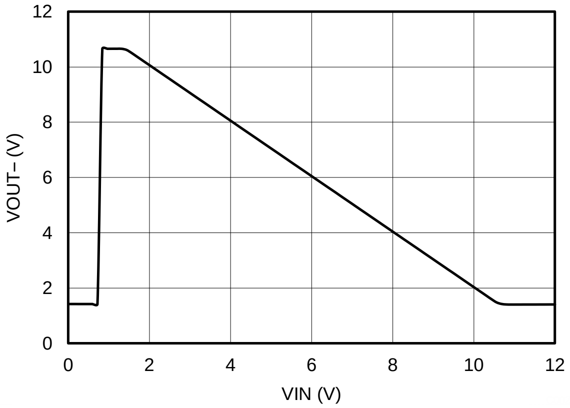


Figure 17. Positive Output Voltage Node vs Input Voltage

9 Power Supply Recommendations

The RC4558 device is specified for operation from ±5 V to ±15 V; many specifications apply from –0°C to 70°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages outside of the ±18-V range can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

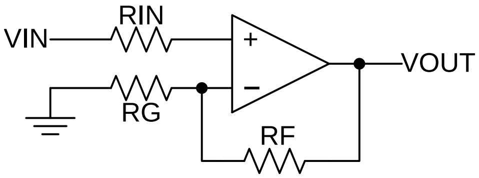


Figure 18. Operational Amplifier Schematic for Noninverting Configuration

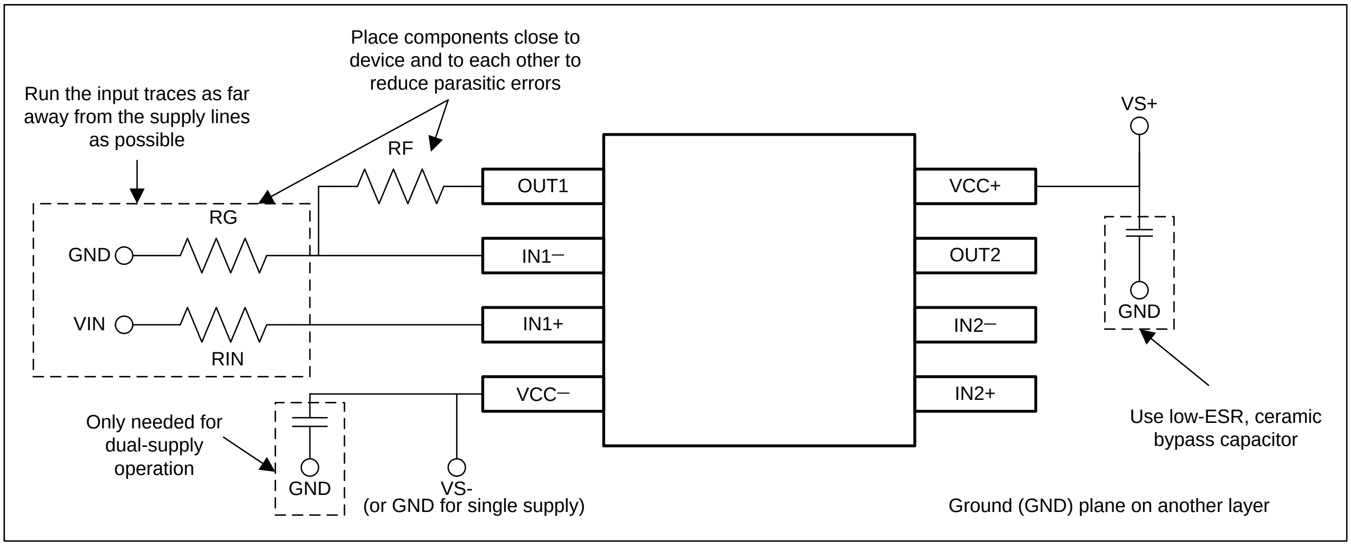


Figure 19. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.3 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4558-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples
RC4558D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YRP ~ YRS ~ YRU)	Samples
RC4558DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(YRP ~ YRS ~ YRU)	Samples
RC4558DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RC4558	Samples
RC4558ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(YSP ~ YSS ~ YSU)	Samples
RC4558IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(YSP ~ YSS ~ YSU)	Samples
RC4558IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	RC4558IP	Samples
RC4558IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	RC4558IP	Samples
RC4558IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
RC4558IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	R4558I	Samples
RC4558IPWRE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		Samples
RC4558IPWRG4	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		
RC4558P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	RC4558P	Samples
RC4558PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	RC4558P	Samples
RC4558PSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
RC4558PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
RC4558PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	0 to 70	R4558	Samples
RC4558PWRE4	ACTIVE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		Samples
RC4558PWRG4	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
RC4558Y	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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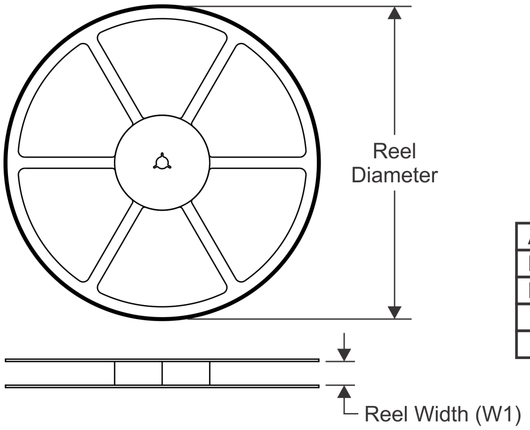
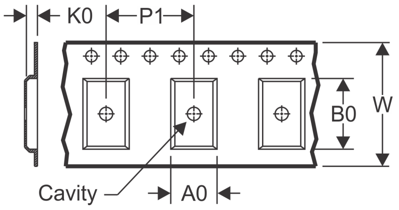
TAPE AND REEL INFORMATION

REEL DIMENSIONS

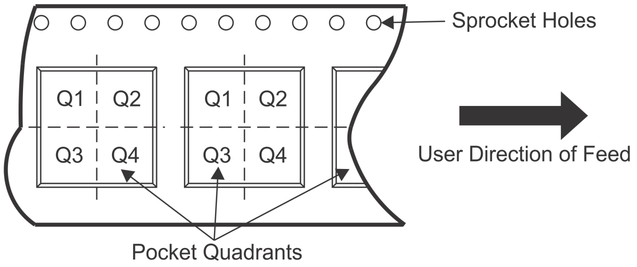


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

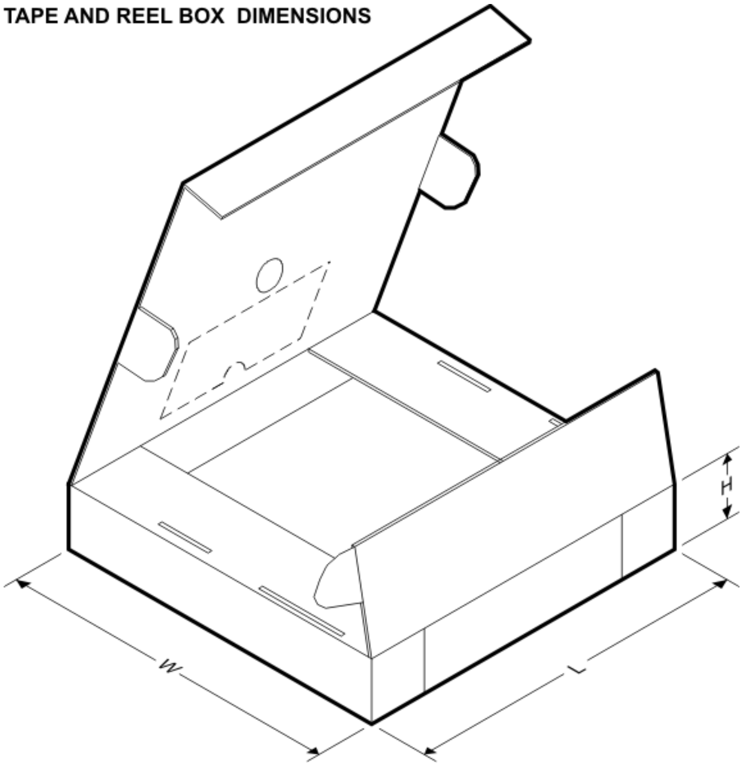
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
RC4558DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
RC4558IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
RC4558IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
RC4558PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
RC4558PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

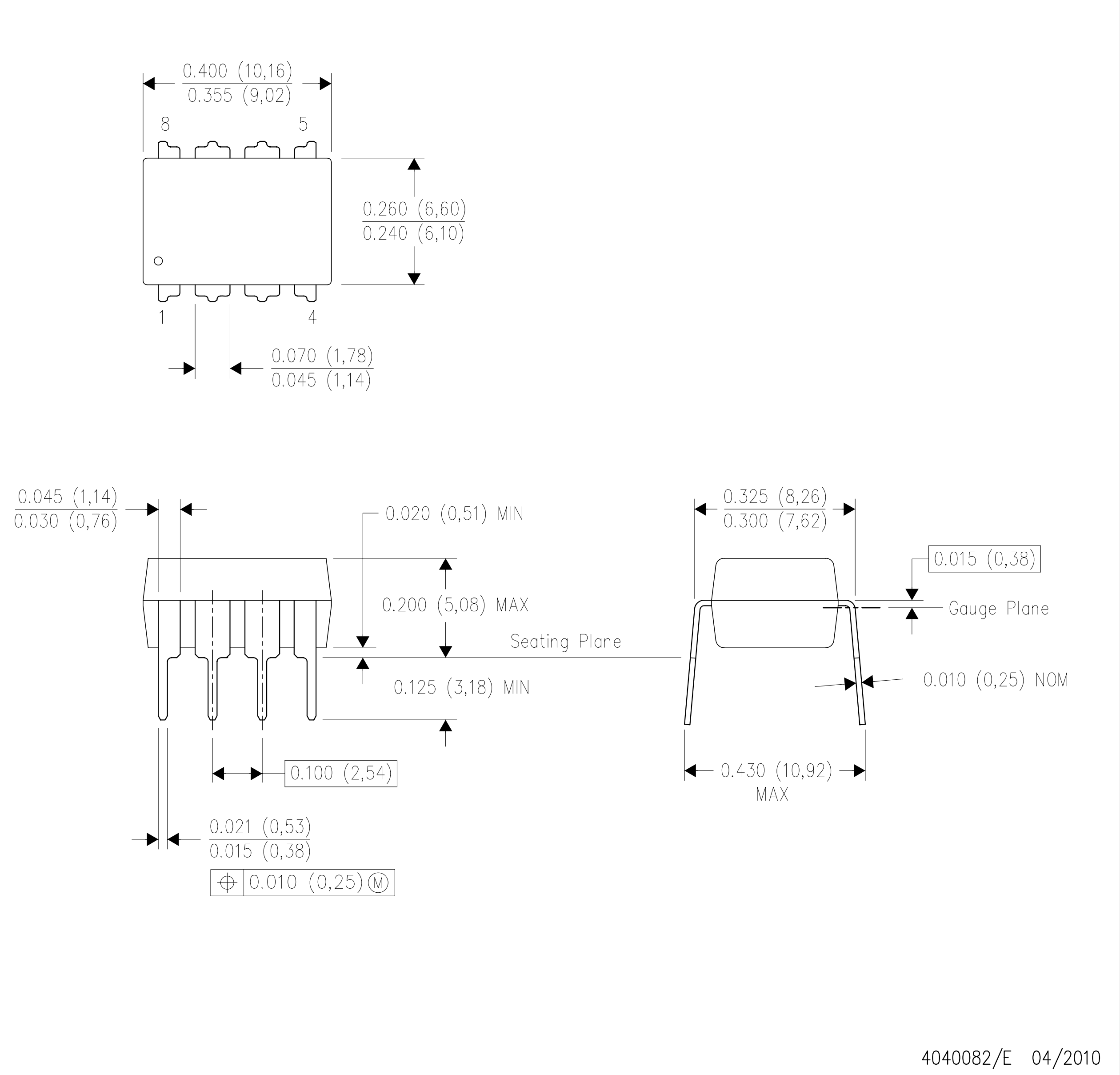
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
RC4558DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
RC4558DR	SOIC	D	8	2500	364.0	364.0	27.0
RC4558DR	SOIC	D	8	2500	340.5	338.1	20.6
RC4558DR	SOIC	D	8	2500	367.0	367.0	35.0
RC4558DRG3	SOIC	D	8	2500	364.0	364.0	27.0
RC4558DRG4	SOIC	D	8	2500	367.0	367.0	35.0
RC4558DRG4	SOIC	D	8	2500	340.5	338.1	20.6
RC4558IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
RC4558IDR	SOIC	D	8	2500	340.5	338.1	20.6
RC4558IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
RC4558IPWR	TSSOP	PW	8	2000	364.0	364.0	27.0
RC4558PSR	SO	PS	8	2000	367.0	367.0	38.0
RC4558PWR	TSSOP	PW	8	2000	364.0	364.0	27.0

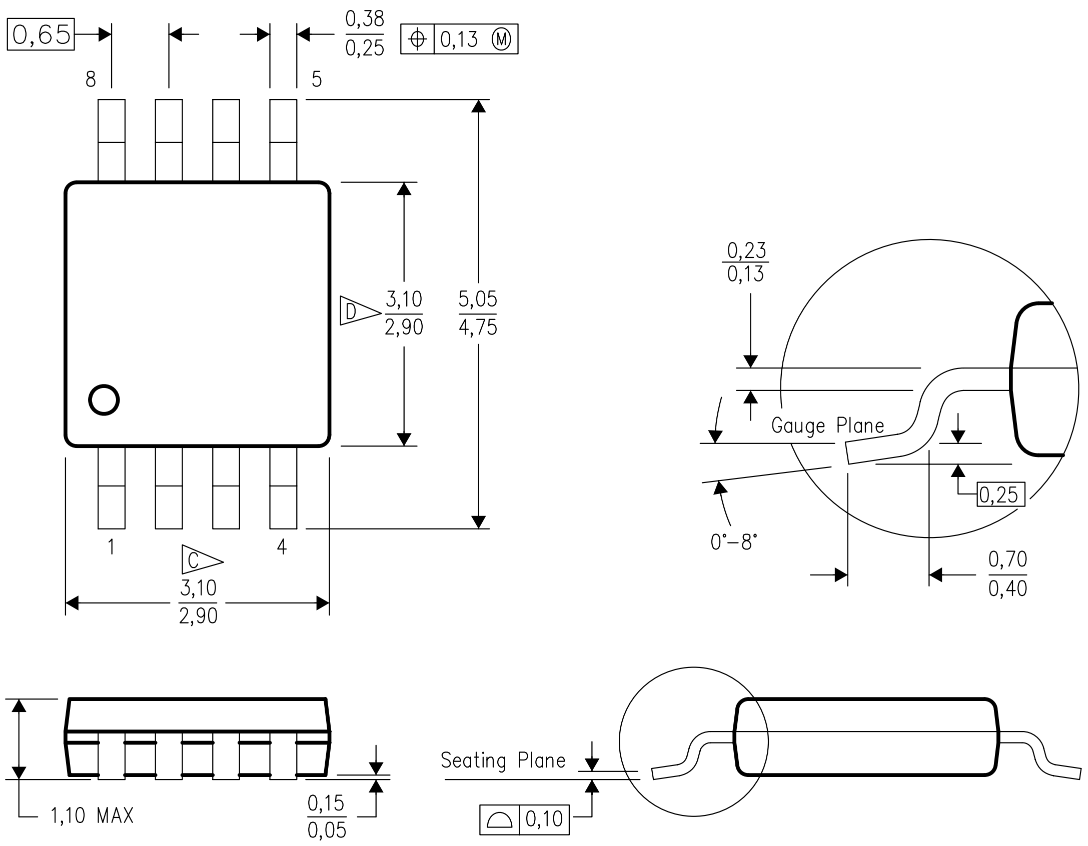
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

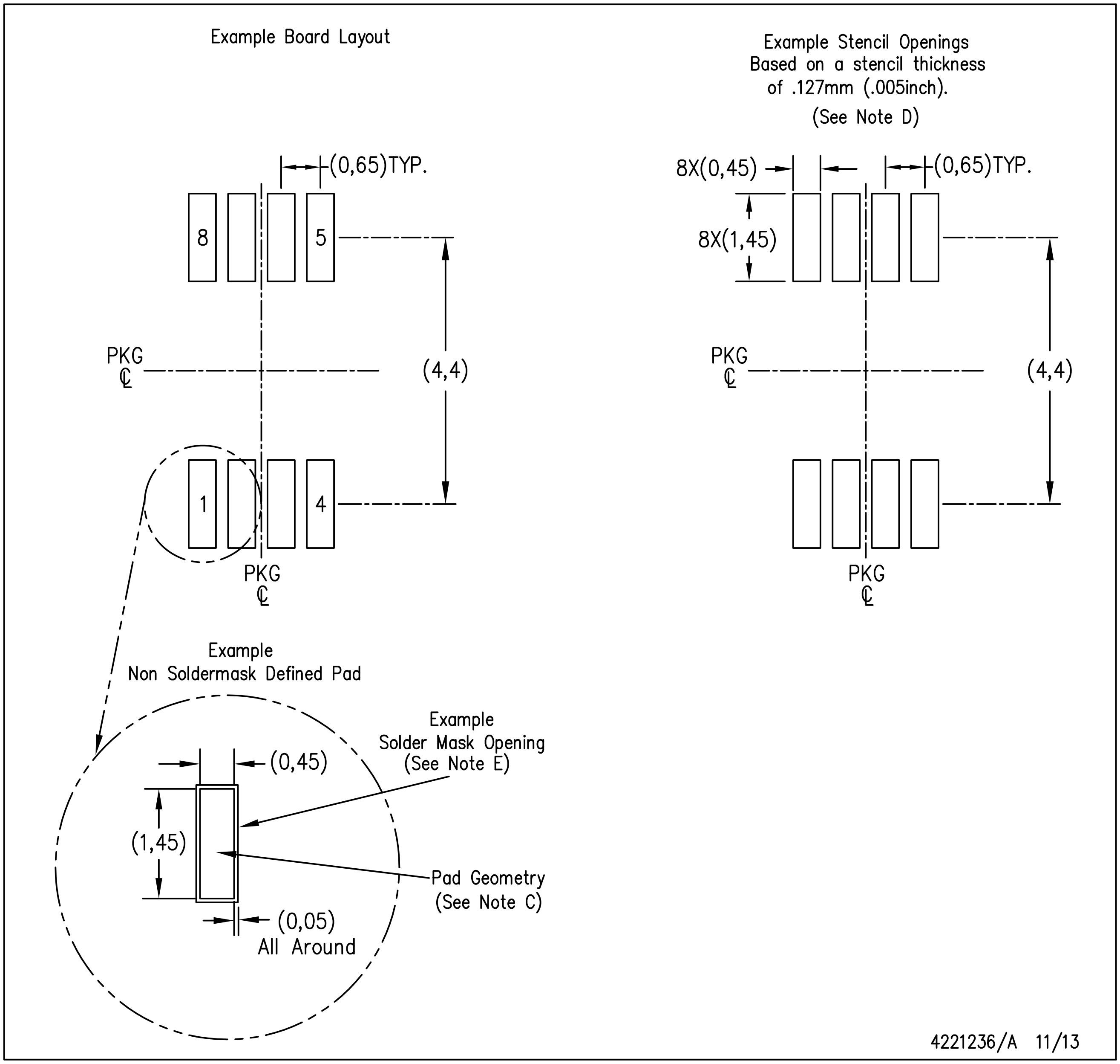
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



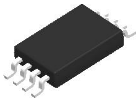
4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



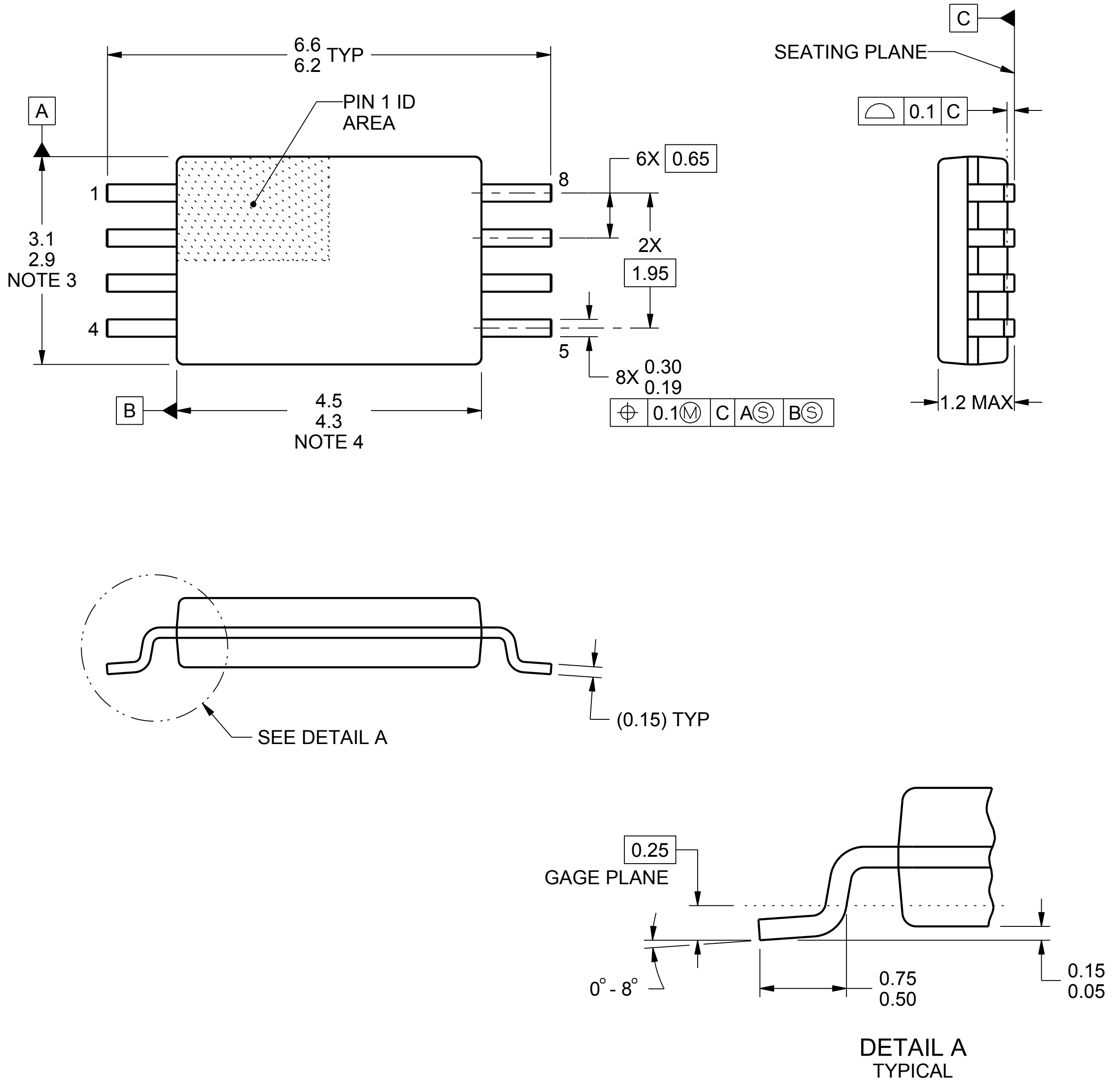
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

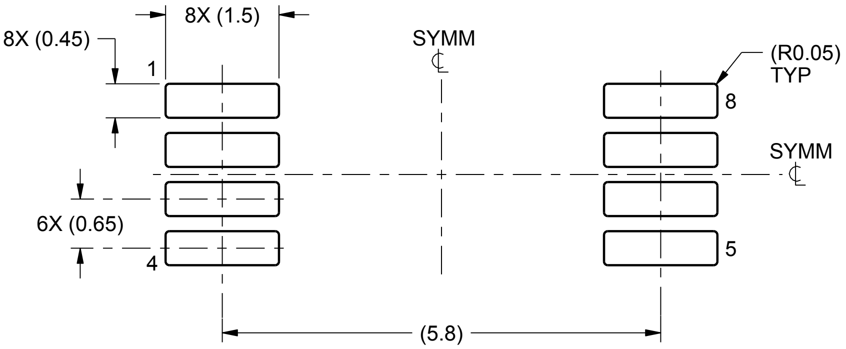
SMALL OUTLINE PACKAGE



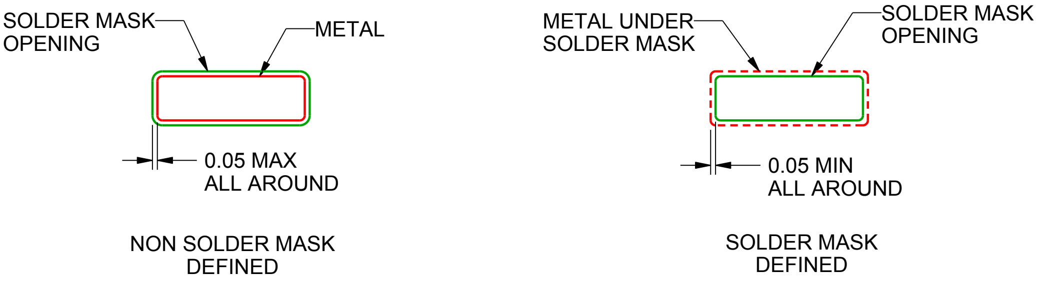
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

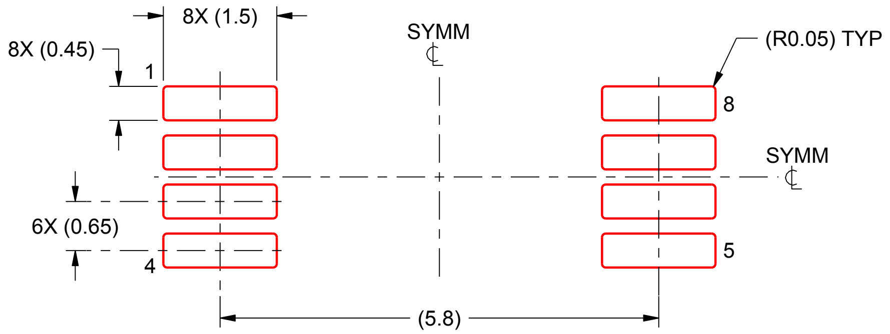


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



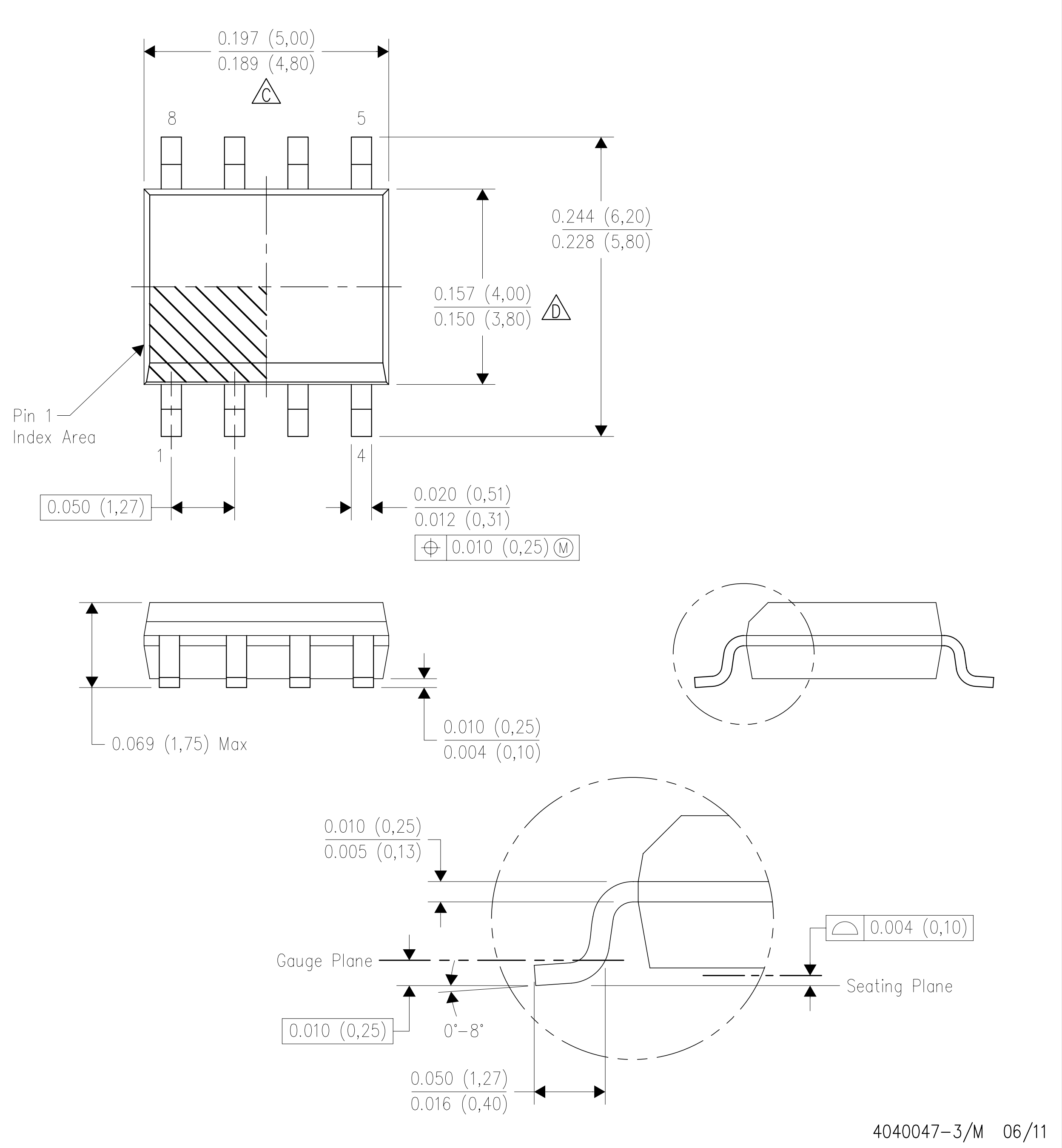
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

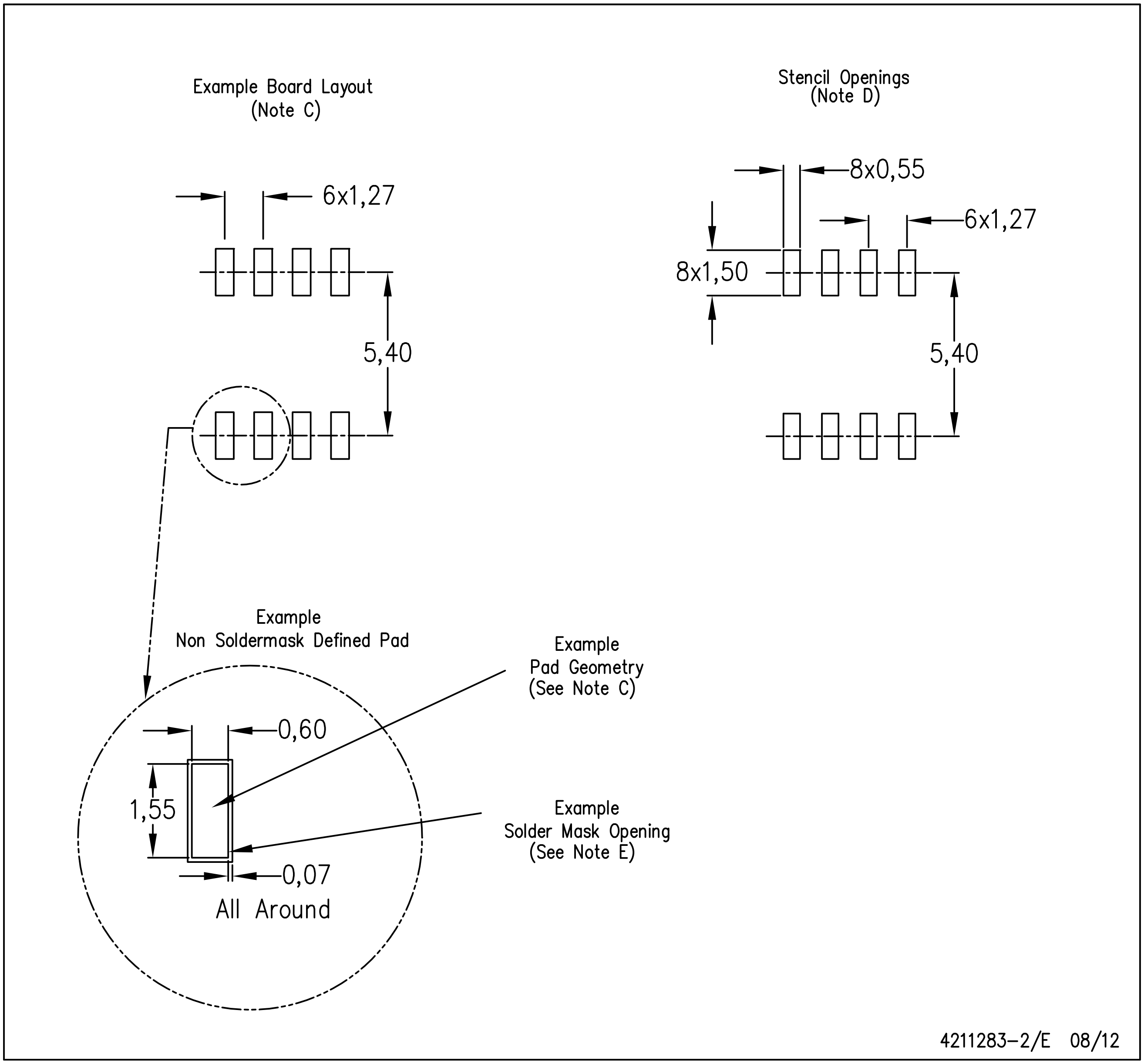
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

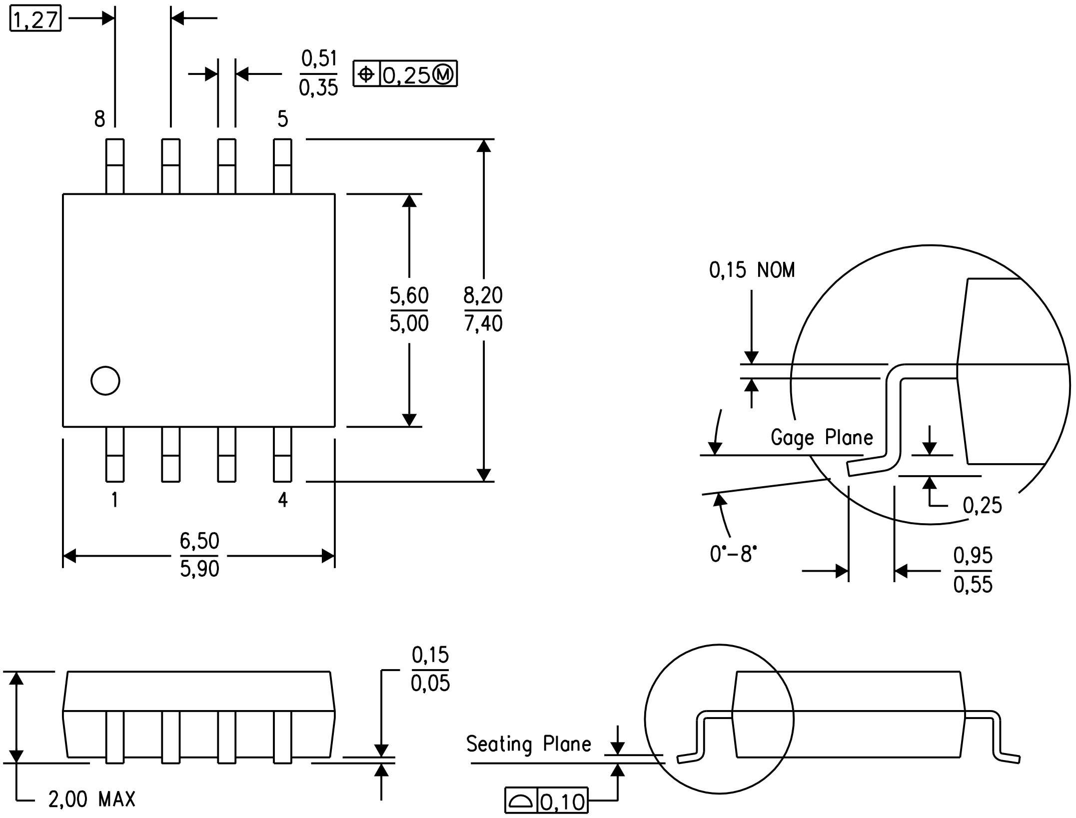


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



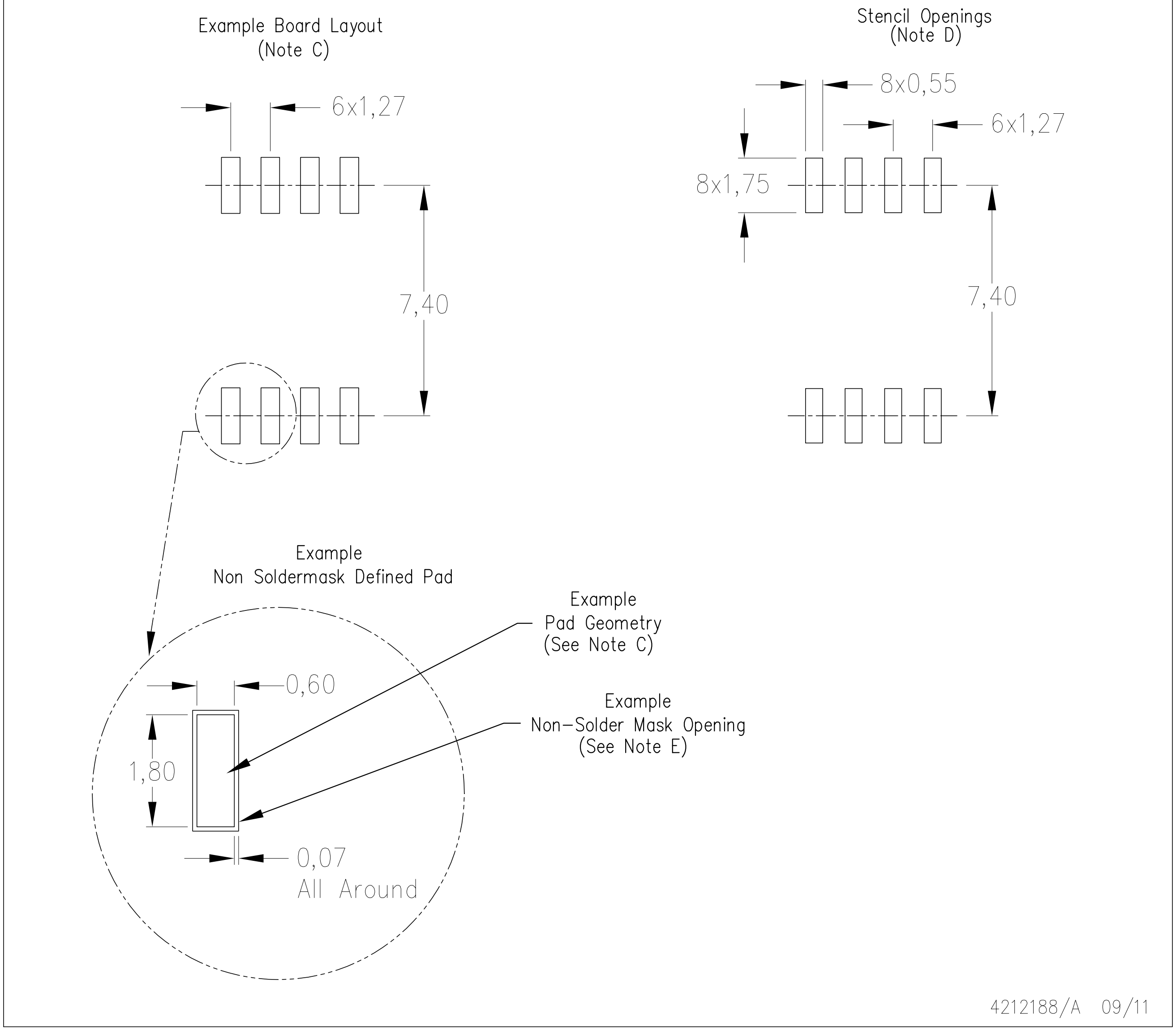
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



4212188/A 09/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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