MC74HC595A

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

High−Performance Silicon−Gate CMOS

The MC74HC595A consists of an 8−bit shift register and an 8−bit D−type latch with three−state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8−bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

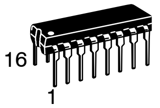
The HC595A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

Features

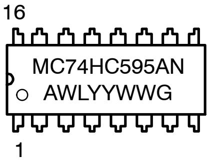
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - Improved Propagation Delays
  - 50% Lower Quiescent Power
  - Improved Input Noise and Latchup Immunity
- Pb−Free Packages are Available*

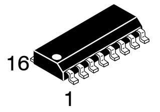
ON Semiconductor®

MARKING DIAGRAMS

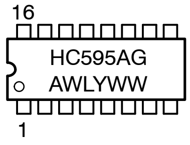


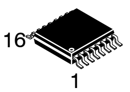
PDIP−16
N SUFFIX
CASE 648



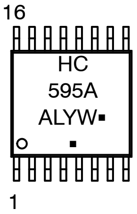


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G, ▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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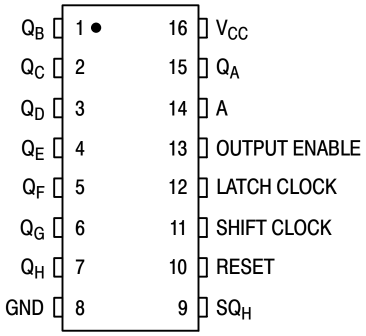
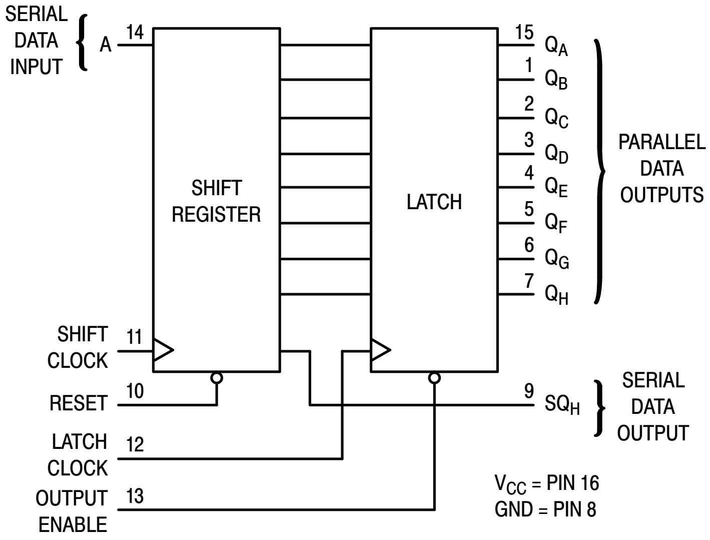
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Publication Order Number:
MC74HC595A/D

PIN ASSIGNMENT



LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
MC74HC595AN	PDIP−16	500 Units / Rail
MC74HC595ANG	PDIP−16 (Pb−Free)	500 Units / Rail
MC74HC595AD	SOIC−16	48 Units / Rail
MC74HC595ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC595ADR2	SOIC−16	2500 Tape & Reel
MC74HC595ADR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74HC595ADT	TSSOP−16*	96 Units / Rail
MC74HC595ADTR2	TSSOP−16*	2500 Tape & Reel
MC74HC595ADTR2G	TSSOP−16* (Pb−Free)	2500 Tape & Reel
MC74HC595AFEL	SOEIAJ−16	2000 Tape & Reel
MC74HC595AFELG	SOEIAJ−16 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V	0	1000	ns
	V_{CC} = 4.5 V	0	500	
	V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out}\rvert \leq 20\ \mu A$	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out}\rvert \leq 20\ \mu A$	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V_{OH}	Minimum High−Level Output Voltage, Q_A − Q_H	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \leq 20\ \mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert \leq 2.4$ mA	3.0	2.48	2.34	2.2	
		$\lvert I_{out}\rvert \leq 6.0$ mA	4.5	3.98	3.84	3.7	
		$\lvert I_{out}\rvert \leq 7.8$ mA	6.0	5.48	5.34	5.2	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low−Level Output Voltage, Q_A – Q_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 2.4$ mA $\lvert I_{out} \rvert \leq 6.0$ mA $\lvert I_{out} \rvert \leq 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
V_{OH}	Minimum High−Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 2.4$ mA $\lvert I_{out} \rvert \leq 4.0$ mA $\lvert I_{out} \rvert \leq 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low−Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 2.4$ mA $\lvert I_{out} \rvert \leq 4.0$ mA $\lvert I_{out} \rvert \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three−State Leakage Current, Q_A – Q_H	Output in High−Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	2.0 3.0 4.5 6.0	145 100 29 25	180 125 36 31	220 150 44 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to Q_A – Q_H (Figures 3 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q_A – Q_H (Figures 4 and 8)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q_A – Q_H (Figures 4 and 8)	2.0 3.0 4.5 6.0	135 90 27 23	170 110 34 29	205 130 41 35	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Q_A – Q_H (Figures 3 and 7)	2.0	60	75	90	ns
		3.0	23	27	31	
		4.5	12	15	18	
		6.0	10	13	15	
t_{TLH}, t_{THL}	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State), Q_A – Q_H	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	300	pF

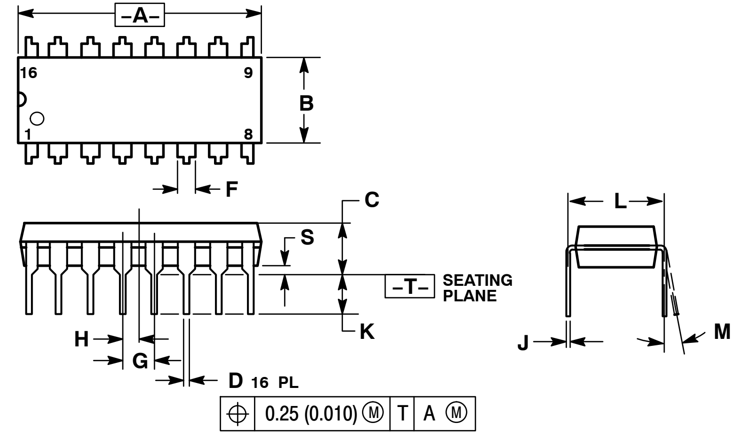
* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to –55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0	75	95	110	ns
		3.0	60	70	80	
		4.5	15	19	22	
		6.0	13	16	19	
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0	5.0	5.0	5.0	ns
		3.0	5.0	5.0	5.0	
		4.5	5.0	5.0	5.0	
		6.0	5.0	5.0	5.0	
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	60	75	90	ns
		3.0	45	60	70	
		4.5	12	15	18	
		6.0	10	13	15	
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

PACKAGE DIMENSIONS

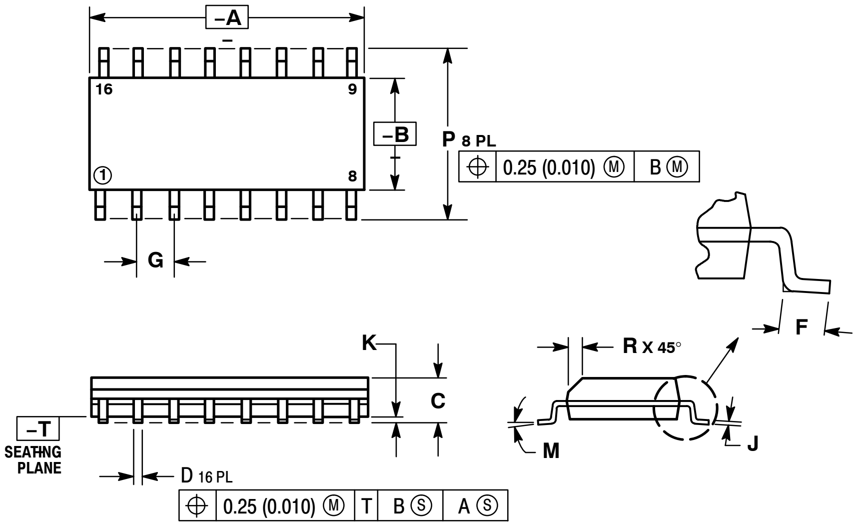
PDIP−16
N SUFFIX
CASE 648−08
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

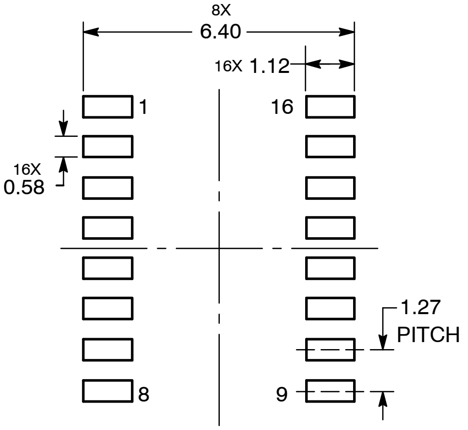
SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS