



# Low-Noise, Low-Distortion INSTRUMENTATION AMPLIFIER Replacement for SSM2017

## FEATURES

- **LOW NOISE:** 1.3nV/ $\sqrt{\text{Hz}}$  at 1kHz
- **LOW THD+N:** 0.004% at 1kHz, G = 100
- **WIDE BANDWIDTH:** 800kHz at G = 100
- **WIDE SUPPLY RANGE:**  $\pm 4.5\text{V}$  to  $\pm 18\text{V}$
- **HIGH CMR:** > 100dB
- **GAIN SET WITH EXTERNAL RESISTOR**
- **DIP-8 AND SOL-16 WIDEBODY PACKAGES**

## APPLICATIONS

- **PROFESSIONAL MICROPHONE PREAMPS**
- **MOVING-COIL TRANSDUCER AMPLIFIERS**
- **DIFFERENTIAL RECEIVERS**
- **BRIDGE TRANSDUCER AMPLIFIERS**

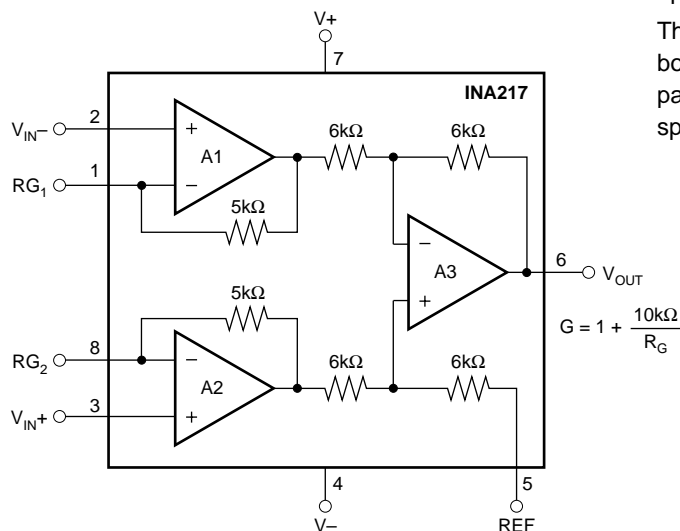
## DESCRIPTION

The INA217 is a low-noise, low-distortion, monolithic instrumentation amplifier. Current-feedback circuitry allows the INA217 to achieve wide bandwidth and excellent dynamic response over a wide range of gain. The INA217 is ideal for low-level audio signals such as balanced low-impedance microphones. Many industrial, instrumentation, and medical applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. The INA217 provides near-theoretical noise performance for 200 $\Omega$  source impedance. The INA217 features differential input, low noise, and low distortion that provides superior performance in professional microphone amplifier applications.

The INA217 features wide supply voltage, excellent output voltage swing, and high output current drive, making it an optimal candidate for use in high-level audio stages.

The INA217 is available in the same DIP-8 and SOL-16 wide body packages and pinouts as the SSM2017. For a smaller package, see the INA163 in SO-14 narrow. The INA217 is specified over the temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V+ to V-	±18V
Signal Input Terminals, Voltage <sup>(2)</sup>	(V-) - 0.5V to (V+) + 0.5V
Current <sup>(2)</sup>	10mA
Output Short-Circuit <sup>(3)</sup>	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

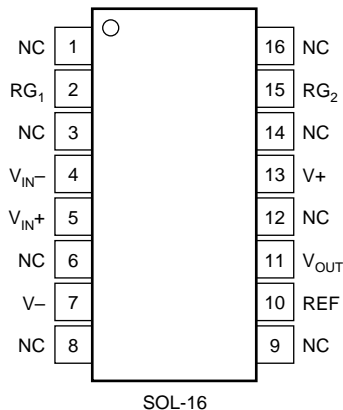
## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA217	SOL-16	DW	INA217
INA217	DIP-8	P	INA217

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

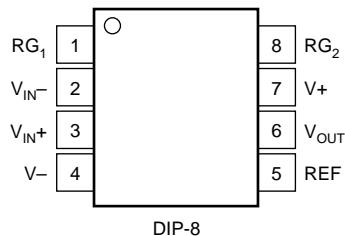
## PIN CONFIGURATIONS

### Top View



SOL-16

NC = No Internal Connection



DIP-8

# ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ .

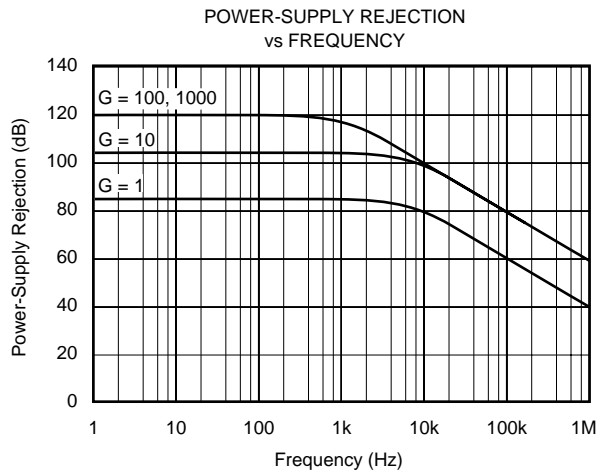
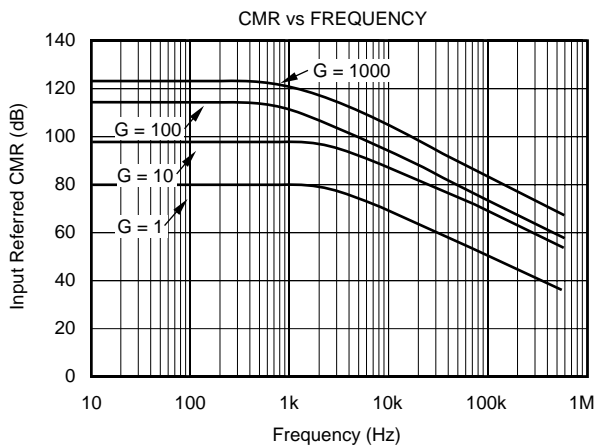
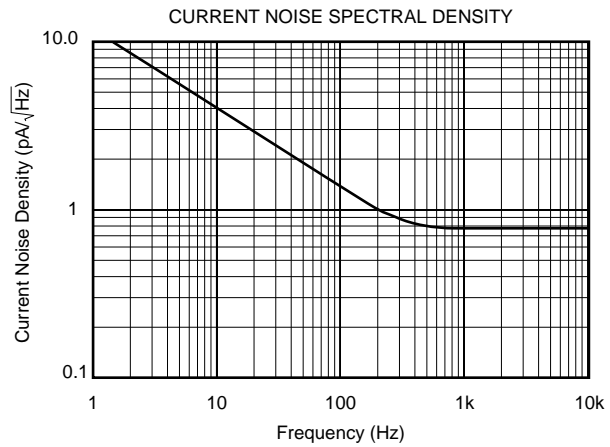
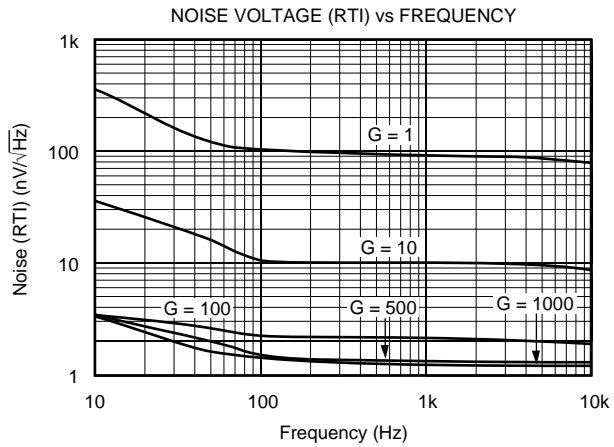
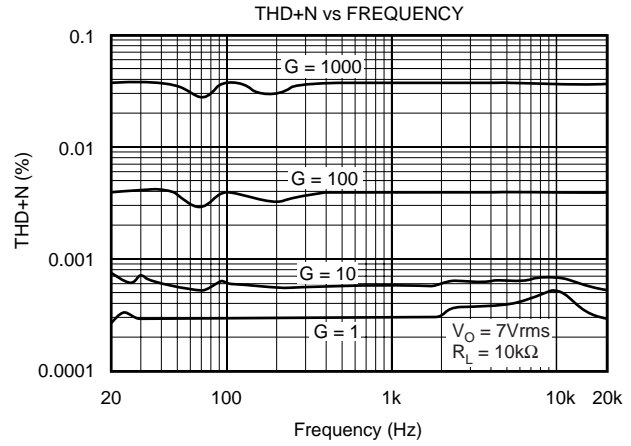
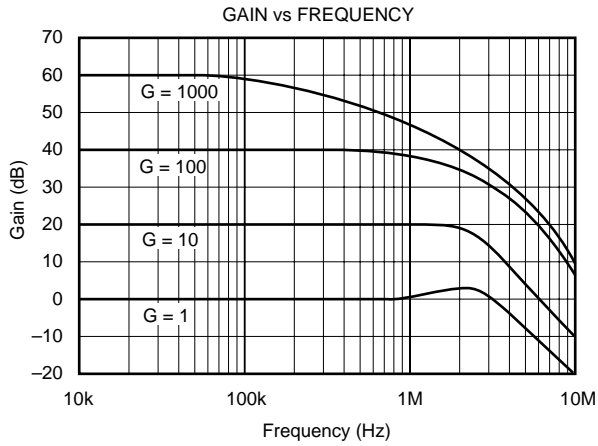
$T_A = +25^{\circ}C$ ,  $R_L = 2k\Omega$ ,  $V_S = \pm 15V$ , unless otherwise noted.

PARAMETER	CONDITIONS	INA217			UNITS
		MIN	TYP	MAX	
<b>GAIN EQUATION</b> Range Gain Error, $G = 1$ $G = 10$ $G = 100$ $G = 1000$ <b>Gain Temp Drift Coefficient, <math>G = 1</math></b> $G > 10$ Nonlinearity, $G = 1$ $G = 100$			$G = 1 + 10k/R_G$ 1 to 10000 $\pm 0.1$ $\pm 0.2$ $\pm 0.5$ $\pm 3$ $\pm 40$ $\pm 0.0003$ $\pm 0.0006$	$\pm 0.25$ $\pm 0.7$  $\pm 10$ $\pm 100$	V/V % % % % <b>ppm/<math>^{\circ}C</math></b> <b>ppm/<math>^{\circ}C</math></b> % of FS % of FS
<b>INPUT STAGE NOISE</b> Voltage Noise $f_O = 1kHz$ $f_O = 100Hz$ $f_O = 10Hz$ Current Noise $f_O = 1kHz$	$R_{SOURCE} = 0\Omega$		1.3 1.5 3.5  0.8		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$  $pA/\sqrt{Hz}$
<b>OUTPUT STAGE NOISE</b> Voltage Noise, $f_O = 1kHz$			90		$nV/\sqrt{Hz}$
<b>INPUT OFFSET VOLTAGE</b> Input Offset Voltage <b>vs Temperature</b> vs Power Supply	$V_{CM} = V_{OUT} = 0V$ $T_A = T_{MIN}$ to $T_{MAX}$ $V_S = \pm 4.5V$ to $\pm 18V$		$50 + 2000/G$ $1 + 20/G$ $1 + 50/G$	$250 + 5000/G$ $3 + 200/G$	$\mu V$ $\mu V/^{\circ}C$ $\mu V/V$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range  Common-Mode Rejection, $G = 1$ $G = 100$	$V_{IN+} - V_{IN-} = 0V$ $V_{IN+} - V_{IN-} = 0V$ $V_{CM} = \pm 11V$ , $R_{SRC} = 0\Omega$	$(V+) - 4$ $(V-) + 4$ 70 100	$(V+) - 3$ $(V-) + 3$ 80 116		V V dB dB
<b>INPUT BIAS CURRENT</b> Initial Bias Current <b>vs Temperature</b> Initial Offset Current <b>vs Temperature</b>			2 $10$ 0.1 $0.5$	12  1	$\mu A$ <b>nA/<math>^{\circ}C</math></b> $\mu A$ <b>nA/<math>^{\circ}C</math></b>
<b>INPUT IMPEDANCE</b>	Differential Common-Mode		$60 \parallel 2$ $60 \parallel 2$		$M\Omega \parallel pF$ $M\Omega \parallel pF$
<b>DYNAMIC RESPONSE</b> Bandwidth, Small Signal, $-3dB$ , $G = 1$ $G = 100$  Slew Rate THD+Noise, $f = 1kHz$ Settling Time, 0.1% 0.01% Overload Recovery	$G = 100$ $G = 100$ , 10V Step $G = 100$ , 10V Step 50% Overdrive		3.4 800 15 0.004 2 3.5 1		MHz kHz V/ $\mu s$ % $\mu s$ $\mu s$ $\mu s$
<b>OUTPUT</b> Voltage  Load Capacitance Stability Short-Circuit Current	$R_L$ to GND  Continuous-to-Common	$(V+) - 2$ $(V-) + 2$	$(V+) - 1.8$ $(V-) + 1.8$ 1000 $\pm 60$		V V pF mA
<b>POWER SUPPLY</b> Rated Voltage Voltage Range Current, Quiescent	$I_O = 0mA$	$\pm 4.5$	$\pm 15$  $\pm 10$	$\pm 18$  $\pm 12$	V V mA
<b>TEMPERATURE RANGE</b> Specification Operating Thermal Resistance DIP-8 SOL-16	$\theta_{JA}$	$-40$ $-40$		$+85$ $+125$	$^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$

NOTE: (1) Gain accuracy is a function of external  $R_G$ .

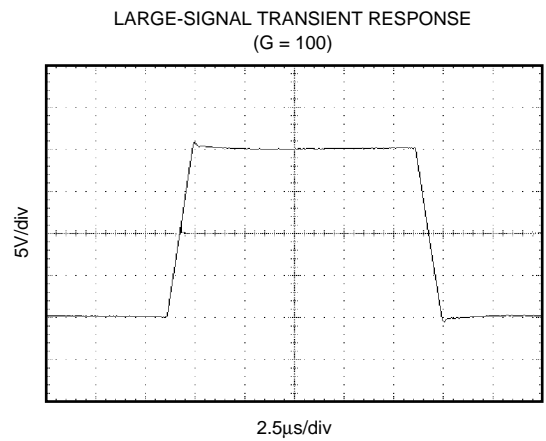
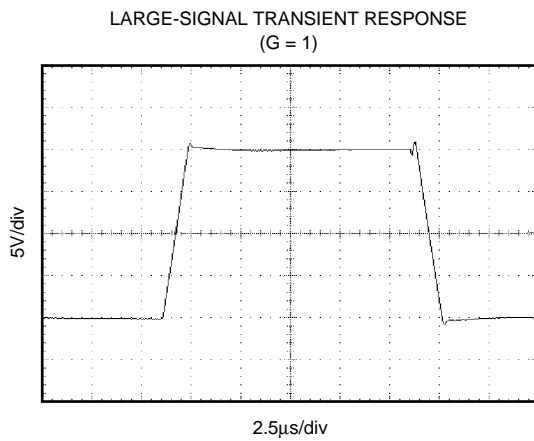
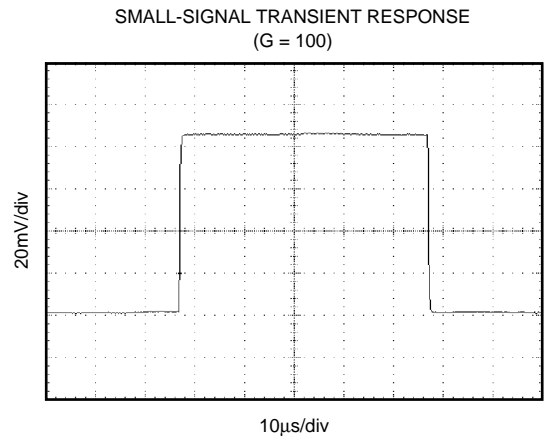
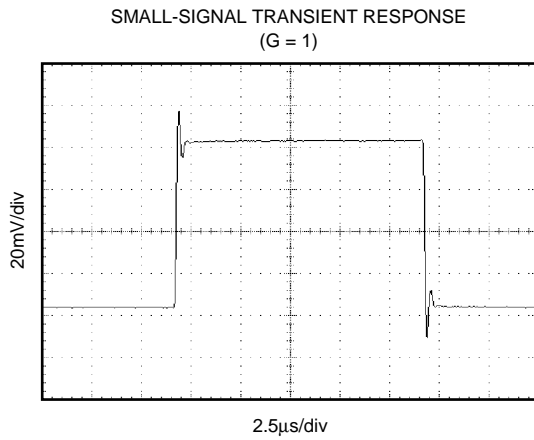
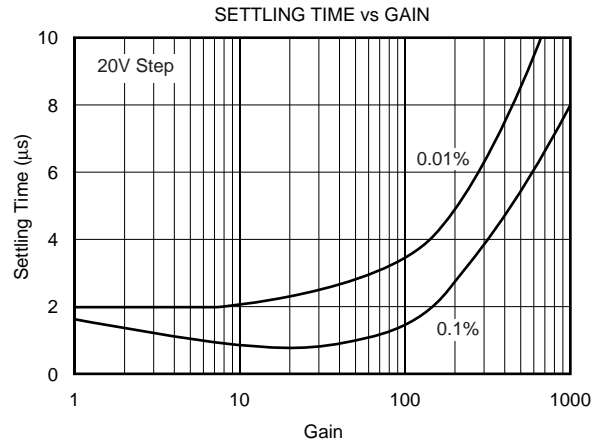
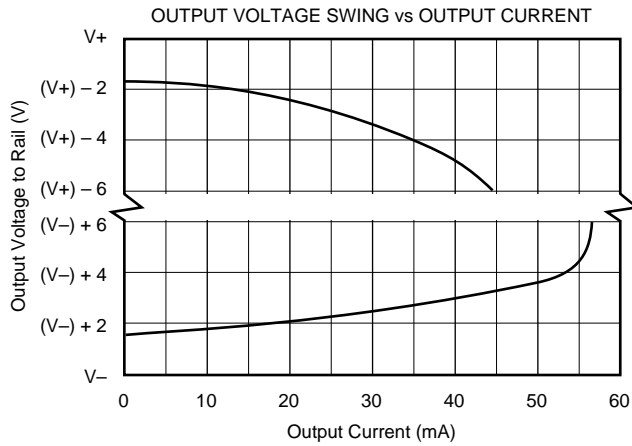
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ ,  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation. Power supplies should be bypassed with 0.1μF tantalum capacitors near the device pins. The output Reference (pin 5) should be a low-impedance connection. Resistance of a few ohms in series with this connection will degrade the common-mode rejection of the INA217.

## GAIN-SET RESISTOR

Gain is set with an external resistor,  $R_G$ , as shown in Figure 1. The two internal 5kΩ feedback resistors are laser-trimmed to 5kΩ within approximately ±0.2%. The gain equation for the INA217 is:

$$G = 1 + \frac{10,000}{R_G}$$

The temperature coefficient of the internal 5kΩ resistors is approximately ±25ppm/°C. Accuracy and TCR of the external  $R_G$  will also contribute to gain error and temperature drift. These effects can be inferred from the gain equation. Make a short, direct connection to the gain set resistor,  $R_G$ . Avoid running output signals near these sensitive input nodes.

## NOISE PERFORMANCE

The INA217 provides very low noise with low-source impedance. Its 1.3nV/√Hz voltage noise delivers near-theoretical noise performance with a source impedance of 200Ω. The input stage design used to achieve this low noise results in

relatively high input bias current and input bias current noise. As a result, the INA217 may not provide the best noise performance with a source impedance greater than 10kΩ. For source impedance greater than 10kΩ, other instrumentation amplifiers may provide improved noise performance.

## INPUT CONSIDERATIONS

Very low source impedance (less than 10Ω) can cause the INA217 to oscillate. This depends on circuit layout, signal source, and input cable characteristics. An input network consisting of a small inductor and resistor, as shown in Figure 2, can greatly reduce any tendency to oscillate. This is especially useful if a variety of input sources are to be connected to the INA217. Although not shown in other figures, this network can be used as needed with all applications shown.

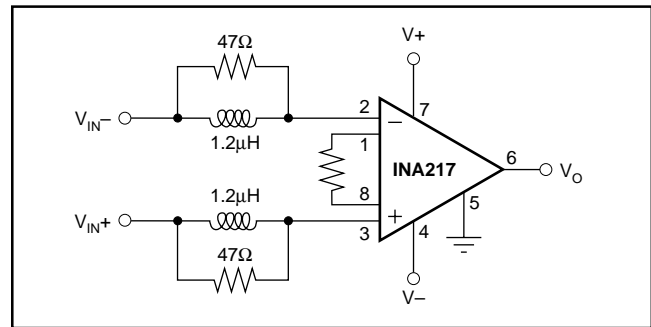


FIGURE 2. Input Stabilization Network.

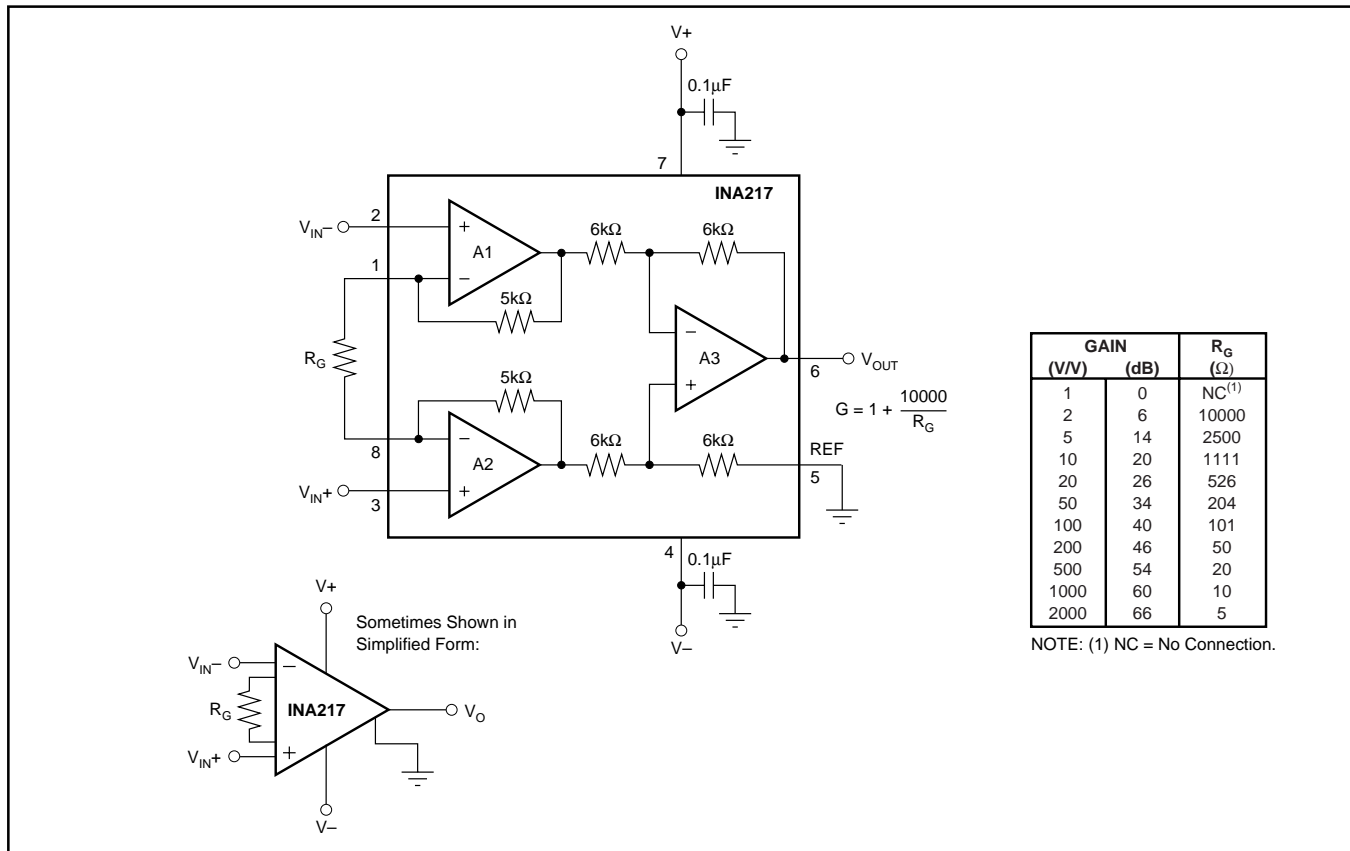


FIGURE 1. Basic Circuit Connections.

## OFFSET VOLTAGE TRIM

A variable voltage applied to pin 5, as shown in Figure 3, can be used to adjust the output offset voltage. A voltage applied to pin 5 is summed with the output signal. An op amp connected as a buffer is used to provide a low impedance at pin 5 to assure good common-mode rejection.

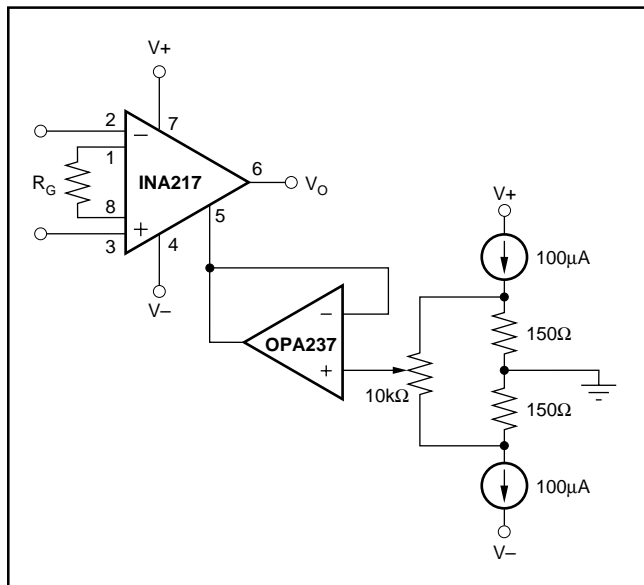


FIGURE 3. Offset Voltage Adjustment Circuit.

## MICROPHONE AMPLIFIER

Figure 4 shows a typical circuit for a professional microphone input amplifier.  $R_1$  and  $R_2$  provide a current path for conventional 48V phantom power source for a remotely located microphone. An optional switch allows phantom power to be disabled.  $C_1$  and  $C_2$  block the phantom power voltage from the INA217 input circuitry. Non-polarized capacitors should be used for  $C_1$  and  $C_2$  if phantom power is to be disabled. For additional input protection against ESD and hot-plugging, four IN4148 diodes may be connected from the input to supply lines.

$R_4$  and  $R_5$  provide a path for input bias current of the INA217. Input offset current (typically 100nA) creates a DC differential input voltage that will produce an output offset voltage. This is generally the dominant source of output offset voltage in this application. With a maximum gain of 1000 (60dB), the output offset voltage can be several volts. This may be entirely acceptable if the output is AC-coupled into the subsequent stage. An alternate technique is shown in Figure 4. An inexpensive FET-input op amp in a feedback loop drives the DC output voltage to 0V. A2 is not in the audio signal path and does not affect signal quality.

Gain is set with a variable resistor,  $R_7$ , in series with  $R_6$ .  $R_6$  determines the maximum gain. The total resistance,  $R_6 + R_7$ , determines the lowest gain. A special reverse-log taper potentiometer for  $R_7$  can be used to create a linear change (in dB) with rotation.

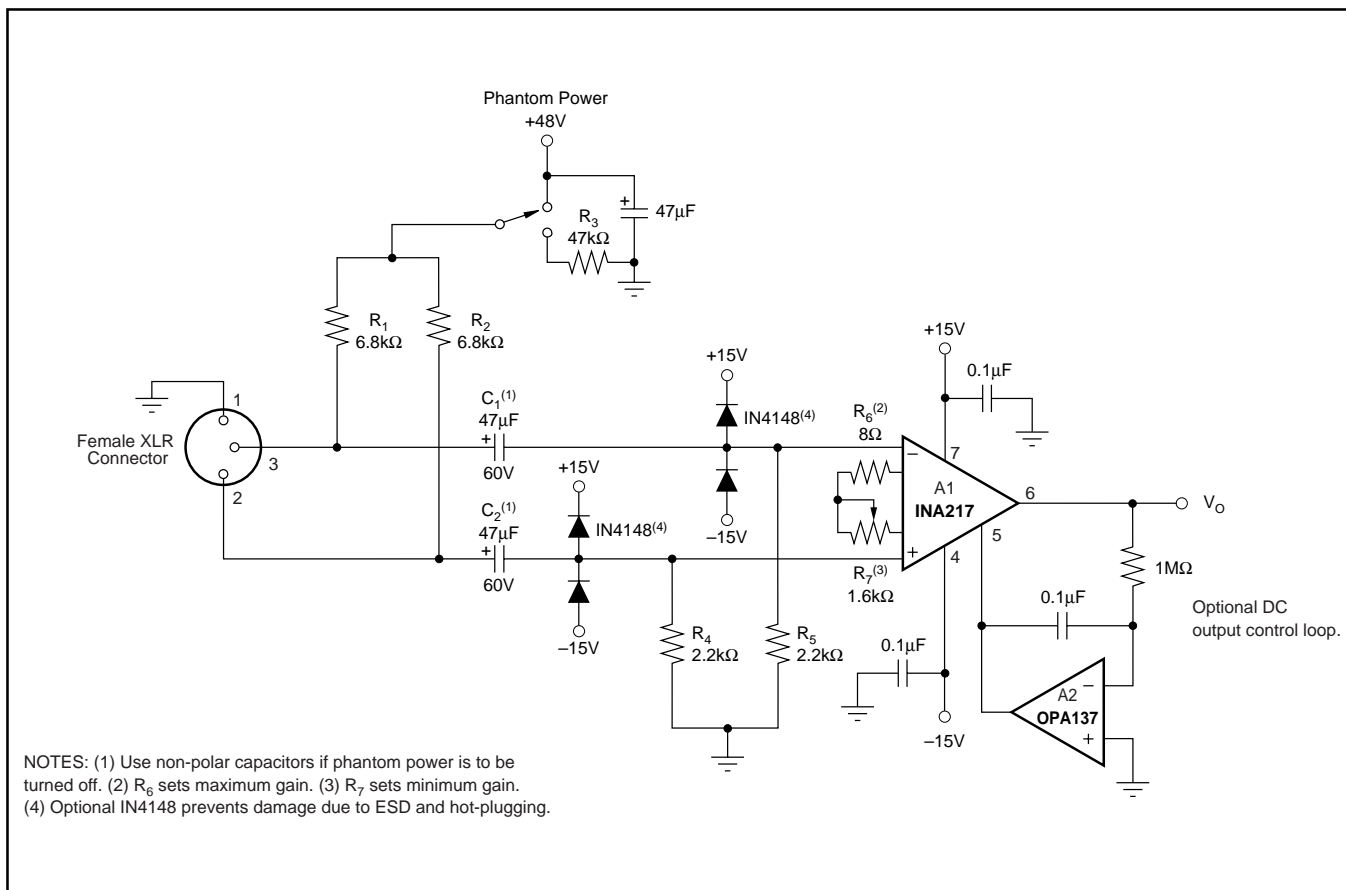


FIGURE 4. Phantom-Powered Microphone Preamplifier.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA217AIDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA217	<a href="#">Samples</a>
INA217AIDWT	ACTIVE	SOIC	DW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA217	<a href="#">Samples</a>
INA217AIDWTE4	ACTIVE	SOIC	DW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA217	<a href="#">Samples</a>
INA217AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	INA217	<a href="#">Samples</a>
INA217AIPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	INA217	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

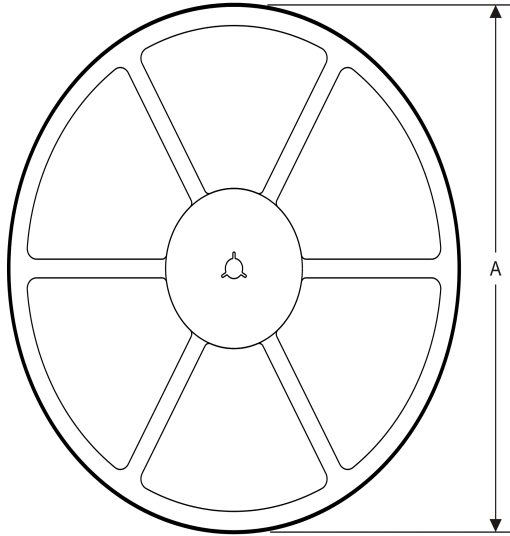
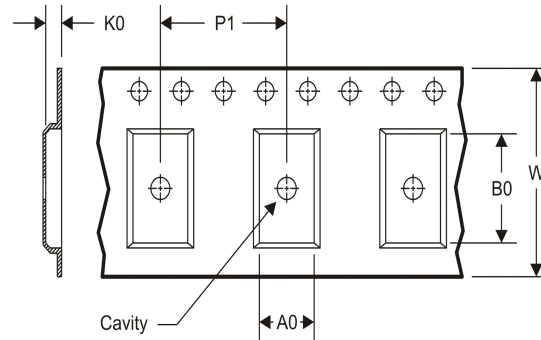
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA217AIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
INA217AIDWT	SOIC	DW	16	250	180.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA217AIDWR	SOIC	DW	16	2000	367.0	367.0	38.0
INA217AIDWT	SOIC	DW	16	250	184.0	184.0	50.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

DW (R-PDSO-G16)

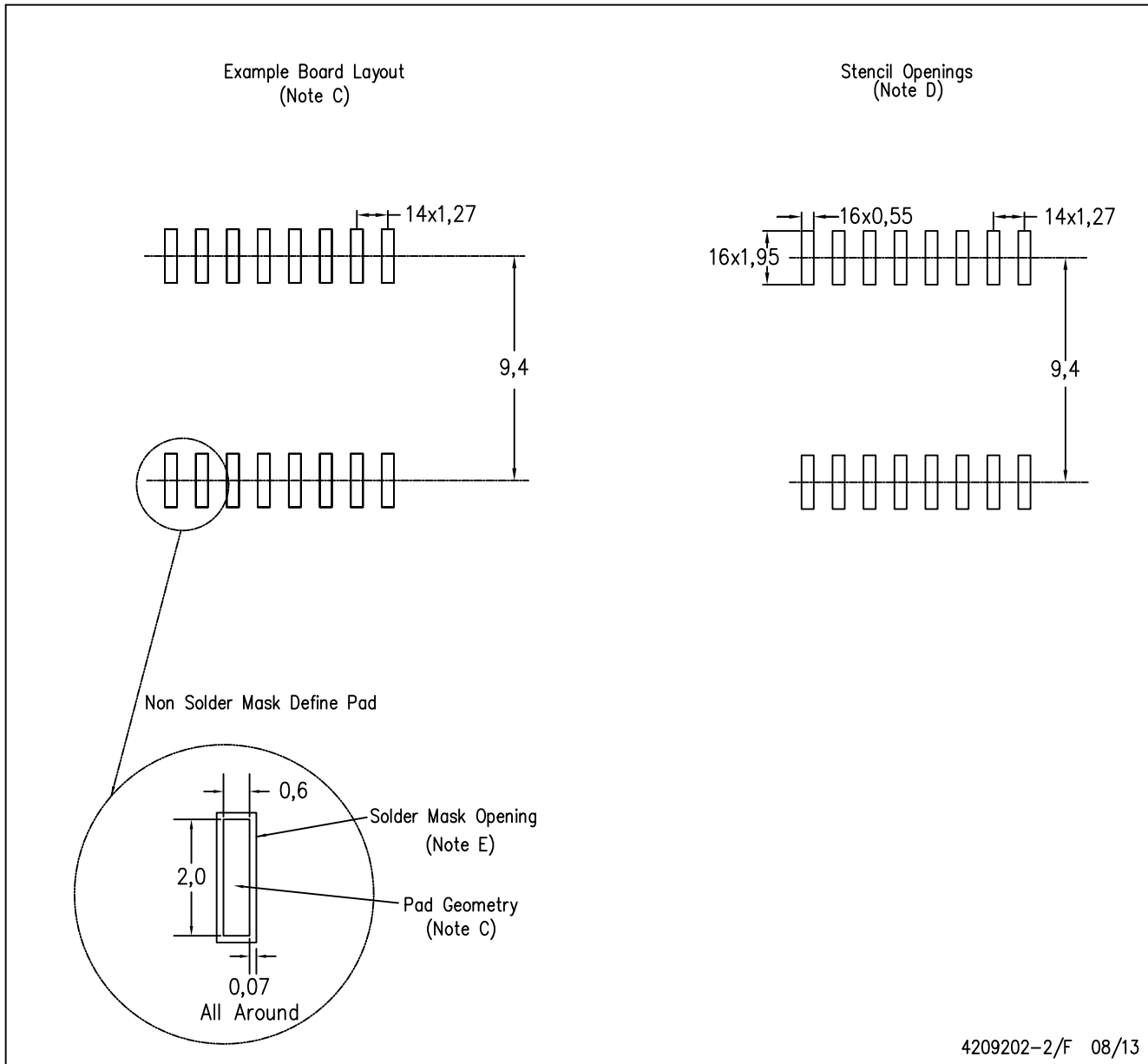
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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