

## DS26C31T/DS26C31M CMOS Quad TRI-STATE® Differential Line Driver

 Check for Samples: [DS26C31M](#), [DS26C31T](#)

### FEATURES

- TTL Input Compatible
- Typical Propagation Delays: 6 ns
- Typical Output Skew: 0.5 ns
- Outputs Will Not Load Line when  $V_{CC} = 0V$
- DS26C31T Meets the Requirements of EIA Standard RS-422
- Operation from Single 5V Supply
- TRI-STATE Outputs for Connection to System Buses
- Low Quiescent Current
- Available in Surface Mount
- Mil-Std-883C Compliant

### DESCRIPTION

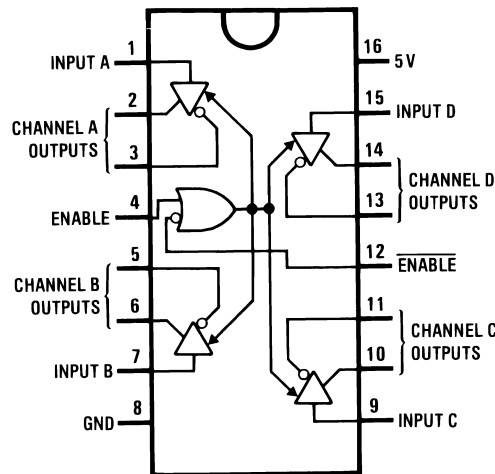
The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken <sup>(1)</sup>. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to  $V_{CC}$  and ground.

(1) The DS26C31M ( $-55^{\circ}C$  to  $+125^{\circ}C$ ) is tested with  $V_{OUT}$  between +6V and 0V while RS-422A condition is +6V and -0.25V.

### Connection Diagrams



**Figure 1. Dual-In-Line Package, Top View**  
 See Package Number D0016A or NFG0016E  
 For Complete Military Product Specifications,  
 refer to the appropriate SMD or MDS.  
 See Package Number NAJ0020A, NFE0016A or NAD0016A



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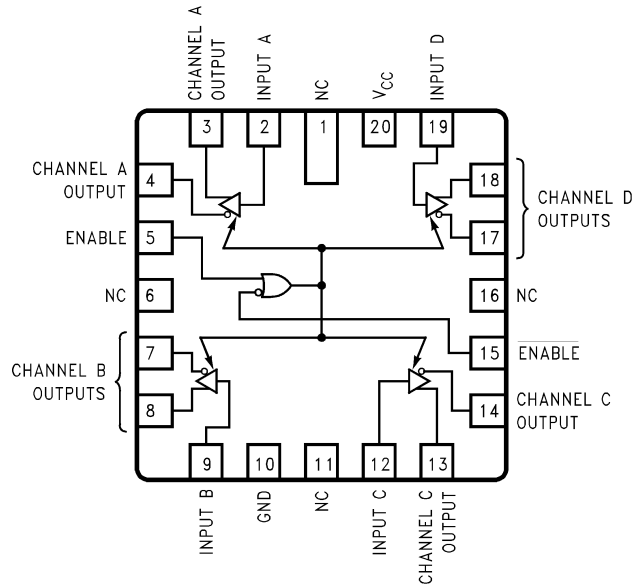


Figure 2. 20-Lead Ceramic Leadless Chip Carrier (NAJ)

Truth Table<sup>(1)</sup>

ENABLE	ENABLE	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

(1) L = Low logic state  
 X = Irrelevant  
 H = High logic state  
 Z = TRI-STATE (high impedance)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

Supply Voltage ( $V_{CC}$ )		-0.5V to 7.0V
DC Input Voltage ( $V_{IN}$ )		-1.5V to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )		-0.5V to 7V
Clamp Diode Current ( $I_{IK}, I_{OK}$ )		$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )		$\pm 150$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )		
Storage Temperature Range ( $T_{STG}$ )		-65°C to +150°C
Max. Power Dissipation ( $P_D$ ) @25°C <sup>(4)</sup>	Ceramic "NFE" Pkg.	2419 mW
	Plastic "NFG" Pkg.	1736 mW
	SOIC "D" Pkg.	1226 mW
	Ceramic "NAD" Pkg.	1182 mW
	Ceramic "NAJ" Pkg.	2134 mW
Lead Temperature ( $T_L$ )	(Soldering, 4 sec.)	260°C
This device does not meet 2000V ESD Rating. <sup>(5)</sup>		

- (1) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.
- (2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) Ratings apply to ambient temperature at 25°C. Above this temperature derate NFG package at 13.89 mW/°C, NFE package 16.13 mW/°C, D package 9.80 mW/°C, NAJ package 12.20 mW/°C, and NAD package 6.75 mW/°C.
- (5) ESD Rating: HBM (1.5 k $\Omega$ , 100 pF); Inputs  $\geq 1500V$ ; Outputs  $\geq 1000V$ ; EIAJ (0 $\Omega$ , 200 pF)  $\geq 350V$

### Operating Conditions

		Min	Max	Units
Supply Voltage ( $V_{CC}$ )		4.50	5.50	V
DC Input or Output Voltage	( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	DS26C31T	-40	+85	°C
	DS26C31M	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			500	ns

### DC Electrical Characteristics

V<sub>CC</sub> = 5V ± 10% (unless otherwise specified)<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Units		
V <sub>IH</sub>	High Level Input Voltage		2.0			V		
V <sub>IL</sub>	Low Level Input Voltage				0.8	V		
V <sub>OH</sub>	High Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = -20 mA	2.5	3.4		V		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = 20 mA		0.3	0.5	V		
V <sub>T</sub>	Differential Output Voltage	R <sub>L</sub> = 100Ω See <sup>(2)</sup>	2.0	3.1		V		
V <sub>T</sub> - $\overline{V_T}$	Difference In Differential Output	R <sub>L</sub> = 100Ω See <sup>(2)</sup>			0.4	V		
V <sub>OS</sub>	Common Mode Output Voltage	R <sub>L</sub> = 100Ω See <sup>(2)</sup>		1.8	3.0	V		
V <sub>OS</sub> - $\overline{V_{OS}}$	Difference In Common Mode Output	R <sub>L</sub> = 100Ω See <sup>(2)</sup>			0.4	V		
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = V <sub>CC</sub> , GND, V <sub>IH</sub> , or V <sub>IL</sub>			±1.0	μA		
I <sub>CC</sub>	Quiescent Supply Current <sup>(3)</sup>	DS26C31T I <sub>OUT</sub> = 0 μA	V <sub>IN</sub> = V <sub>CC</sub> or GND		200	500	μA	
			V <sub>IN</sub> = 2.4V or 0.5V <sup>(3)</sup>		0.8	2.0	mA	
		DS26C31M I <sub>OUT</sub> = 0 μA	V <sub>IN</sub> = V <sub>CC</sub> or GND		200	500	μA	
			V <sub>IN</sub> = 2.4V or 0.5V <sup>(3)</sup>		0.8	2.1	mA	
I <sub>OZ</sub>	TRI-STATE Output Leakage Current	V <sub>OUT</sub> = V <sub>CC</sub> or GND ENABLE = V <sub>IL</sub> $\overline{\text{ENABLE}}$ = V <sub>IH</sub>		±0.5	±5.0	μA		
I <sub>SC</sub>	Output Short Circuit Current	V <sub>IN</sub> = V <sub>CC</sub> or GND <sup>(2)(4)</sup>	-30		-150	mA		
I <sub>OFF</sub>	Output Leakage Current Power Off <sup>(2)</sup>	DS26C31T V <sub>CC</sub> = 0V	V <sub>OUT</sub> = 6V			100	μA	
			V <sub>OUT</sub> = -0.25V			-100	μA	
		DS26C31M V <sub>CC</sub> = 0V	V <sub>OUT</sub> = 6V				100	μA
			V <sub>OUT</sub> = 0V <sup>(5)</sup>				-100	μA

- (1) Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.
- (2) See EIA Specification RS-422 for exact test conditions.
- (3) Measured per input. All other inputs at V<sub>CC</sub> or GND.
- (4) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.
- (5) The DS26C31M (-55°C to +125°C) is tested with V<sub>OUT</sub> between +6V and 0V while RS-422A condition is +6V and -0.25V.

### Switching Characteristics

V<sub>CC</sub> = 5V ±10%, t<sub>r</sub> ≤ 6 ns, t<sub>f</sub> ≤ 6 ns (Figure 3, Figure 4, Figure 5, Figure 6)<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delays Input to Output	S1 Open	2	6	11	14	ns
Skew	<sup>(2)</sup>	S1 Open		0.5	2.0	3.0	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Differential Output Rise And Fall Times	S1 Open		6	10	14	ns
t <sub>PZH</sub>	Output Enable Time	S1 Closed		11	19	22	ns
t <sub>PZL</sub>	Output Enable Time	S1 Closed		13	21	28	ns

- (1) Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.
- (2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

### Switching Characteristics (continued)

 $V_{CC} = 5V \pm 10\%$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$  (Figure 3, Figure 4, Figure 5, Figure 6)<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
$t_{PHZ}$	Output Disable Time <sup>(3)</sup>	S1 Closed		5	9	12	ns
$t_{PLZ}$	Output Disable Time <sup>(3)</sup>	S1 Closed		7	11	14	ns
$C_{PD}$	Power Dissipation Capacitance <sup>(4)</sup>			50			pF
$C_{IN}$	Input Capacitance			6			pF

(3) Output disable time is the delay from ENABLE or  $\overline{\text{ENABLE}}$  being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

(4)  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

### Comparison Table of Switching Characteristics into “LS-Type” Load

 $V_{CC} = 5V$ ,  $T_A = 25^\circ\text{C}$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$  (Figure 4, Figure 6, Figure 7, Figure 8)<sup>(1)</sup>

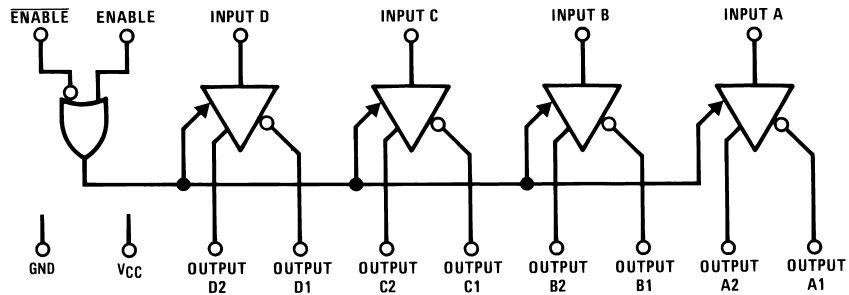
Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
$t_{PLH}, t_{PHL}$	Propagation Delays Input to Output	$C_L = 30 \text{ pF}$ S1 Closed S2 Closed	6	8	10	15	ns
Skew	See <sup>(2)</sup>	$C_L = 30 \text{ pF}$ S1 Closed S2 Closed	0.5	1.0	2.0	6.0	ns
$t_{THL}, t_{TLH}$	Differential Output Rise and Fall Times	$C_L = 30 \text{ pF}$ S1 Closed S2 Closed	4	6			ns
$t_{PLZ}$	Output Disable Time <sup>(3)</sup>	$C_L = 10 \text{ pF}$ S1 Closed S2 Open	6	9	15	35	ns
$t_{PHZ}$	Output Disable Time <sup>(3)</sup>	$C_L = 10 \text{ pF}$ S1 Open S2 Closed	4	7	15	25	ns
$t_{PZL}$	Output Enable Time	$C_L = 30 \text{ pF}$ S1 Closed S2 Open	14	20	20	30	ns
$t_{PZH}$	Output Enable Time	$C_L = 30 \text{ pF}$ S1 Open S2 Closed	11	17	20	30	ns

(1) This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or verified.

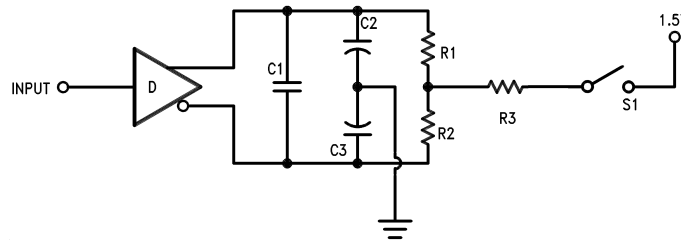
(2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

(3) Output disable time is the delay from ENABLE or  $\overline{\text{ENABLE}}$  being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Logic Diagram



AC Test Circuit and Switching Time Waveforms



Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

Figure 3. AC Test Circuit

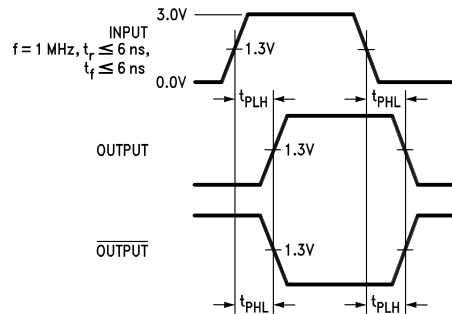


Figure 4. Propagation Delays

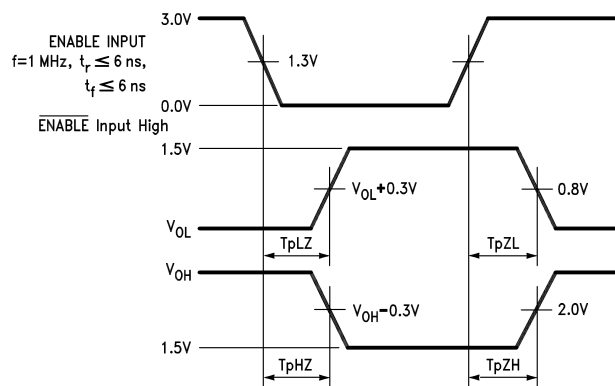
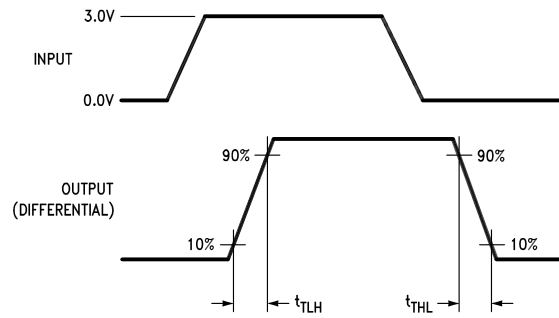


Figure 5. Enable and Disable Times



Input pulse;  $f = 1 \text{ MHz}$ , 50%;  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$

Figure 6. Differential Rise and Fall Times

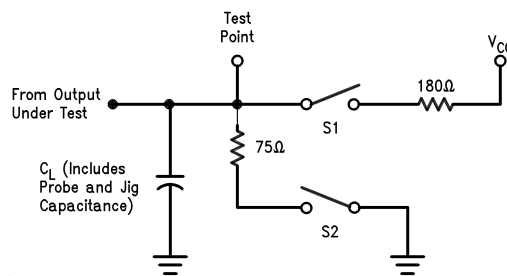


Figure 7. Load AC Test Circuit for “LS-Type” Load

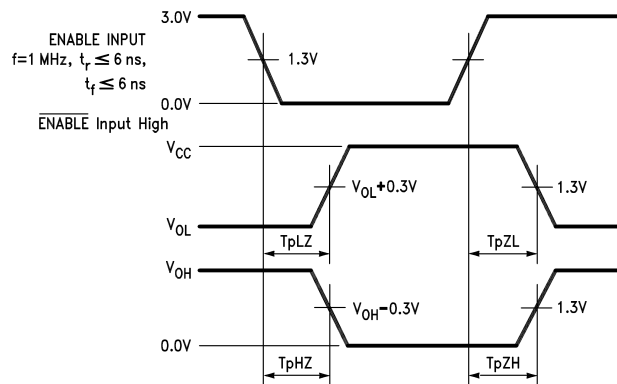
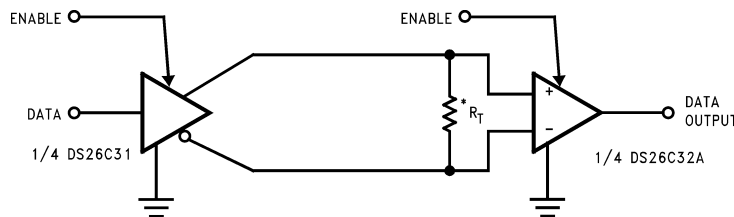


Figure 8. Enable and Disable Times for “LS-Type” Load

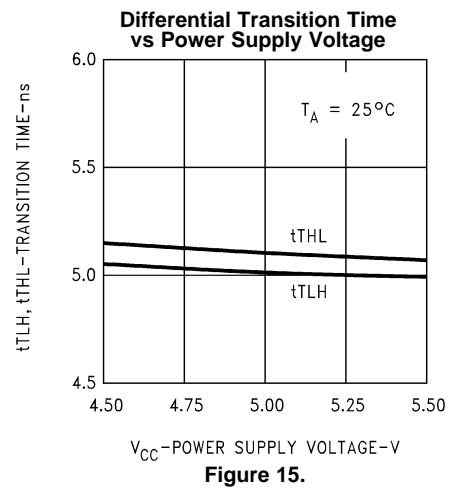
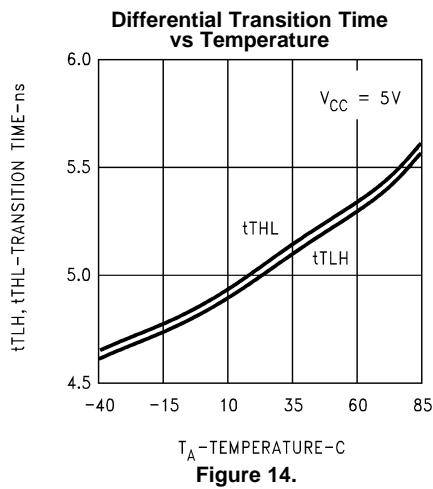
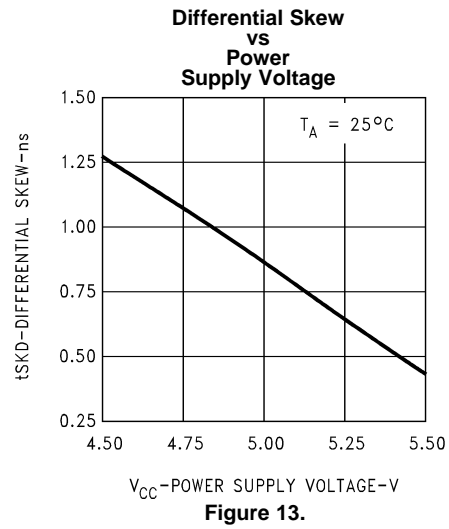
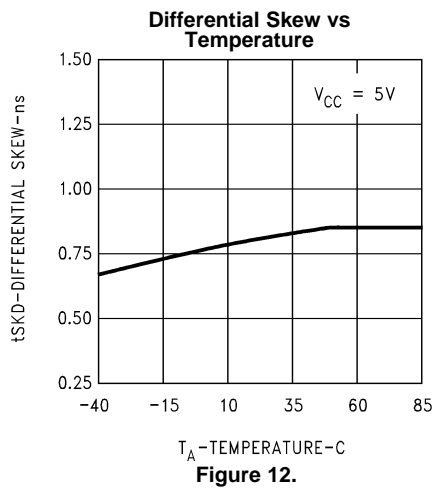
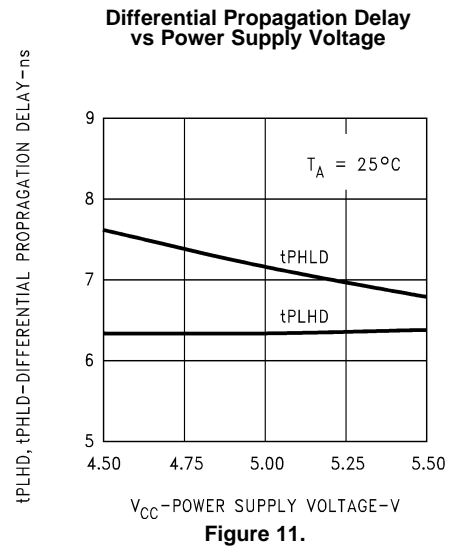
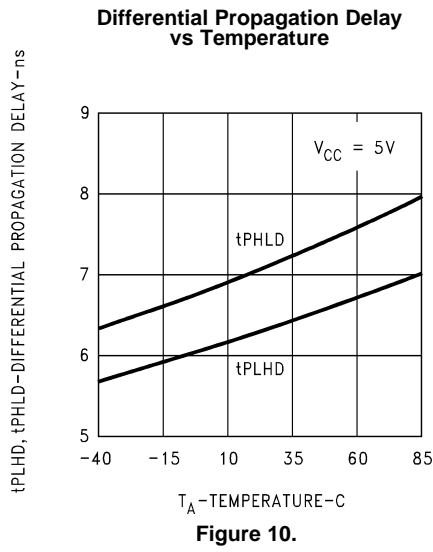
Typical Applications



\* $R_T$  is optional although highly recommended to reduce reflection.

Figure 9. Two-Wire Balanced System, RS-422

### Typical Performance Characteristics





Typical Performance Characteristics (continued)

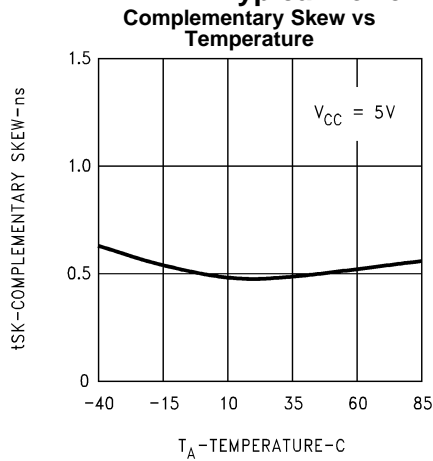


Figure 16.

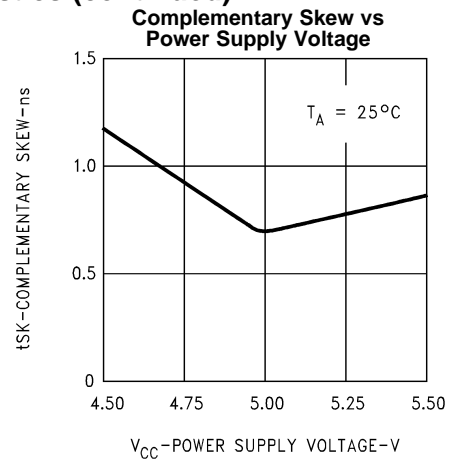


Figure 17.

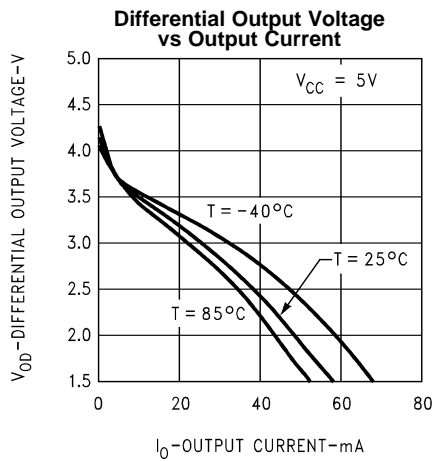


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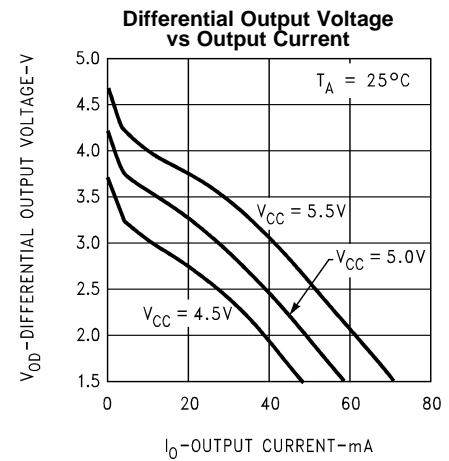


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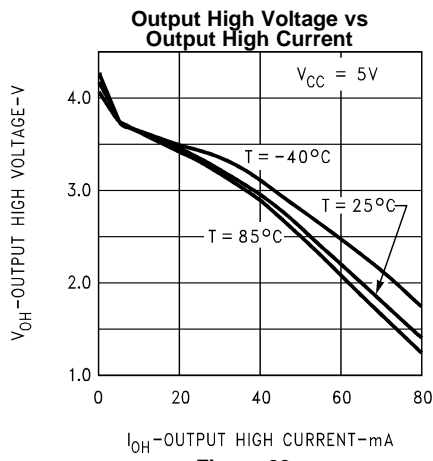


Figure 20.

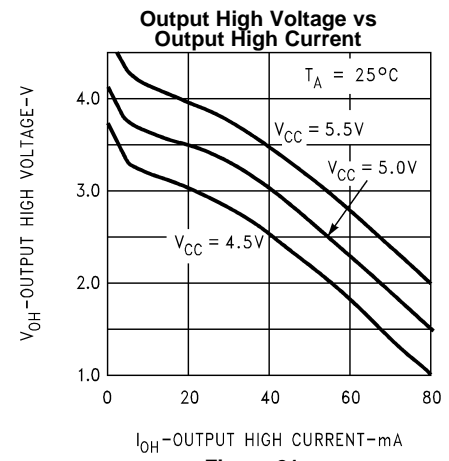
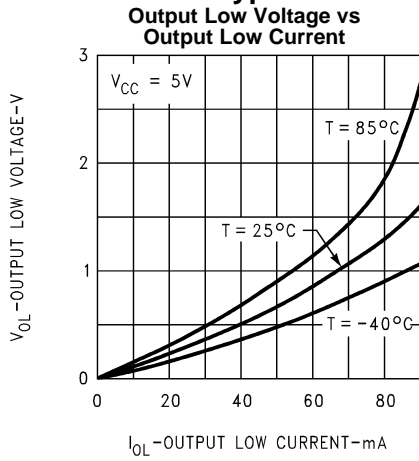
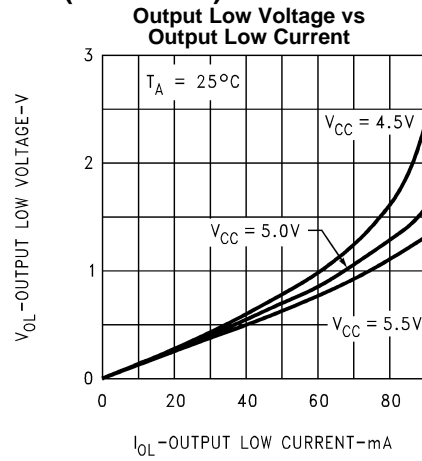


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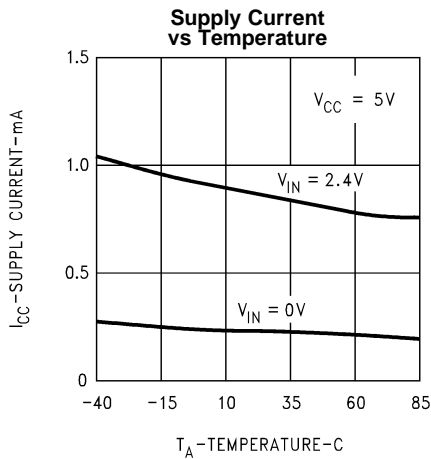
**Typical Performance Characteristics (continued)**



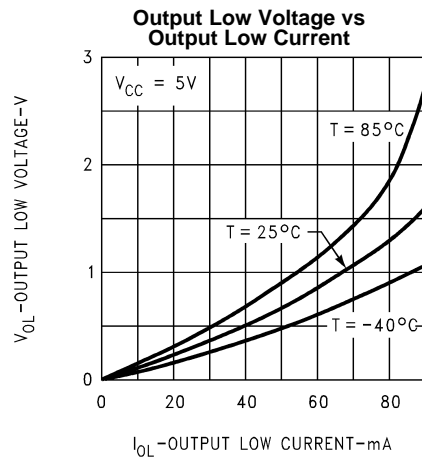
**Figure 22.**



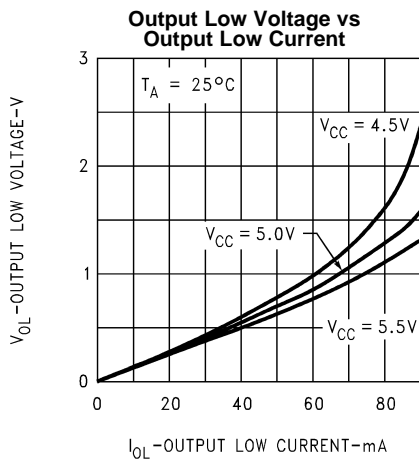
**Figure 23.**



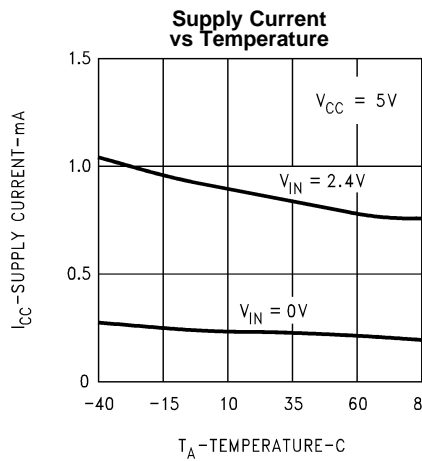
**Figure 24.**



**Figure 25.**



**Figure 26.**



**Figure 27.**

Typical Performance Characteristics (continued)

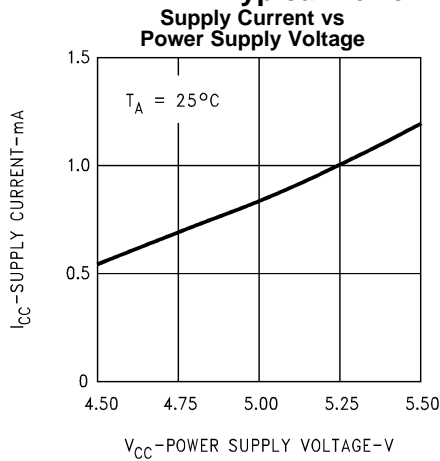


Figure 28.

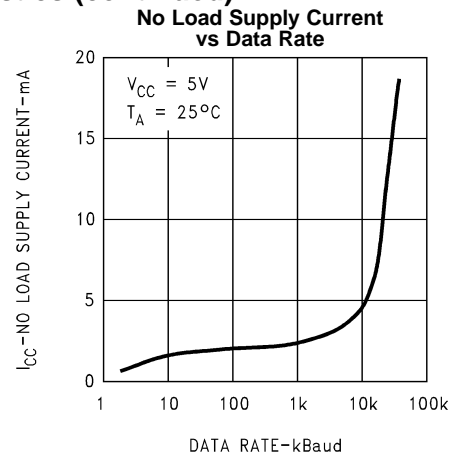


Figure 29.

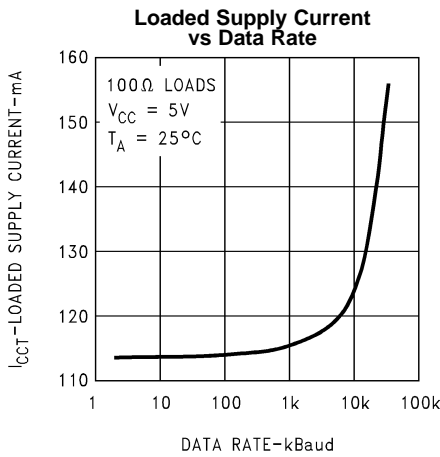


Figure 30.

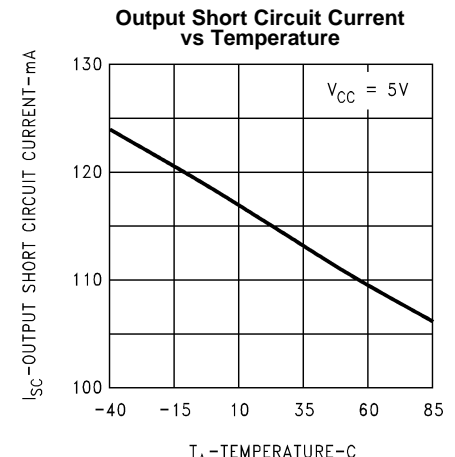


Figure 31.

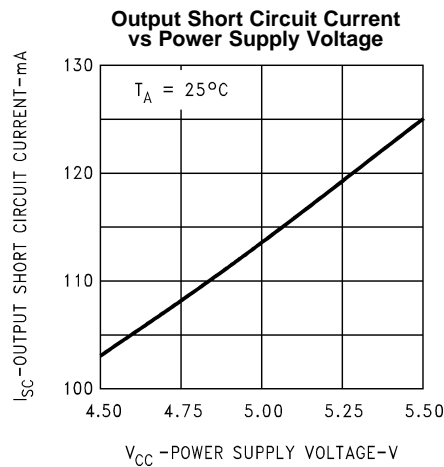


Figure 32.

## REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format .....	11

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26C31TM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS26C31TM	
DS26C31TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	SN   CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C31TM	<b>Samples</b>
DS26C31TMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS26C31TM	
DS26C31TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C31TM	<b>Samples</b>
DS26C31TN	NRND	PDIP	NFG	16	25	TBD	Call TI	Call TI	-40 to 85	DS26C31TN	
DS26C31TN/NOPB	ACTIVE	PDIP	NFG	16	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	DS26C31TN	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26C31TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

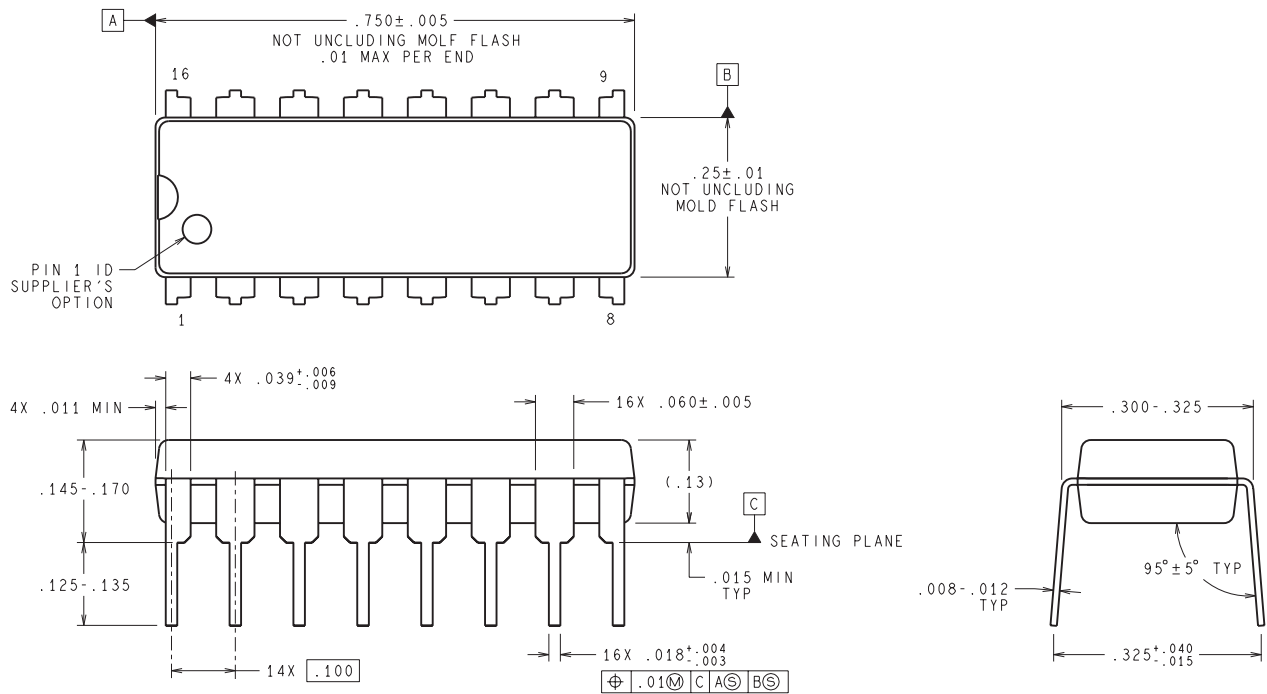


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26C31TMX	SOIC	D	16	2500	367.0	367.0	35.0



NFG0016E



DIMENSIONS ARE IN INCHES  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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