

FEATURES

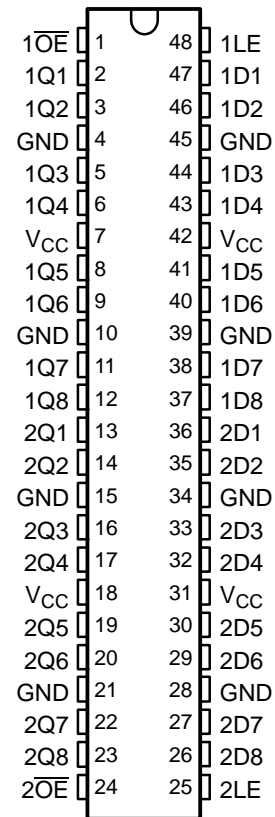
- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.2 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 16-bit transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16373A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|-----------------------|-----------------------|-------------------|
| -40°C to 85°C | FBGA – GRD | Tape and reel | SN74LVC16373AGRDR | LD373A |
| | FBGA – ZRD (Pb-free) | | SN74LVC16373AZRDR | |
| | SSOP – DL | Tube | SN74LVC16373ADL | LVC16373A |
| | | Tape and reel | SN74LVC16373ADLR | |
| | TSSOP – DGG | Tape and reel | SN74LVC16373ADGGR | LVC16373A |
| | | | 74LVC16373ADGGRG4 | |
| | TVSOP – DGV | Tape and reel | SN74LVC16373ADGVR | LD373A |
| | | | 74LVC16373ADGVRE4 | |
| VFBGA – GQL | Tape and reel | SN74LVC16373AGQLR | LD373A | |
| | | VFBGA – ZQL (Pb-free) | | SN74LVC16373AZQLR |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74LVC16373A
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCAS755A–DECEMBER 2003–REVISED SEPTEMBER 2005

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

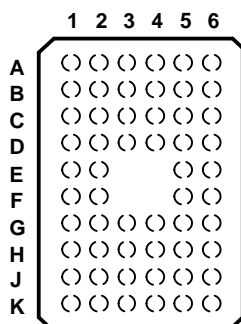
\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

GQL OR ZQL PACKAGE
(TOP VIEW)

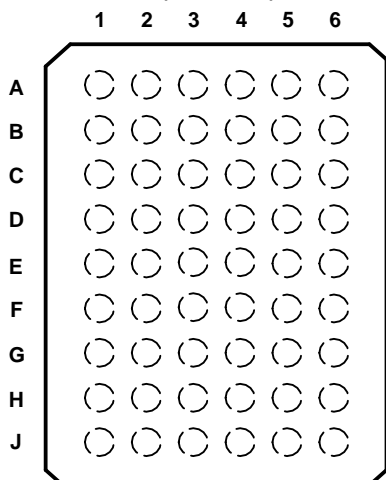


TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-------------------|-----|----------|----------|-----|-----|
| A | 1 \overline{OE} | NC | NC | NC | NC | 1LE |
| B | 1Q2 | 1Q1 | GND | GND | 1D1 | 1D2 |
| C | 1Q4 | 1Q3 | V_{CC} | V_{CC} | 1D3 | 1D4 |
| D | 1Q6 | 1Q5 | GND | GND | 1D5 | 1D6 |
| E | 1Q8 | 1Q7 | | | 1D7 | 1D8 |
| F | 2Q1 | 2Q2 | | | 2D2 | 2D1 |
| G | 2Q3 | 2Q4 | GND | GND | 2D4 | 2D3 |
| H | 2Q5 | 2Q6 | V_{CC} | V_{CC} | 2D6 | 2D5 |
| J | 2Q7 | 2Q8 | GND | GND | 2D8 | 2D7 |
| K | 2 \overline{OE} | NC | NC | NC | NC | 2LE |

(1) NC – No internal connection

GRD OR ZRD PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)

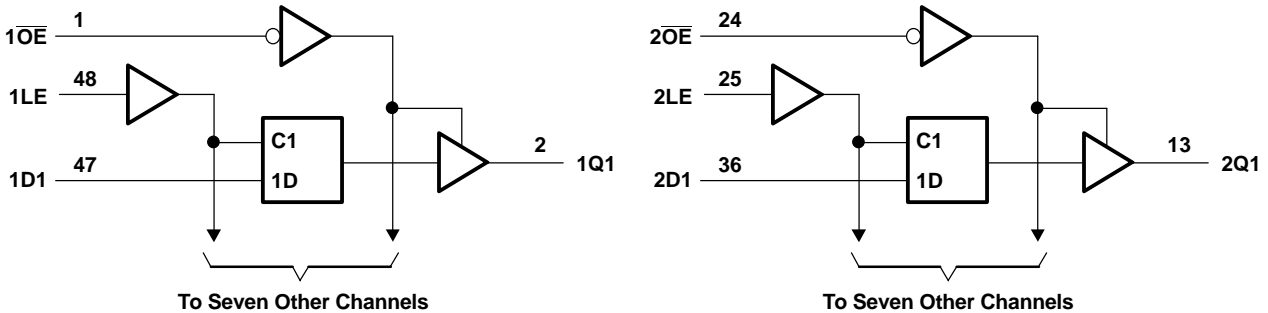
| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|-------------------|----------|-----|-----|
| A | 1Q1 | NC | 1 \overline{OE} | 1LE | NC | 1D1 |
| B | 1Q3 | 1Q2 | NC | NC | 1D2 | 1D3 |
| C | 1Q5 | 1Q4 | V_{CC} | V_{CC} | 1D4 | 1D5 |
| D | 1Q7 | 1Q6 | GND | GND | 1D6 | 1D7 |
| E | 2Q1 | 1Q8 | GND | GND | 1D8 | 2D1 |
| F | 2Q3 | 2Q2 | GND | GND | 2D2 | 2D3 |
| G | 2Q5 | 2Q4 | V_{CC} | V_{CC} | 2D4 | 2D5 |
| H | 2Q7 | 2Q6 | NC | NC | 2D6 | 2D7 |
| J | 2Q8 | NC | 2 \overline{OE} | 2LE | NC | 2D8 |

(1) NC – No internal connection

FUNCTION TABLE

| INPUTS | | | OUTPUT Q |
|--------|----|---|----------------|
| OE | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q ₀ |
| H | X | X | Z |

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DGV, and DL packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|-----------------|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | | -50 | mA |
| I _{OK} | Output clamp current | | -50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through each V _{CC} or GND | | ±100 | mA |
| θ _{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | | 70 |
| | | DGV package | | 58 |
| | | DL package | | 63 |
| | | GQL/ZQL package | | 42 |
| | | GRD/ZRD package | | 36 |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74LVC16373A
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

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Recommended Operating Conditions⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|------------------------------------|------------------------|-----------------|----|
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | High or low state | 0 | V _{CC} | V |
| | | High-impedance state | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | mA |
| | | V _{CC} = 2.3 V | | –8 | |
| | | V _{CC} = 2.7 V | | –12 | |
| | | V _{CC} = 3 V | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 2.7 V | | 12 | |
| | | V _{CC} = 3 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | 10 | ns/V | |
| T _A | Operating free-air temperature | –40 | 85 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------|--|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} - 0.2 | | | V |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -8 mA | 2.3 V | 1.7 | | | |
| | I _{OH} = -12 mA | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| I _{OH} = -24 mA | 3 V | 2.2 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.7 | |
| | I _{OL} = 12 mA | 2.7 V | | | 0.4 | |
| | I _{OL} = 24 mA | 3 V | | | 0.55 | |
| I _I | V _I = 0 to 5.5 V | 3.6 V | | | ±5 | μA |
| I _{off} | V _I or V _O = 5.5 V | 0 | | | ±10 | μA |
| I _{OZ} | V _O = 0 to 5.5 V | 3.6 V | | | ±10 | μA |
| I _{CC} | V _I = V _{CC} or GND | 3.6 V | I _O = 0 | | 20 | μA |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾ | | | | 20 | |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | | 5 | pF |
| C _o | V _O = V _{CC} or GND | 3.3 V | | | 6.5 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|-----------------|-----------------------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | 3.3 | | 3.3 | | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, data before LE↓ | 1.6 | | 1.2 | | 1.7 | | 1.7 | | ns |
| t _h | Hold time, data after LE↓ | 1 | | 1.1 | | 1.2 | | 1.2 | | ns |

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|------------------|-----------------|----------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | D | Q | 1.5 | 6.4 | 1 | 4.2 | 1 | 4.9 | 1.6 | 4.2 | ns |
| | LE | | 1.5 | 7.1 | 1 | 4.8 | 1 | 5.3 | 2.1 | 4.6 | |
| t _{en} | \overline{OE} | Q | 1.5 | 6.7 | 1 | 4.7 | 1 | 5.7 | 1.3 | 4.7 | ns |
| t _{dis} | \overline{OE} | Q | 1.5 | 8.4 | 1 | 5 | 1 | 6.3 | 2.5 | 5.9 | ns |

SN74LVC16373A
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

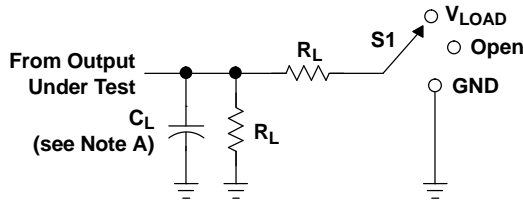
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Operating Characteristics

T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------------|---|------------------|-------------------------|-------------------------|-------------------------|------|
| | | | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per latch | Outputs enabled | 32 | 35 | 39 | pF |
| | | Outputs disabled | 4 | 4 | 6 | |

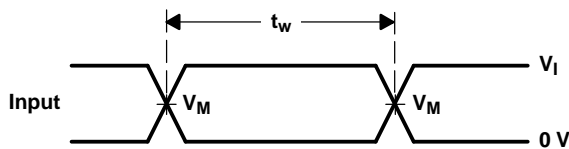
PARAMETER MEASUREMENT INFORMATION



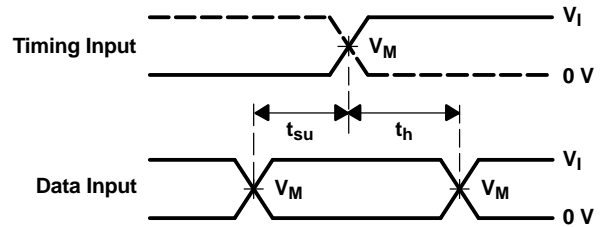
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

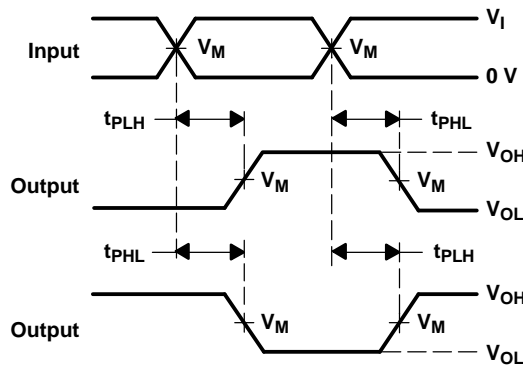
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



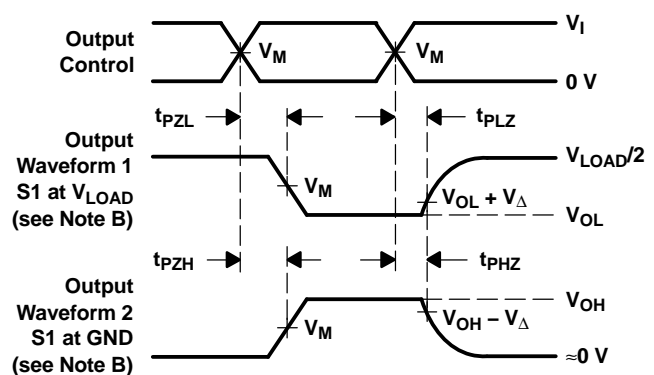
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|----------------------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74LVC16373ADGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC16373A | Samples |
| 74LVC16373ADGVRE4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LD373A | Samples |
| 74LVC16373ADGVRG4 | ACTIVE | TVSOP | DGV | 48 | | TBD | Call TI | Call TI | -40 to 85 | LD373A | Samples |
| SN74LVC16373ADGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC16373A | Samples |
| SN74LVC16373ADGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LD373A | Samples |
| SN74LVC16373ADL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC16373A | Samples |
| SN74LVC16373ADLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC16373A | Samples |
| SN74LVC16373ADLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC16373A | Samples |
| SN74LVC16373ADLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC16373A | Samples |
| SN74LVC16373AGQLR | OBSOLETE | BGA MICROSTAR JUNIOR | GQL | 56 | | TBD | Call TI | Call TI | -40 to 85 | LD373A | |
| SN74LVC16373AZQLR | ACTIVE | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LD373A | Samples |
| SN74LVC16373AZRDR | ACTIVE | BGA MICROSTAR JUNIOR | ZRD | 54 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LD373A | Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC16373A :

- Enhanced Product: [SN74LVC16373A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC16373ADGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVC16373ADGVR | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |
| SN74LVC16373ADLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74LVC16373AZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 330.0 | 16.4 | 4.8 | 7.3 | 1.5 | 8.0 | 16.0 | Q1 |
| SN74LVC16373AZRDR | BGA MICROSTAR JUNIOR | ZRD | 54 | 1000 | 330.0 | 16.4 | 5.8 | 8.3 | 1.55 | 8.0 | 16.0 | Q1 |

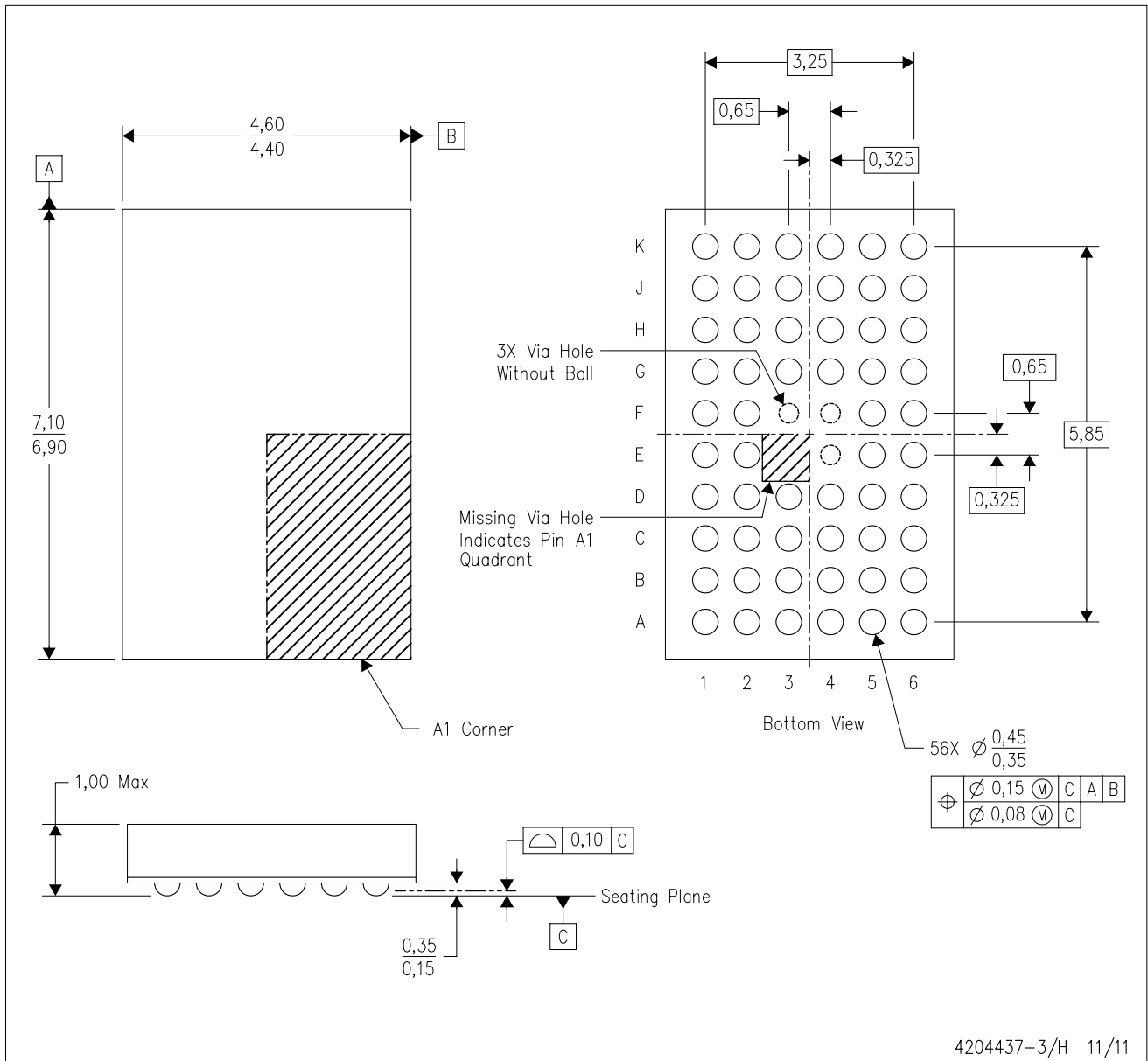
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC16373ADGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC16373ADGVR | TVSOP | DGV | 48 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC16373ADLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |
| SN74LVC16373AZQLR | BGA MICROSTAR JUNIOR | ZQL | 56 | 1000 | 333.2 | 345.9 | 28.6 |
| SN74LVC16373AZRDR | BGA MICROSTAR JUNIOR | ZRD | 54 | 1000 | 333.2 | 345.9 | 28.6 |

ZQL (R-PBGA-N56)

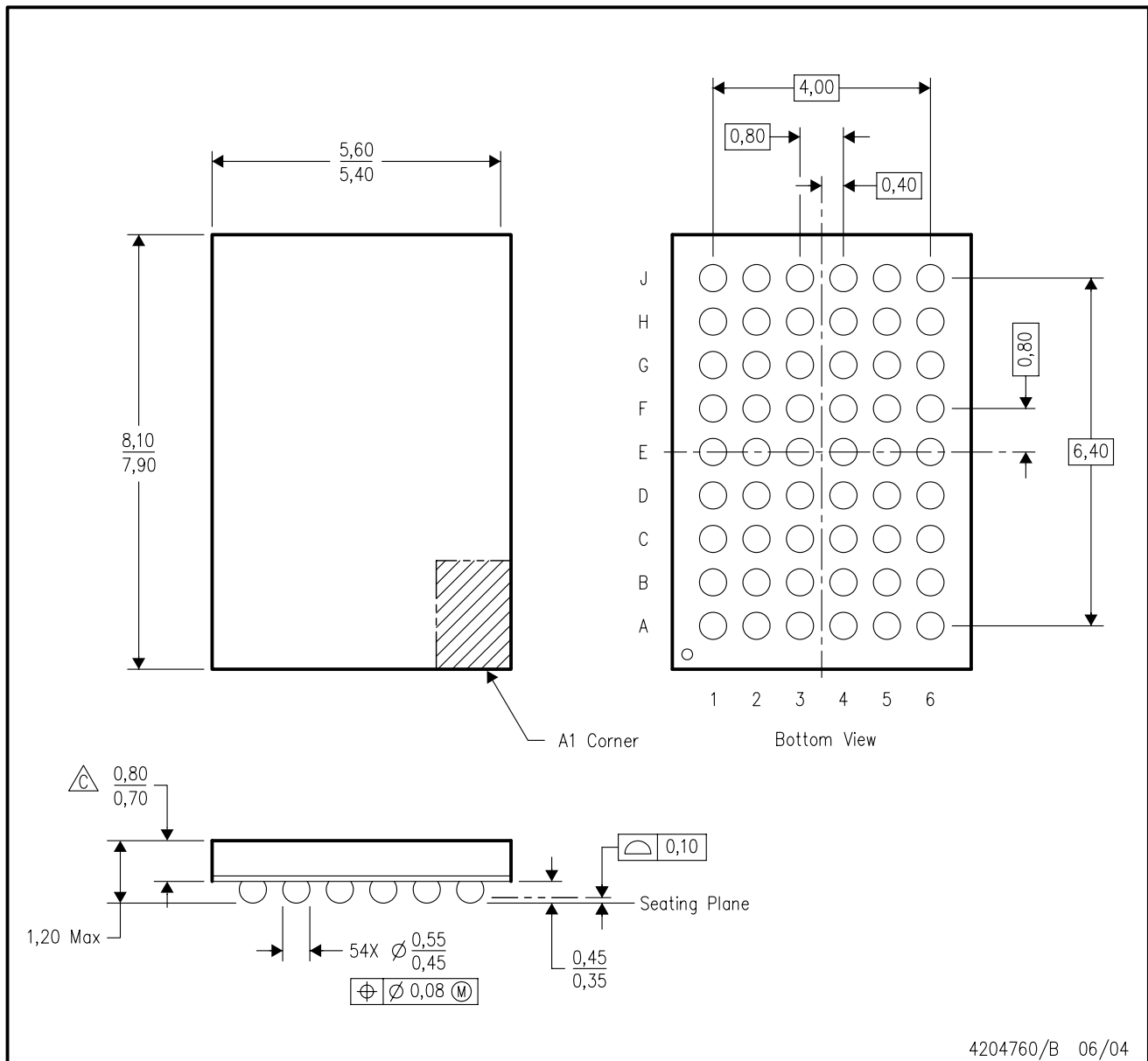
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY

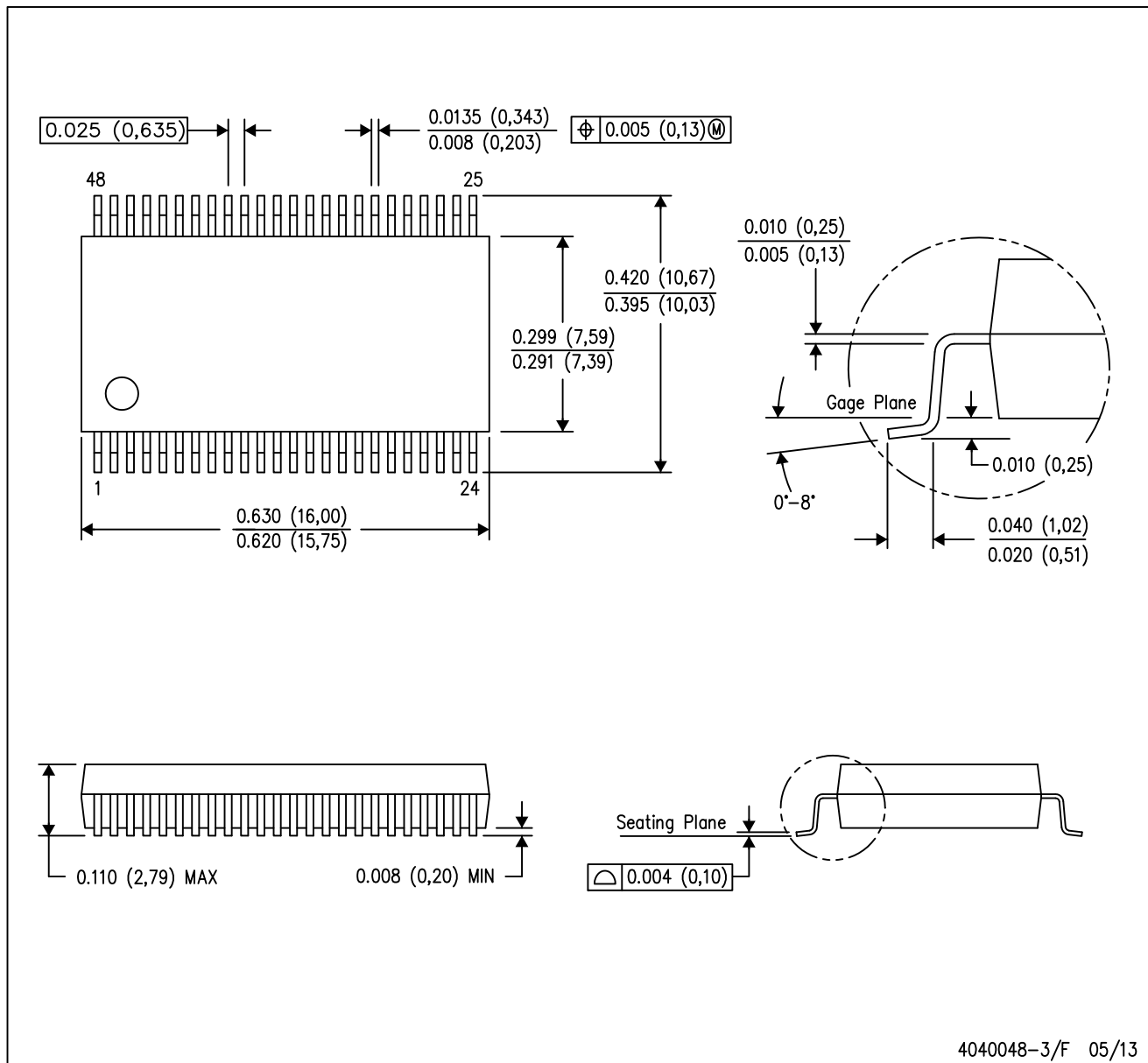


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - \triangle Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

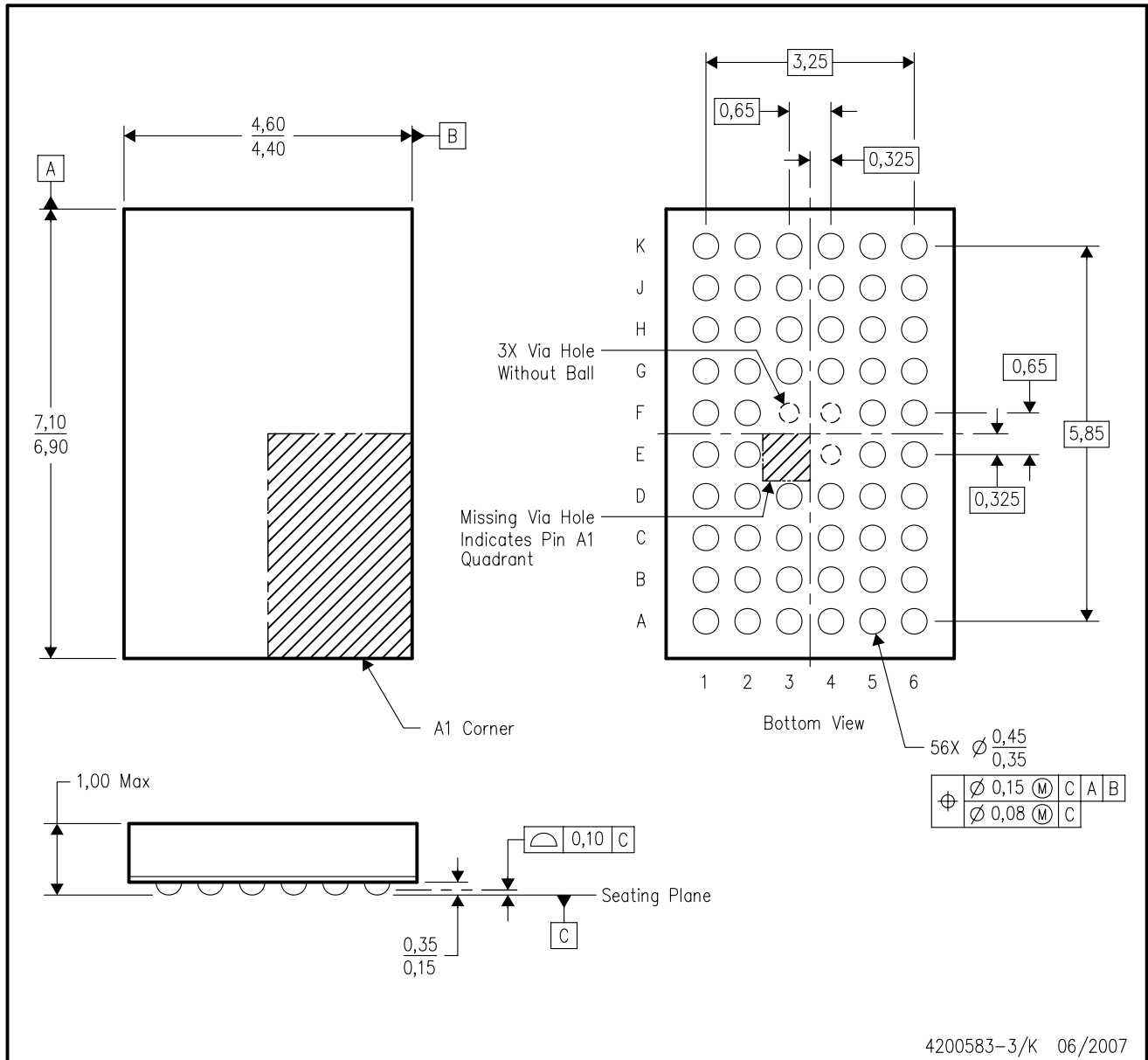


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

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GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

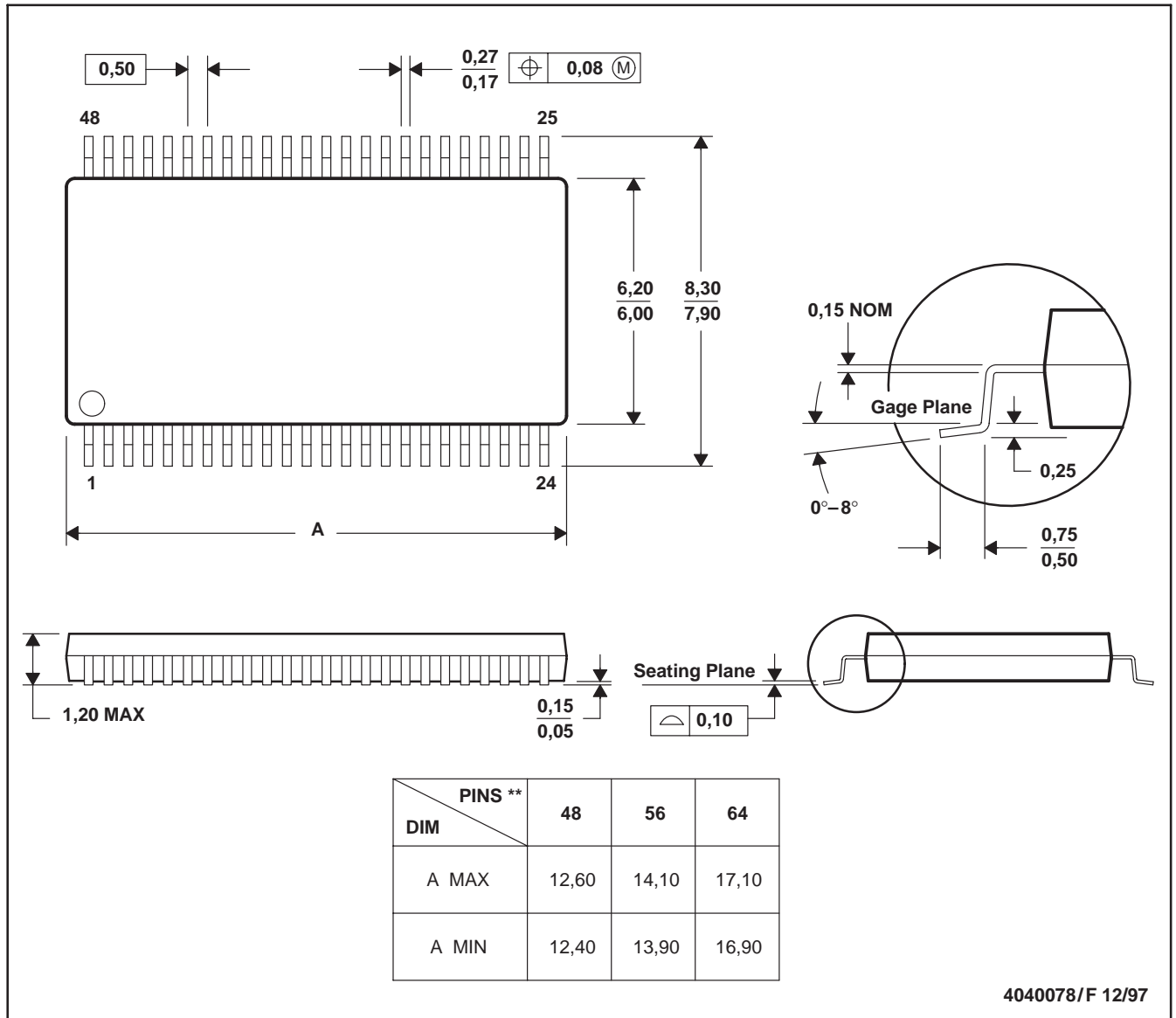


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BA-2.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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