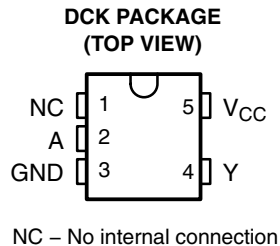


# SN74AHCT1G04-Q1 SINGLE INVERTER GATE

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- Qualified for Automotive Applications
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operating Range of 4.5 V to 5.5 V
- Max  $t_{pd}$  of 7.5 ns at 5 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible



## description/ordering information

The SN74AHCT1G04 contains one gate. The device performs the Boolean function  $Y = \bar{A}$ .

### ORDERING INFORMATION†

| $T_A$          | PACKAGE‡          |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | SOT (SC-70) – DCK | Reel of 3000 | CAHCT1G04QDCKRQ1      | BCS              |

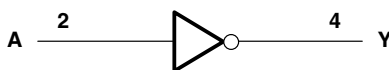
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

### FUNCTION TABLE

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | L           |
| L          | H           |

## logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN74AHCT1G04-Q1

## SINGLE INVERTER GATE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|  |                            |
|--|----------------------------|
| Supply voltage range, $V_{CC}$                                 | -0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                        | -0.5 V to 7 V              |
| Output voltage range, $V_O$ (see Note 1)                       | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                    | -20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) | ±20 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )     | ±25 mA                     |
| Continuous current through $V_{CC}$ or GND                     | ±50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 2)          | 252°C/W                    |
| Storage temperature range, $T_{stg}$                           | -65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

|  | MIN | MAX      | UNIT |
|--|-----|----------|------|
| $V_{CC}$ Supply voltage                                | 4.5 | 5.5      | V    |
| $V_{IH}$ High-level input voltage                      | 2   |          | V    |
| $V_{IL}$ Low-level input voltage                       |     | 0.8      | V    |
| $V_I$ Input voltage                                    | 0   | 5.5      | V    |
| $V_O$ Output voltage                                   | 0   | $V_{CC}$ | V    |
| $I_{OH}$ High-level output current                     |     | -8       | mA   |
| $I_{OL}$ Low-level output current                      |     | 8        | mA   |
| $\Delta t/\Delta v$ Input transition rise or fall rate |     | 20       | ns/V |
| $T_A$ Operating free-air temperature                   | -40 | 125      | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS                                     | $V_{CC}$     | $T_A = 25^\circ\text{C}$ |     |      | MIN | MAX  | UNIT |
|--------------------------|---|--------------|--------------------------|-----|------|-----|------|------|
|                          |   |              | MIN                      | TYP | MAX  |     |      |      |
| $V_{OH}$                 | $I_{OH} = -50 \mu\text{A}$                          | 4.5 V        | 4.4                      | 4.5 |      | 4.4 |      | V    |
|                          | $I_{OH} = -8 \text{ mA}$                            |              | 3.94                     |     |      | 3.8 |      |      |
| $V_{OL}$                 | $I_{OL} = 50 \mu\text{A}$                           | 4.5 V        |                          |     | 0.1  |     | 0.1  | V    |
|                          | $I_{OL} = 8 \text{ mA}$                             |              |                          |     | 0.36 |     | 0.44 |      |
| $I_I$                    | $V_I = 5.5 \text{ V or GND}$                        | 0 V to 5.5 V |                          |     | ±0.1 |     | ±1   | μA   |
| $I_{CC}$                 | $V_I = V_{CC} \text{ or GND, } I_O = 0$             | 5.5 V        |                          |     | 1    |     | 10   | μA   |
| $\Delta I_{CC}^\ddagger$ | One input at 3.4 V, Other inputs at $V_{CC}$ or GND | 5.5 V        |                          |     | 1.35 |     | 1.5  | mA   |
| $C_i$                    | $V_I = V_{CC} \text{ or GND}$                       | 5 V          |                          | 4   | 10   |     | 10   | pF   |

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or  $V_{CC}$ .



# SN74AHCT1G04-Q1 SINGLE INVERTER GATE

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     |     | MIN | MAX | UNIT |
|-----------|-----------------|----------------|----------------------|--------------------------|-----|-----|-----|-----|------|
|           |                 |                |                      | MIN                      | TYP | MAX |     |     |      |
| $t_{PLH}$ | A               | Y              | $C_L = 15\text{ pF}$ | 4.7                      | 6.7 | 1   | 7.5 | ns  |      |
| $t_{PHL}$ |                 |                |                      | 4.7                      | 6.7 | 1   | 7.5 |     |      |
| $t_{PLH}$ | A               | Y              | $C_L = 50\text{ pF}$ | 5.5                      | 7.7 | 1   | 8.5 | ns  |      |
| $t_{PHL}$ |                 |                |                      | 5.5                      | 7.7 | 1   | 8.5 |     |      |

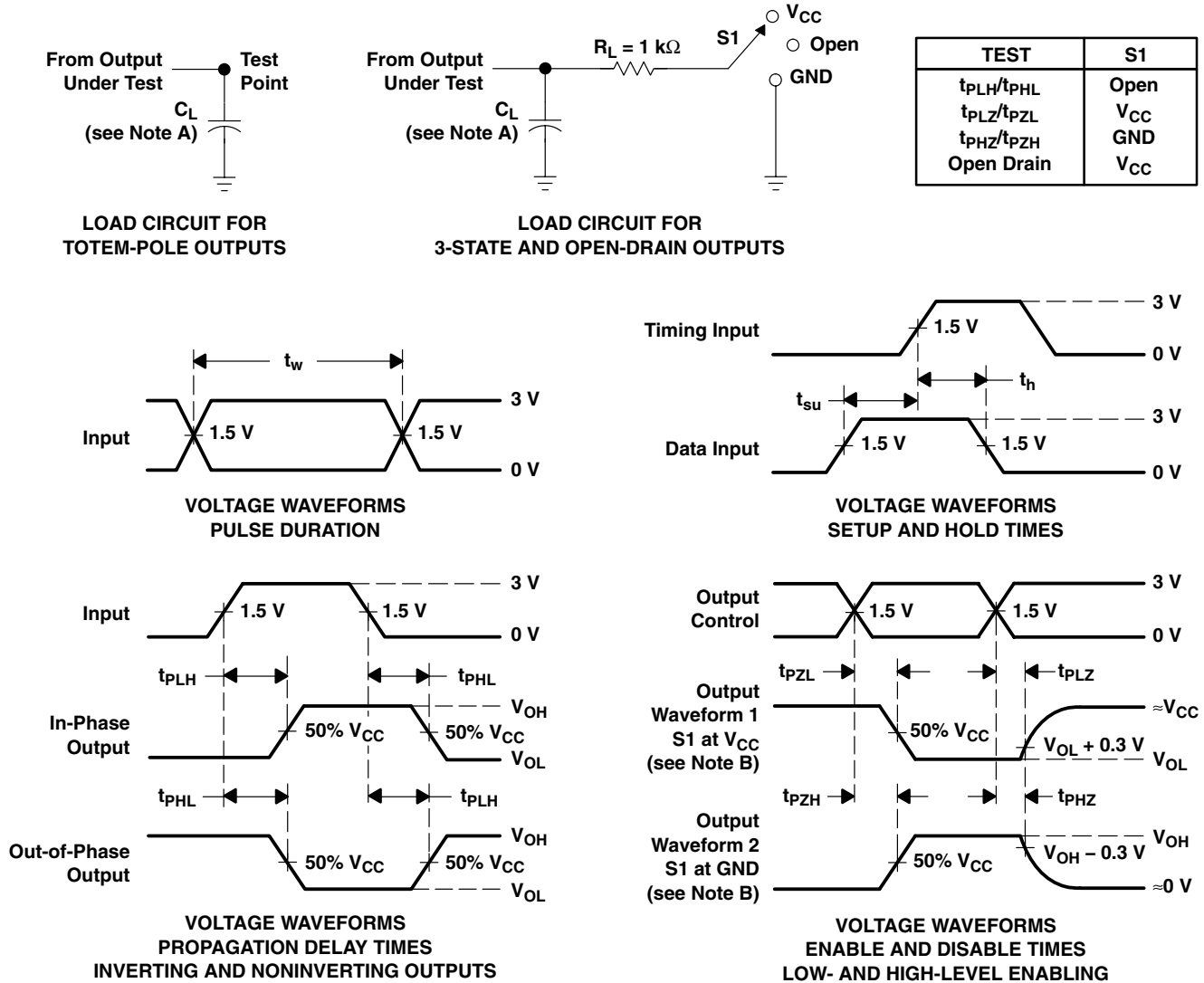
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER                              | TEST CONDITIONS             | TYP | UNIT |
|--|-----------------------------|-----|------|
| $C_{pd}$ Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 14  | pF   |

# SN74AHCT1G04-Q1 SINGLE INVERTER GATE

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device   | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CAHCT1G04QDCKRG4Q1 | ACTIVE        | SC70         | DCK             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU   Call TI     | Level-1-260C-UNLIM   | -40 to 125   | BCS                     | <a href="#">Samples</a> |
| CAHCT1G04QDCKRQ1   | ACTIVE        | SC70         | DCK             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | BCS                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AHCT1G04-Q1 :**

- Catalog: [SN74AHCT1G04](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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