- **Operating Range 2-V to 5.5-V V_{CC}**
- **Unbuffered Outputs**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
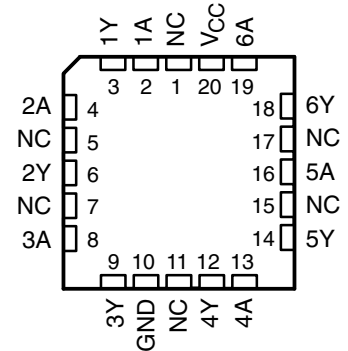 - **1000-V Charged-Device Model (C101)**

SN54AHCU04 . . . J OR W PACKAGE
SN74AHCU04 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)

1A	1		14	V_{CC}
1Y	2		13	6A
2A	3		12	6Y
2Y	4		11	5A
3A	5		10	5Y
3Y	6		9	4A
GND	7		8	4Y

SN74AHCU04 . . . RGY PACKAGE
(TOP VIEW)

1A (1), V_{CC} (14)
1Y (2) — 6A (13)
2A (3) — 6Y (12)
2Y (4) — 5A (11)
3A (5) — 5Y (10)
3Y (6) — 4A (9)
GND (7), 4Y (8)

SN54AHCU04 . . . FK PACKAGE
(TOP VIEW)

1Y (3), 1A (2), NC (1), V_{CC} (20), 6A (19)
2A (4) — 6Y (18)
NC (5) — NC (17)
2Y (6) — 5A (16)
NC (7) — NC (15)
3A (8) — 5Y (14)
3Y (9), GND (10), NC (11), 4Y (12), 4A (13)
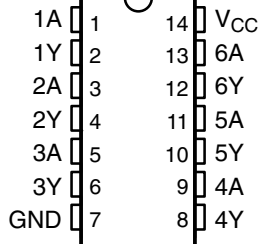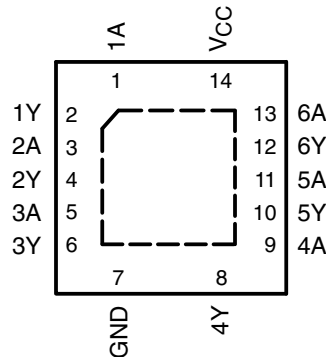
NC – No internal connection

description/ordering information

The 'AHCU04 devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$. Internal circuitry consists of single-stage inverters that can be used in analog applications such as crystal oscillators.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Tape and reel	SN74AHCU04RGYR	HD04
	PDIP – N	Tube	SN74AHCU04N	SN74AHCU04N
	SOIC – D	Tube	SN74AHCU04D	AHCU04
		Tape and reel	SN74AHCU04DR	
	SOP – NS	Tape and reel	SN74AHCU04NSR	AHCU04
	SSOP – DB	Tape and reel	SN74AHCU04DBR	HD04
	TSSOP – PW	Tube	SN74AHCU04PW	HD04
		Tape and reel	SN74AHCU04PWR	
	TVSOP – DGV	Tape and reel	SN74AHCU04DGVR	HD04
−55°C to 125°C	CDIP – J	Tube	SNJ54AHCU04J	SNJ54AHCU04J
	CFP – W	Tube	SNJ54AHCU04W	SNJ54AHCU04W
	LCCC – FK	Tube	SNJ54AHCU04FK	SNJ54AHCU04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

A ———————▷○——————— Y
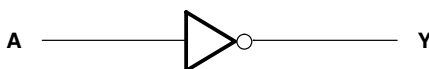
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . –20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 86°C/W
(see Note 2): DB package . . . . 96°C/W
(see Note 2): DGV package . . . . 127°C/W
(see Note 2): N package . . . . 80°C/W
(see Note 2): NS package . . . . 76°C/W
(see Note 2): PW package . . . . 113°C/W
(see Note 3): RGY package . . . . 47°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

TEXAS
INSTRUMENTS

recommended operating conditions (see Note 4)

			SN54AHCU04 MIN	SN54AHCU04 MAX	SN74AHCU04 MIN	SN74AHCU04 MAX	UNIT
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.7		1.7		V
		V_{CC} = 3 V	2.4		2.4		
		V_{CC} = 5.5 V	4.4		4.4		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.3		0.3	V
		V_{CC} = 3 V		0.6		0.6	
		V_{CC} = 5.5 V		1.1		1.1	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V_{CC} = 5 V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54AHCU04 MIN	SN54AHCU04 MAX	SN74AHCU04 MIN	SN74AHCU04 MAX	UNIT
V_{OH}	I_{OH} = −50 μA	2 V	1.8	2		1.8		1.8		V
		3 V	2.7	3		2.7		2.7		
		4.5 V	4	4.5		4		4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
	I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}	I_{OL} = 50 μA	2 V			0.2		0.2		0.2	V
		3 V			0.3		0.3		0.3	
		4.5 V			0.5		0.5		0.5	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i	V_I = V_{CC} or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

TEXAS INSTRUMENTS

SN54AHCU04, SN74AHCU04
HEX INVERTERS

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCU04		SN74AHCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5*	7.1*	1*	8.5*	1	8.5	ns
t_{PHL}					5*	7.1*	1*	8.5*	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	1	12	ns
t_{PHL}					7.5	10.6	1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCU04		SN74AHCU04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.5*	5.5*	1*	6*	1	6.5	ns
t_{PHL}					3.5*	5.5*	1*	6*	1	6.5	
t_{PLH}	A	Y	C_L = 50 pF		5	7	1	8	1	8	ns
t_{PHL}					5	7	1	8	1	8	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

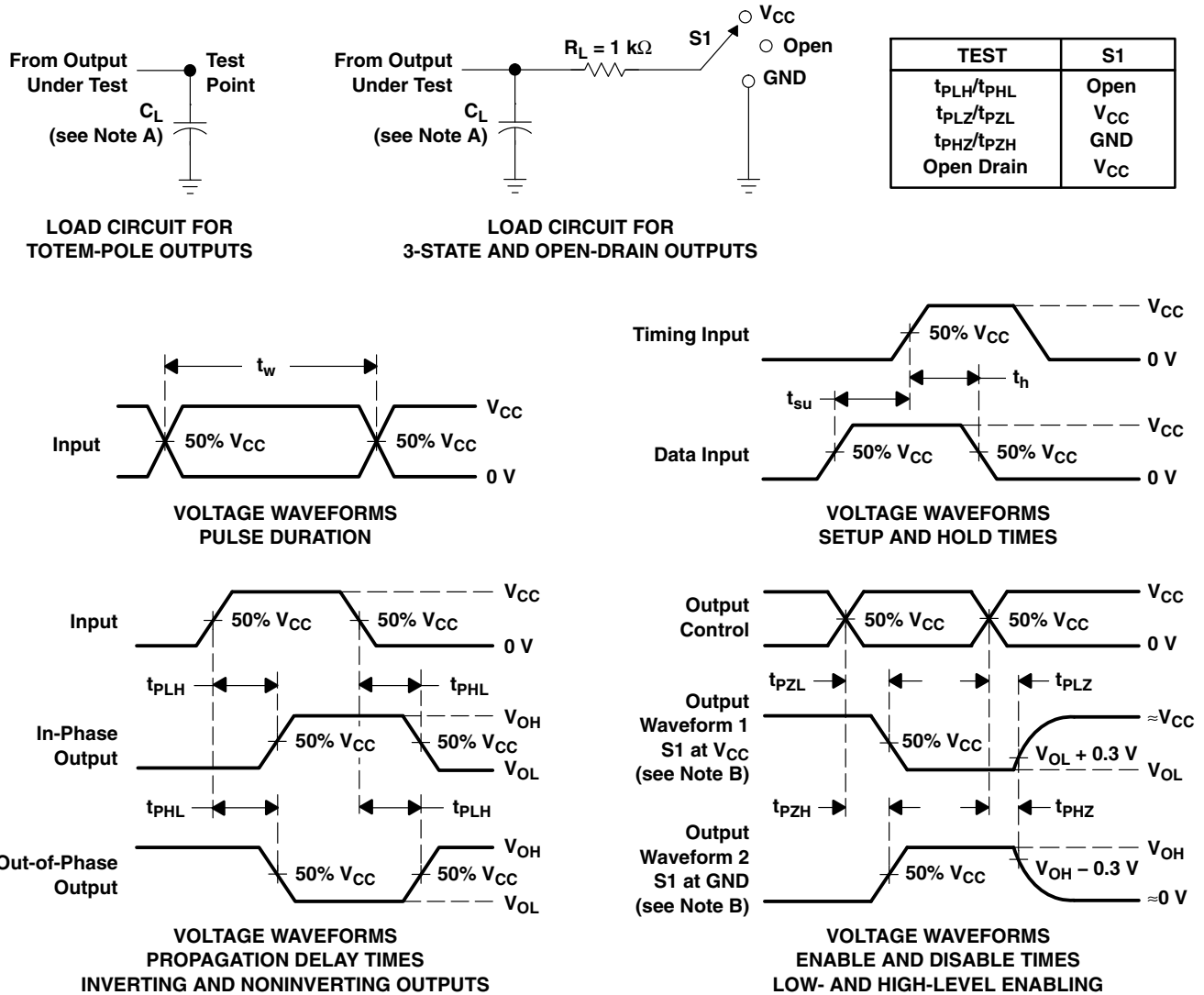| PARAMETER		SN74AHCU04			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.3		V
$V_{IH(D)}$	High-level dynamic input voltage	4			V
$V_{IL(D)}$	Low-level dynamic input voltage			1	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	7.3	pF

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PARAMETER MEASUREMENT INFORMATION

From Output Under Test **Test Point**

C_L (see Note A)

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

From Output Under Test $R_L = 1\ k\Omega$ **S1**

○ V_{CC}
○ Open
○ GND

C_L (see Note A)

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

Input — t_w — 50% V_{CC} ... 50% V_{CC} — V_{CC} / 0 V

VOLTAGE WAVEFORMS PULSE DURATION

Timing Input — 50% V_{CC} — V_{CC} / 0 V

t_{su} t_h

Data Input — 50% V_{CC} ... 50% V_{CC} — V_{CC} / 0 V

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

Input — 50% V_{CC} ... 50% V_{CC} — V_{CC} / 0 V

t_{PLH} ... t_{PHL}

In-Phase Output — 50% V_{CC} ... 50% V_{CC} — V_{OH} / V_{OL}

t_{PHL} ... t_{PLH}

Out-of-Phase Output — 50% V_{CC} ... 50% V_{CC} — V_{OH} / V_{OL}

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

Output Control — 50% V_{CC} ... 50% V_{CC} — V_{CC} / 0 V

t_{PZL} ... t_{PLZ}

Output Waveform 1 S1 at V_{CC} (see Note B) — 50% V_{CC} — ≈V_{CC} / V_{OL} + 0.3 V / V_{OL}

t_{PZH} ... t_{PHZ}

Output Waveform 2 S1 at GND (see Note B) — 50% V_{CC} — V_{OH} / V_{OH} − 0.3 V / ≈0 V

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B.   Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C.   All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\ \Omega$, $t_r ≤ 3$ ns, $t_f ≤ 3$ ns.
D.   The outputs are measured one at a time with one input transition per measurement.
E.   All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9680301Q2A SNJ54AHCU04FK	Samples
5962-9680301QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QCA SNJ54AHCU04J	Samples
5962-9680301QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QDA SNJ54AHCU04W	Samples
SN74AHCU04D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	Samples
SN74AHCU04DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	Samples
SN74AHCU04DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	Samples
SN74AHCU04DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	Samples
SN74AHCU04DGVR	OBSOLETE	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04DGVRE4	OBSOLETE	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04DGVRG4	OBSOLETE	TVSOP	DGV	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	Samples
SN74AHCU04DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	Samples
SN74AHCU04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCU04N	Samples
SN74AHCU04NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCU04N	Samples
SN74AHCU04NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCU04	Samples
SN74AHCU04PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCU04PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCU04PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	Samples
SN74AHCU04PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HD04	Samples
SNJ54AHCU04FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9680301Q2A SNJ54AHCU 04FK	Samples
SNJ54AHCU04J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QCA SNJ54AHCU04J	Samples
SNJ54AHCU04W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9680301QDA SNJ54AHCU04W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHCU04, SN74AHCU04 :

- Catalog: SN74AHCU04

- Automotive: SN74AHCU04-Q1, SN74AHCU04-Q1

- Enhanced Product: SN74AHCU04-EP, SN74AHCU04-EP

- Military: SN54AHCU04

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCU04DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHCU04DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCU04NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCU04PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCU04DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AHCU04DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AHCU04NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AHCU04PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

DIM ＼ PINS **	14	16	18	20
[A]	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

[A]

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.260 (6,60)
0.235 (5,97)

0.008 (0,20)
0.004 (0,10)

0.080 (2,03)
0.045 (1,14)

0.280 (7,11) MAX

0.019 (0,48)
0.015 (0,38)

1   14

0.050 (1,27)

0.390 (9,91)
0.335 (8,51)

0.005 (0,13) MIN
4 Places

7   8

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180−2/F 04/14

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
        E. Falls within MIL STD 1835 GDFP1−F14

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FK (S−CQCC−N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

B SQ

A SQ

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a metal lid.
        D. Falls within JEDEC MS−004

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N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14) D
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

Gauge Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option D

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

	PINS **						
DIM	**14**	**16**	**20**	**24**	**38**	**48**	**56**
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
            14/16/20/56 Pins – MO-194

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

$\dfrac{0.344\ (8,75)}{0.337\ (8,55)}$ Ⓒ

14   8

$\dfrac{0.244\ (6,20)}{0.228\ (5,80)}$

$\dfrac{0.157\ (4,00)}{0.150\ (3,80)}$ /D\

1   7

Pin 1
Index Area

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

$\dfrac{0.010\ (0,25)}{0.004\ (0,10)}$

$\dfrac{0.010\ (0,25)}{0.005\ (0,13)}$

Gauge Plane

0.004 (0,10)

0.010 (0,25)

0°−8°

Seating Plane

$\dfrac{0.050\ (1,27)}{0.016\ (0,40)}$

4040047−5/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      /C\   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0.006 (0,15) each side.
      /D\   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AB.

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D (R–PDSO–G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

14x1,50

12x1,27

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

0,60

1,55

0.07
All Around

4211283–3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC–7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14   8

⟋D⟍ 4,50
     4,30

6,60
6,20

1   7

5,10
4,90

⟋C⟍

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌀ 0,10

4040064−3/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
        ⟋C⟍ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
        ⟋D⟍ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

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PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

├─12x0,65

5,60

Stencil Openings
(Note D)

├─ 14x0,30

├─12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

├─0,35

1,60

Example
Solder Mask Opening
(See Note E)

├─ 0,07
All Around

4211284−2/F 12/12

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Publication IPC−7351 is recommended for alternate designs.
           D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
           E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

1,27

0,51
0,35   ⊕ 0,25Ⓜ

14   8

5,60   8,20
5,00   7,40

1   7

A

0,15 NOM

Gage Plane

0,25

0°–10°   1,05
0,55

0,15
0,05

2,00 MAX

Seating Plane

△ 0,10

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-150

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