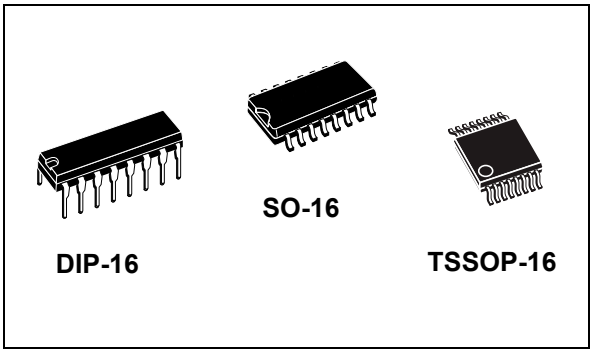
M74HC595

8-bit shift register with output latches (3-state)

Datasheet - production data



Features

- High speed: f_{MAX} = 59 MHz (typ.) at V_{CC} = 6 V
- Low power dissipation: I_{CC} = 4 µA (max.) at T_A= 25 °C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- Symmetrical output impedance:
  - $|I_{OH}| = I_{OL}$ = 6 mA (min.) for QA to QH
  - $|I_{OH}| = I_{OL}$ = 4 mA (min.) for QH'
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Wide operating voltage range: V_{CC} (opr.) = 2 V to 6 V
- Pin and function compatible with 74 series 595

Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The M74HC595 device is a high speed CMOS 8-bit shift register with output latches (3-state) fabricated with silicon gate C^2MOS technology.

This device contains an 8-bit serial in, parallel out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-state outputs. Separate clocks are provided for both the shift register and the storage register.

The shift register has direct overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Order code	Temperature range	Package	Packaging	Marking
M74HC595RM13TR	-55/+125 °C	SO-16	Tape and reel	74HC595
M74HC595YRM13TR(1)	-40/+125 °C	SO-16 (automotive grade)	Tape and reel	74HC595Y
M74HC595TTR	-55/+125 °C	TSSOP-16	Tape and reel	HC595
M74HC595YTTR(1)	-40/+125 °C	TSSOP-16(automotive grade)	Tape and reel	HC595Y
M74HC595B1R	-55/+125 °C	PDIP-16	Tube	M74HC595B1

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent are ongoing.

Contents

1 Pin information

Figure 1. Pin connection and IEC logic symbols

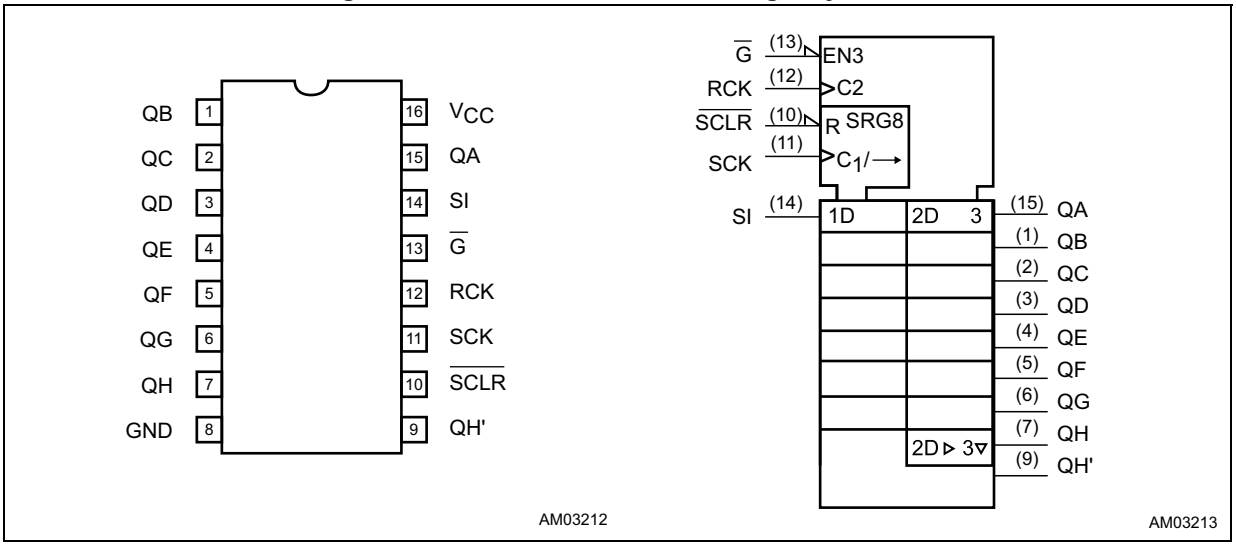
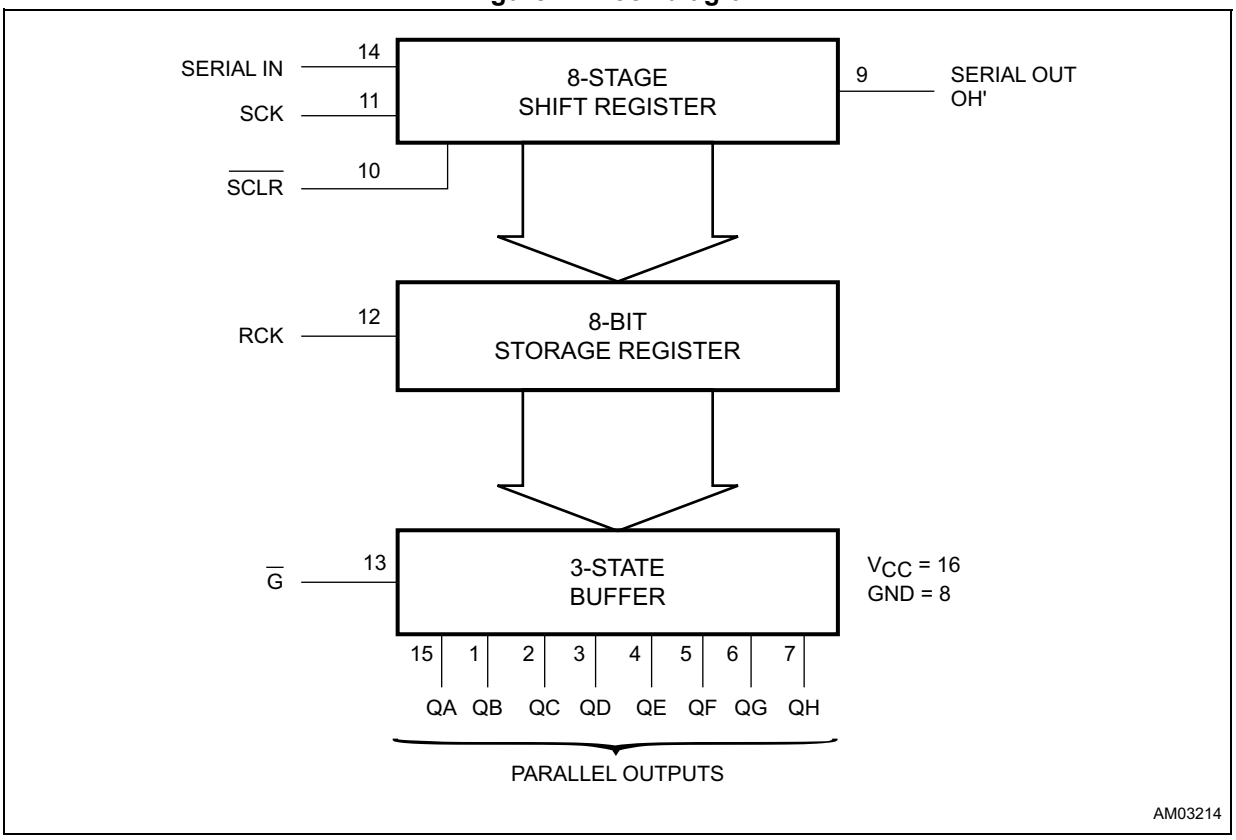


Table 2. Pin description

Pin no	Symbol	Name and function
1, 2, 3, 4, 5, 6, 7, 15	QA to QH	Data outputs
9	QH’	Serial data outputs
10	$\overline{SCLR}$	Shift register clear input
11	SCK	Shift register clock input
13	$\overline{G}$	Output enable input
14	SI	Serial data input
12	RCK	Storage register clock input
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

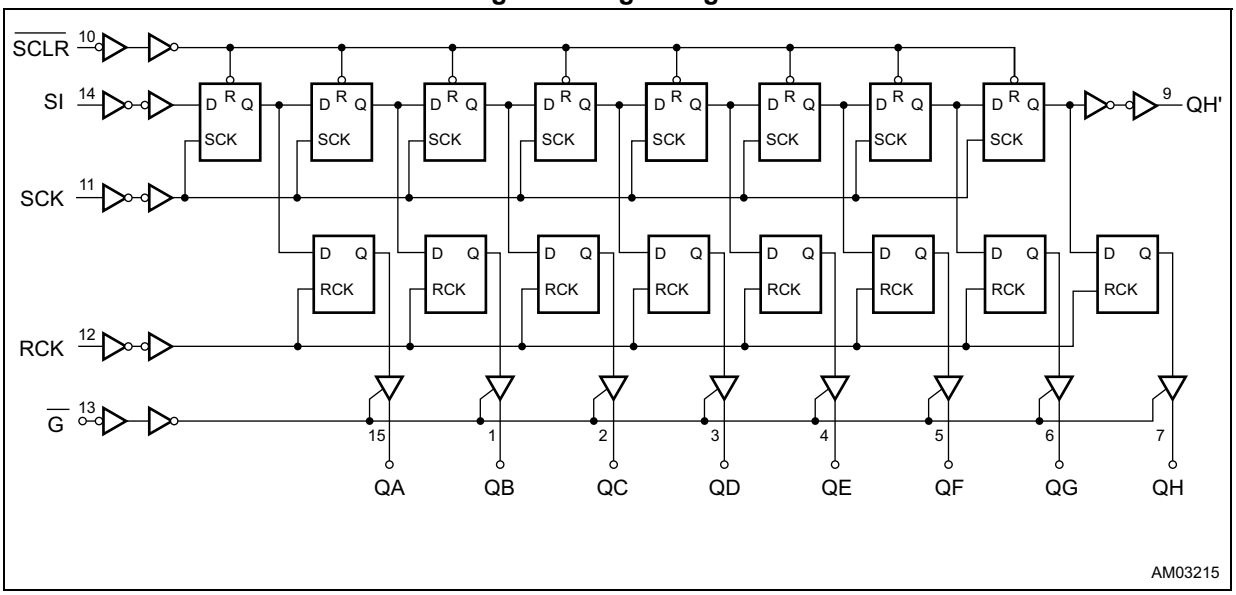
2 Functional description

Figure 2. Block diagram



1. This block diagram has not be used to estimate propagation delays.

Figure 3. Logic diagram



1. This logic diagram has not be used to estimate propagation delays.

Table 3. Truth table(1)

Inputs					Outputs
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared
L	⎍	H	X	X	First stage of S.R. becomes “L” other stages store the data of previous stage, respectively
H	⎍	H	X	X	First stage of S.R. becomes “H” other stages store the data of previous stage, respectively
X	⎎	H	X	X	State of S.R. is not changed
X	X	X	⎍	X	S.R. data is stored into storage register
X	X	X	⎎	X	Storage register state is not changed

1. X: don’t care.

Figure 4. Timing chart

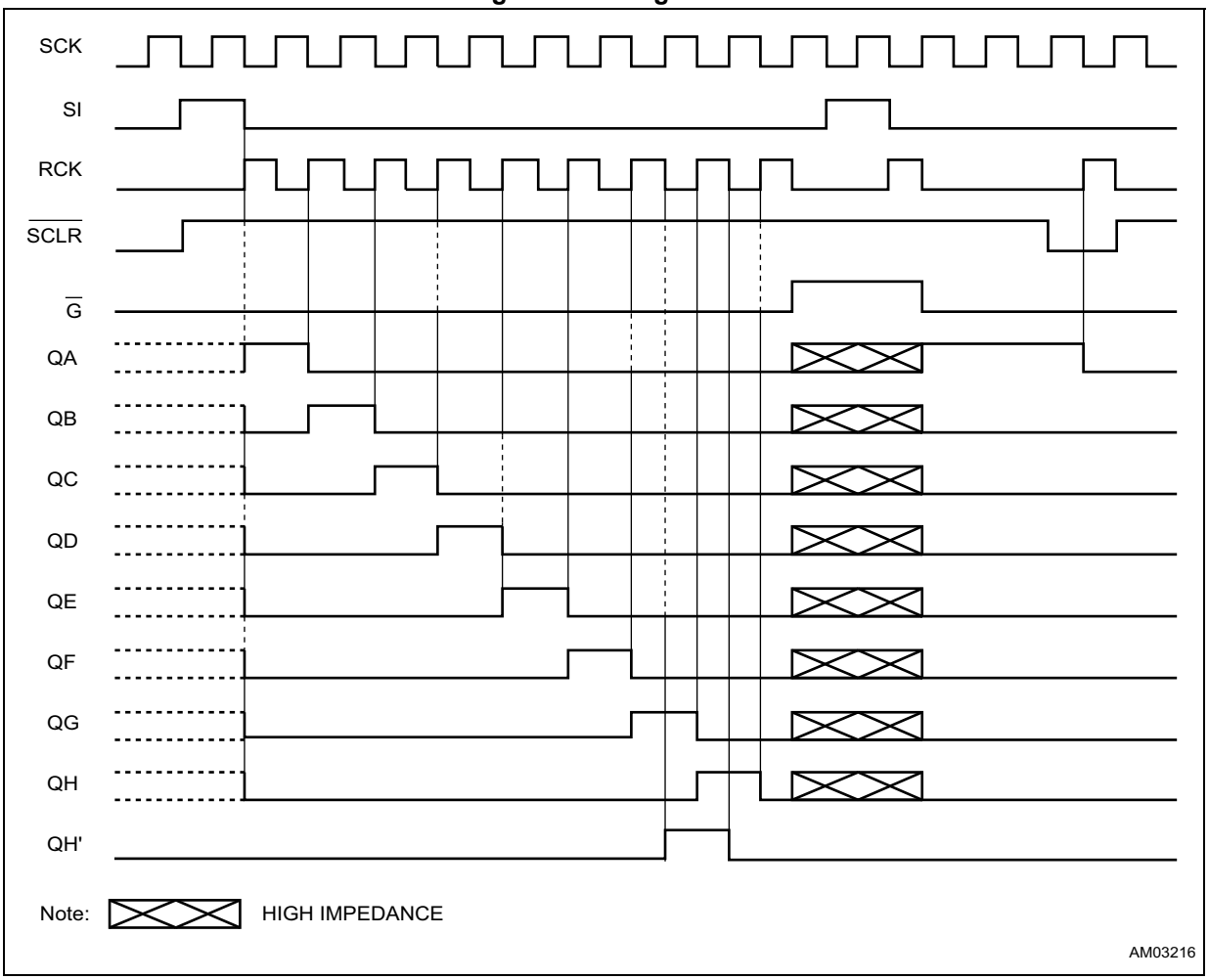
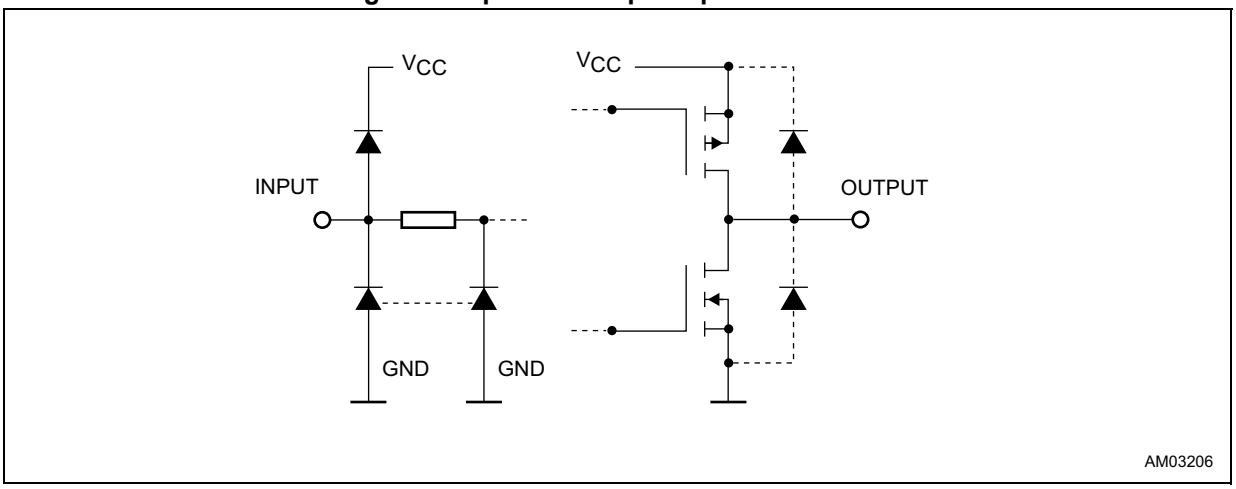


Figure 5. Input and output equivalent circuit



3 Electrical description

Table 4. Absolute maximum ratings(1)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		-0.5 to +7	V
V_I	DC input voltage		-0.5 to V_{CC} + 0.5	V
V_O	DC output voltage		-0.5 to V_{CC} + 0.5	V
I_{IK}	DC input diode current		± 20	mA
I_{OK}	DC output diode current		± 20	mA
I_O	DC output current		± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current		± 70	mA
P_D	Power dissipation	DIP	750(2)	mW
		SOP	500(2)	mW
		TSSOP	450(2)	mW
T_{stg}	Storage temperature		-65 to +150	°C
T_L	Lead temperature (10 sec.)		300	°C

1. Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
2. Power dissipation at 65 °C. Derating from 65 °C to 125 °C: DIP package -10 mW/°C; SO package -7 mW/°C; TSSOP package -6.1 mW/°C.

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		2 to 6	V
V_I	Input voltage		0 to V_{CC}	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
t_r, t_f	Input rise and fall time	V_{CC} = 2.0 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	ns
		V_{CC} = 6.0 V	0 to 400	ns

Table 6. DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High level input voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low level input voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High level output voltage (for QH' outputs)	2.0	I_O = -20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O = -20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O = -20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O = -7.8 mA	5.68	5.8		5.63		5.60		
V_{OH}	High level output voltage (for QA to QH outputs)	2.0	I_O = -20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O = -20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O = -20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O = -6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O = -7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low level output voltage (for QH' outputs)	2.0	I_O = 20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O = 20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O = 20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O = 7.8 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low level output voltage (for QA to QH outputs)	2.0	I_O = 20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O = 20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O = 20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O = 6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O = 7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input leakage current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High impedance output leakage current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 10	µA
I_{CC}	Quiescent supply current	6.0	V_I = V_{CC} or GND			4		40		80	µA

Table 7. AC electrical characteristics (C_L = 50 pF, input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH}, t_{THL}	Output transition time (Qn)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{TLH}, t_{THL}	Output transition time (QH')	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH}, t_{PHL}	Propagation delay time (SCK - QH')	2.0	50			45	125		155		190	ns
		4.5				15	25		31		38	
		6.0				13	21		26		32	
t_{PLH}, t_{PHL}	Propagation delay time ($\overline{SCLR}$ - QH')	2.0	50			60	175		220		265	ns
		4.5				18	35		44		53	
		6.0				15	30		37		45	
t_{PLH}, t_{PHL}	Propagation delay time (RCK - Qn)	2.0	50			60	150		190		225	ns
		4.5				20	30		38		45	
		6.0				17	26		32		38	
		2.0	150			75	190		240		285	ns
		4.5				25	38		48		57	
		6.0				22	32		41		48	
t_{PZL}, t_{PZH}	High impedance output enable time	2.0	50	R_L = 1 KΩ		45	135		170		205	ns
		4.5				15	27		34		41	
		6.0				13	23		29		35	
		2.0	150	R_L = 1 KΩ		60	175		220		265	ns
		4.5				20	35		44		53	
		6.0				17	30		37		45	
t_{PLZ}, t_{PHZ}	High impedance output disable time	2.0	50	R_L = 1 KΩ		30	150		190		225	ns
		4.5				15	30		38		45	
		6.0				14	26		32		38	

Table 7. AC electrical characteristics (C_L = 50 pF, input t_r = t_f = 6 ns) (continued)

Symbol	Parameter	Test condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum clock frequency	2.0	50		6.0	17		4.8		4		MHz
		4.5			30	50		24		20		
		6.0			35	59		28		24		
		2.0	150		5.2	14		4.2		3.4		MHz
		4.5			26	40		21		17		
		6.0			31	45		25		20		
$t_{W(H)}$	Minimum pulse width (SCK, RCK)	2.0	50			17	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
$t_{W(L)}$	Minimum pulse width ($\overline{SCLR}$)	2.0	50			20	75		95		110	ns
		4.5				6	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum setup time (SI - CCK)	2.0	50			25	50		65		75	ns
		4.5				5	10		13		15	
		6.0				4	9		11		13	
t_s	Minimum setup time (SCK - RCK)	2.0	50			35	75		95		110	ns
		4.5				8	15		19		22	
		6.0				6	13		16		19	
t_s	Minimum setup time ($\overline{SCRL}$ - RCK)	2.0	50			40	100		125		145	ns
		4.5				10	20		25		29	
		6.0				7	17		21		25	
t_h	Minimum hold time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum clear removal time	2.0	50			15	50		65		75	ns
		4.5				3	10		13		15	
		6.0				3	9		11		13	

Table 8. Capacitive characteristics

Symbol	Parameter	Test condition	Value							Unit
		V_{CC} (V)	T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input capacitance			5	10		10		10	pF
C_{PD}	Power dissipation capacitance(1)			184						pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to *Figure 6: Test circuit*). Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$.

Figure 6. Test circuit

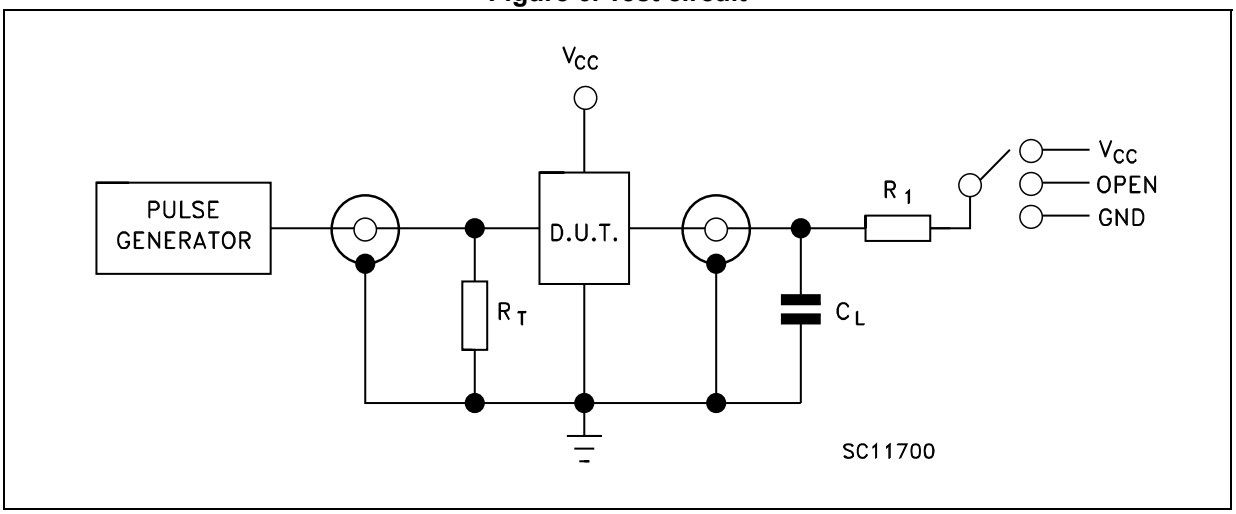


Table 9. Propagation delay time configuration

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

Note: *C_L = 50 pF/150 pF or equivalent (includes jig and probe capacitance)*
R_1 = 1 KΩ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω).

Figure 7. Waveform 1: SCK to QH' propagation delay times, SCK minimum pulse width (f = 1 MHz; 50% duty cycle)

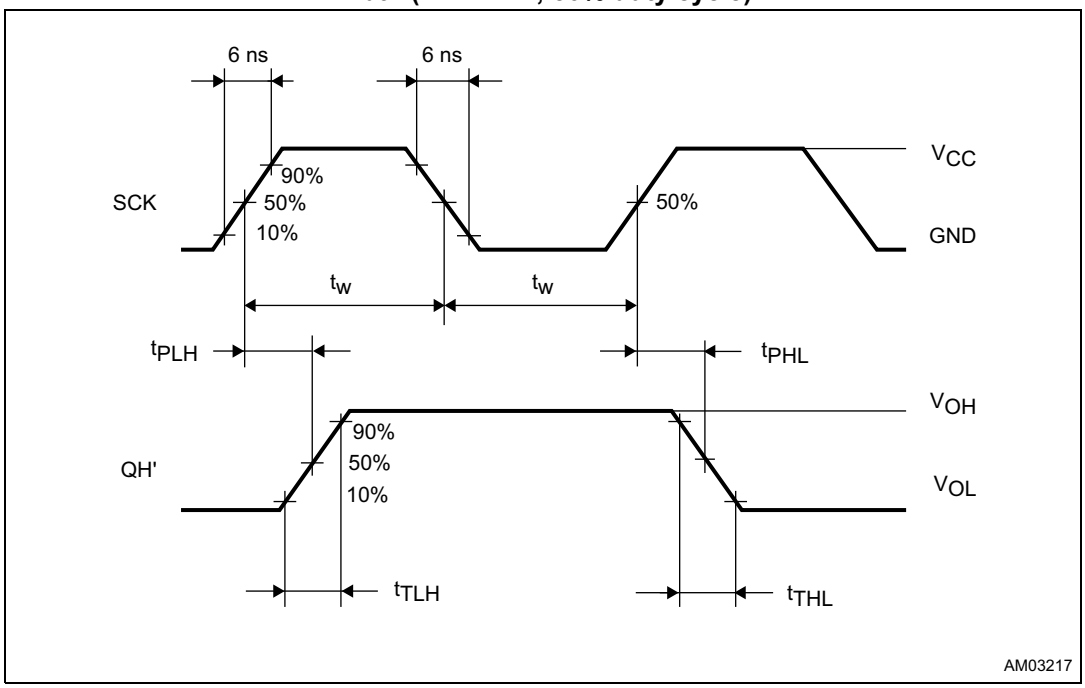


Figure 8. Waveform 2: RCK to QN propagation delay times (f = 1 MHz; 50% duty cycle)

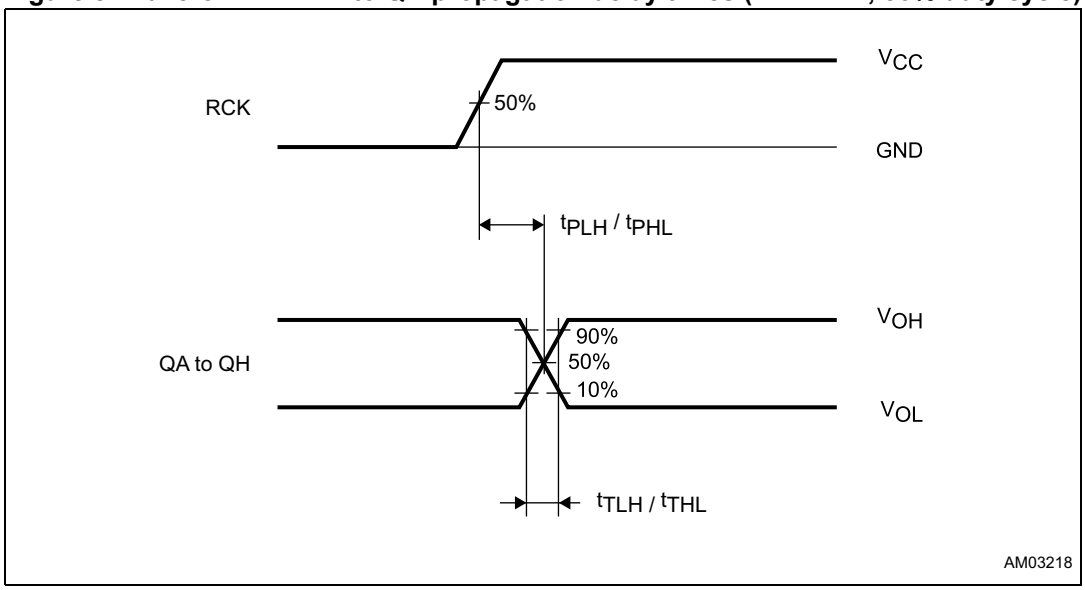


Figure 9. Waveform 3: SI to SCK setup and hold times (f = 1 MHz; 50% duty cycle)

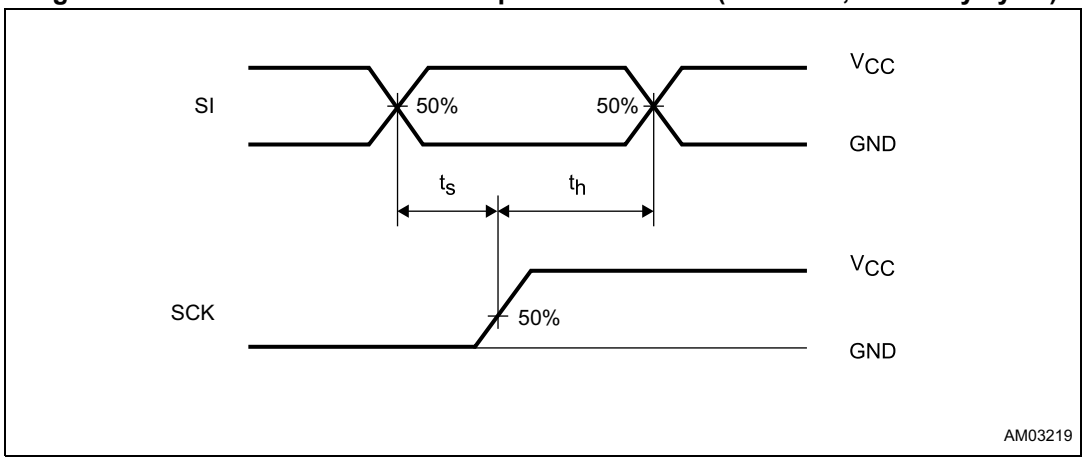


Figure 10. Waveform 4: SCK to RCK setup and hold times (f = 1 MHz; 50% duty cycle)

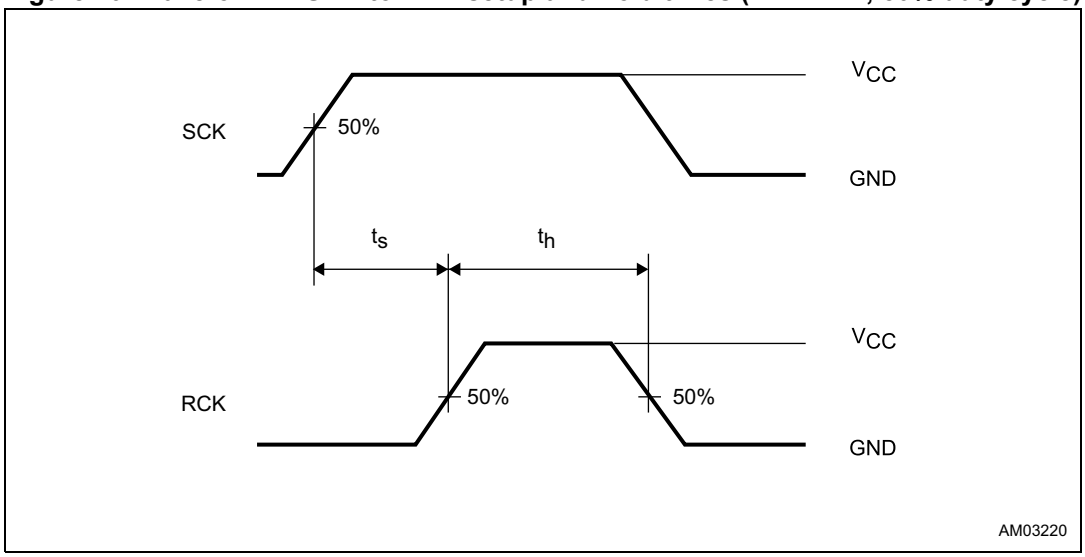


Figure 11. Waveform 5: $\overline{\text{SCLR}}$ minimum pulse width, minimum removal time (f = 1 MHz; 50% duty cycle)

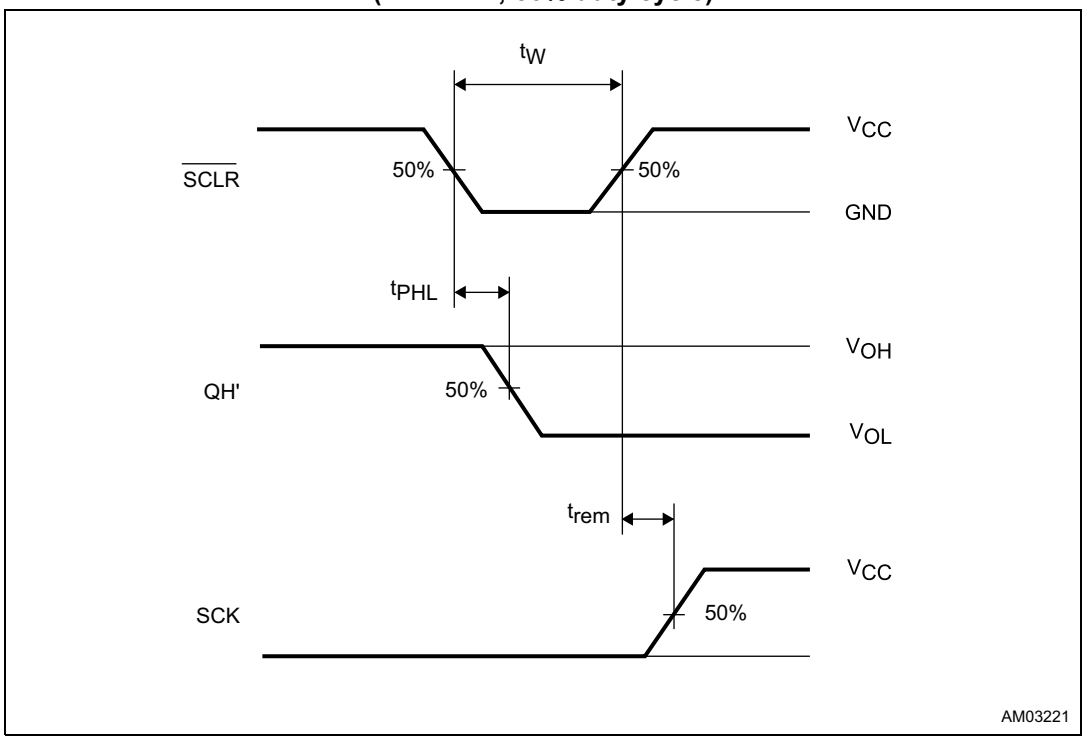


Figure 12. Waveform 6: OUTPUT ENABLE and DISABLE times (f = 1 MHz; 50% duty cycle)

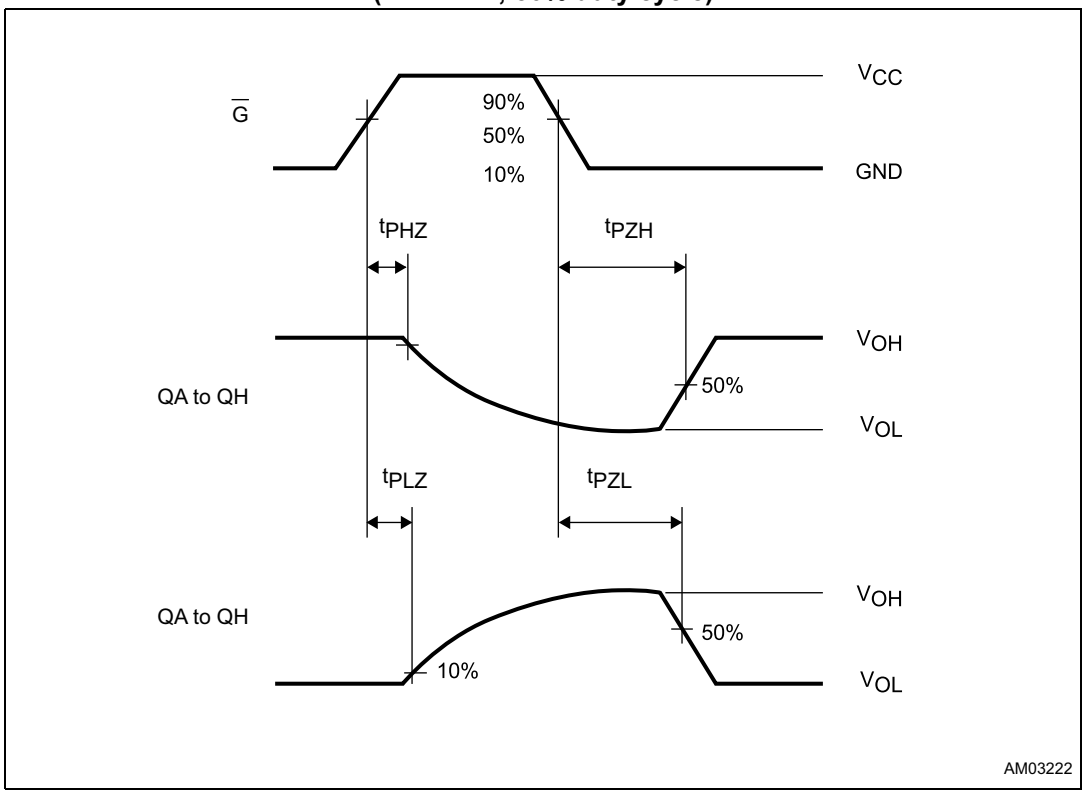
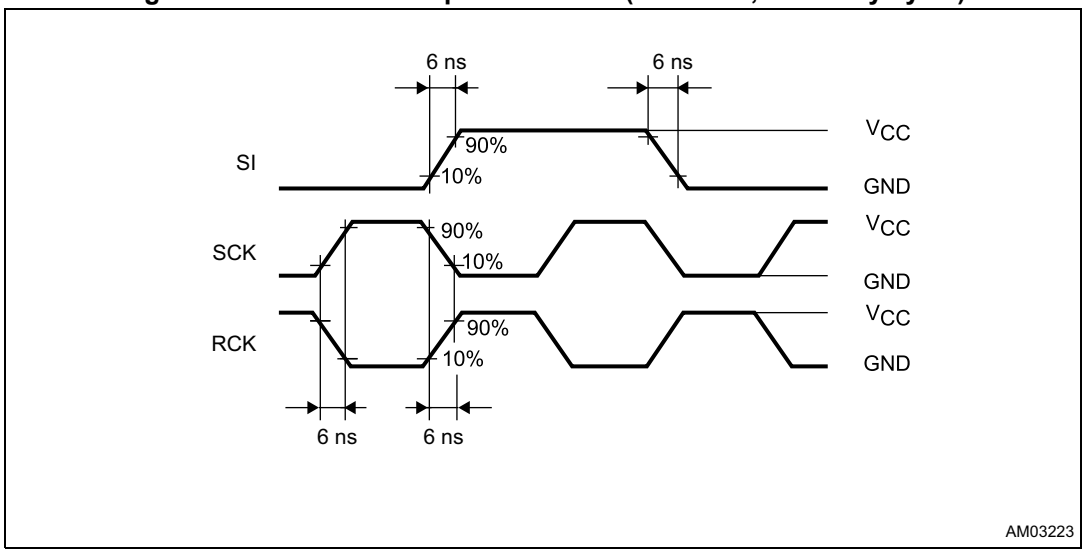


Figure 13. Waveform 7: input waveform (f = 1 MHz; 50% duty cycle)



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 14. Plastic DIP-16 (0.25) package outline

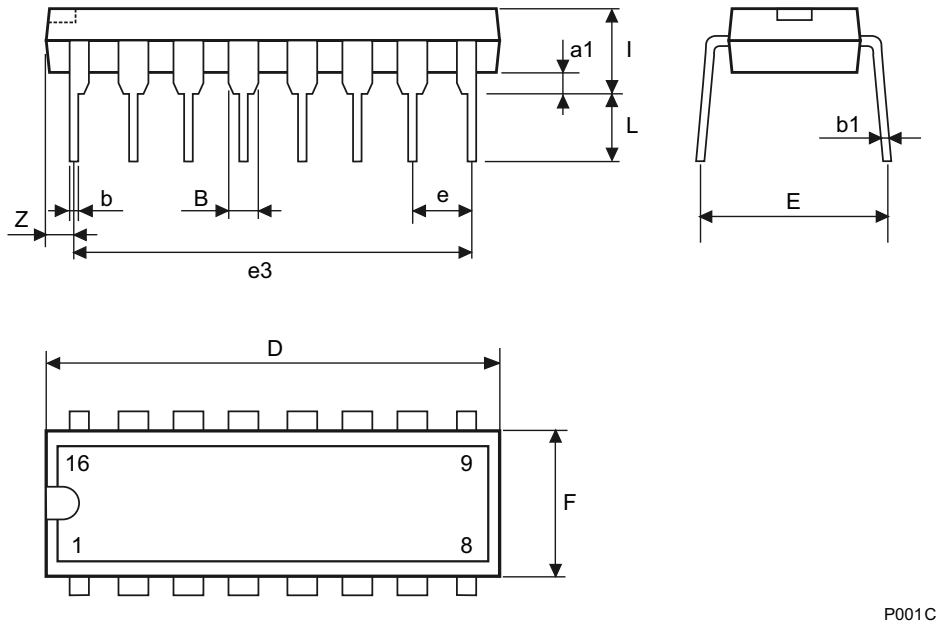


Table 10. Plastic DIP-16 (0.25) package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

Figure 15. SO-16 package outline

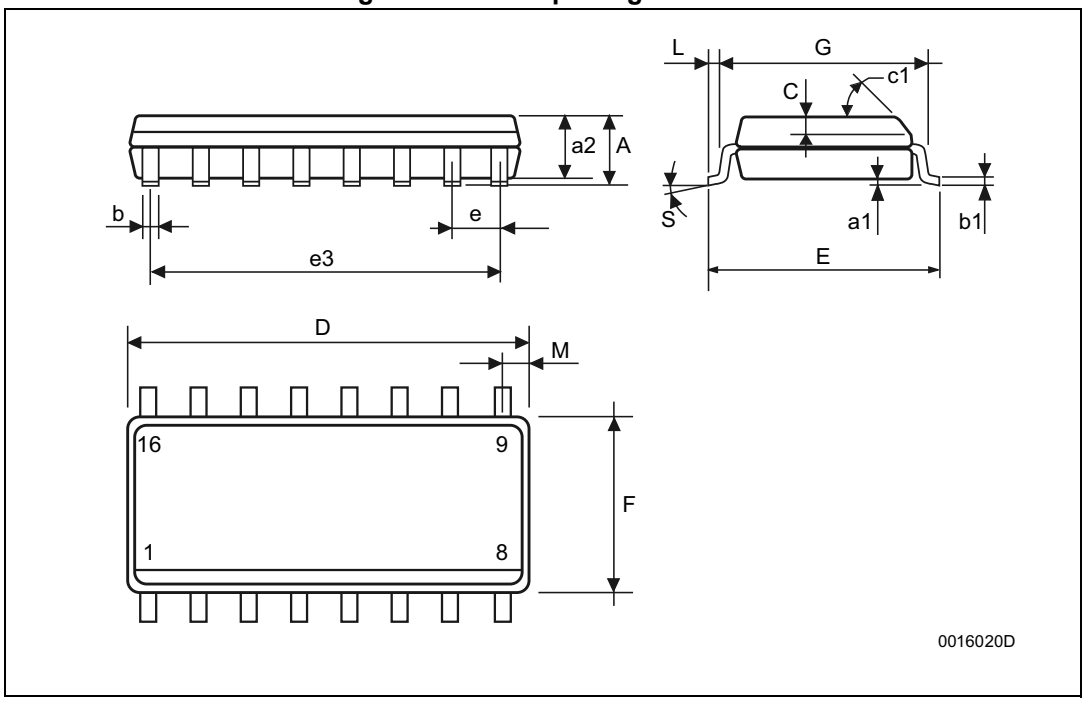
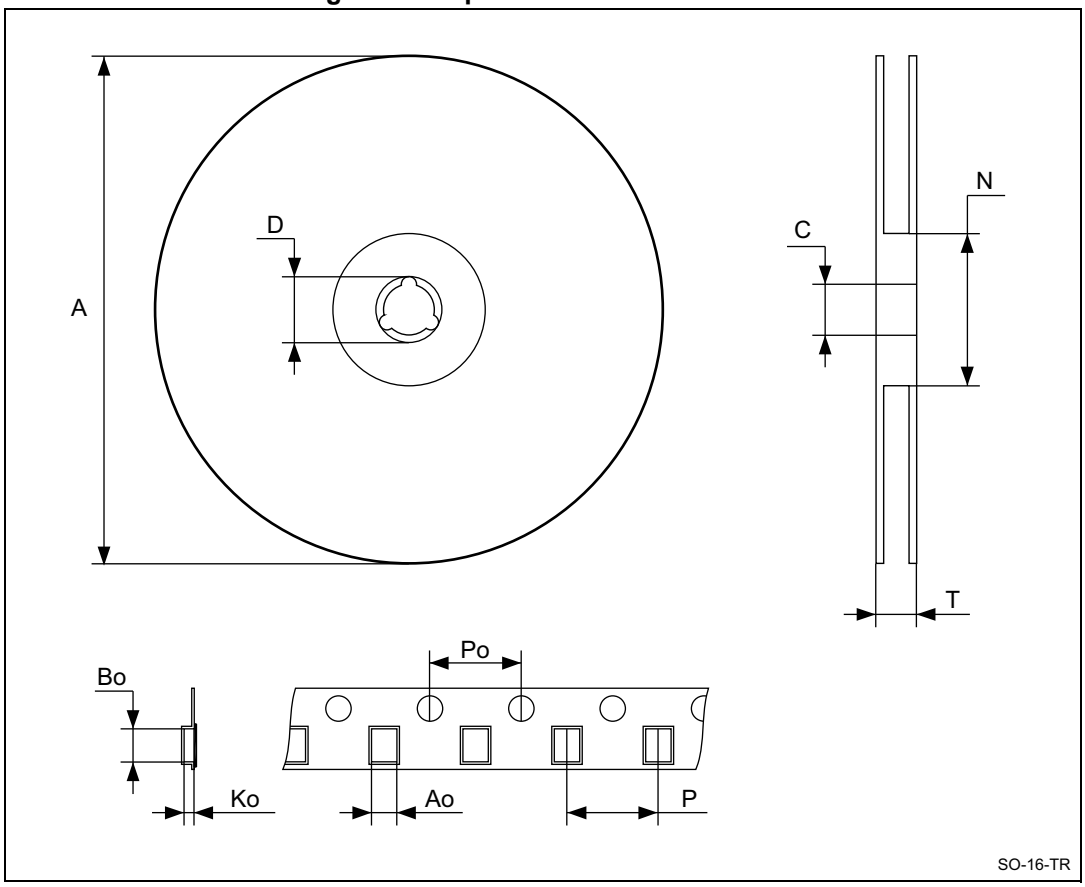


Table 11. SO-16 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.004		0.008
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

Figure 16. Tape and reel SO-16 outline



1. Drawing is not in scale.

Table 12. Tape and reel SO-16 mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

Figure 17. TSSOP-16 package outline

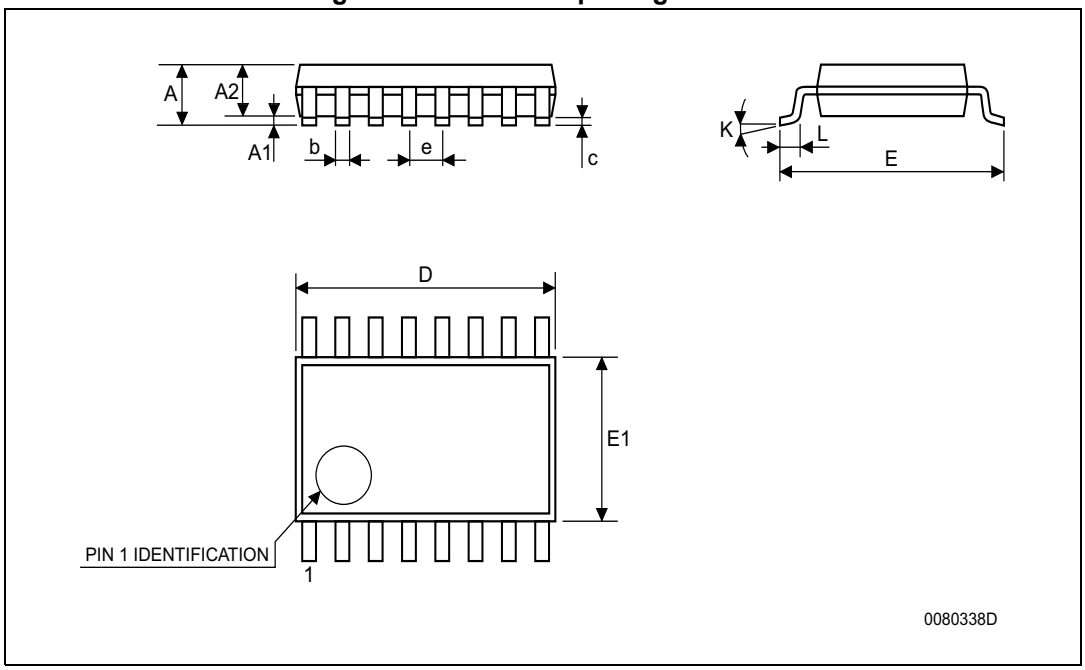
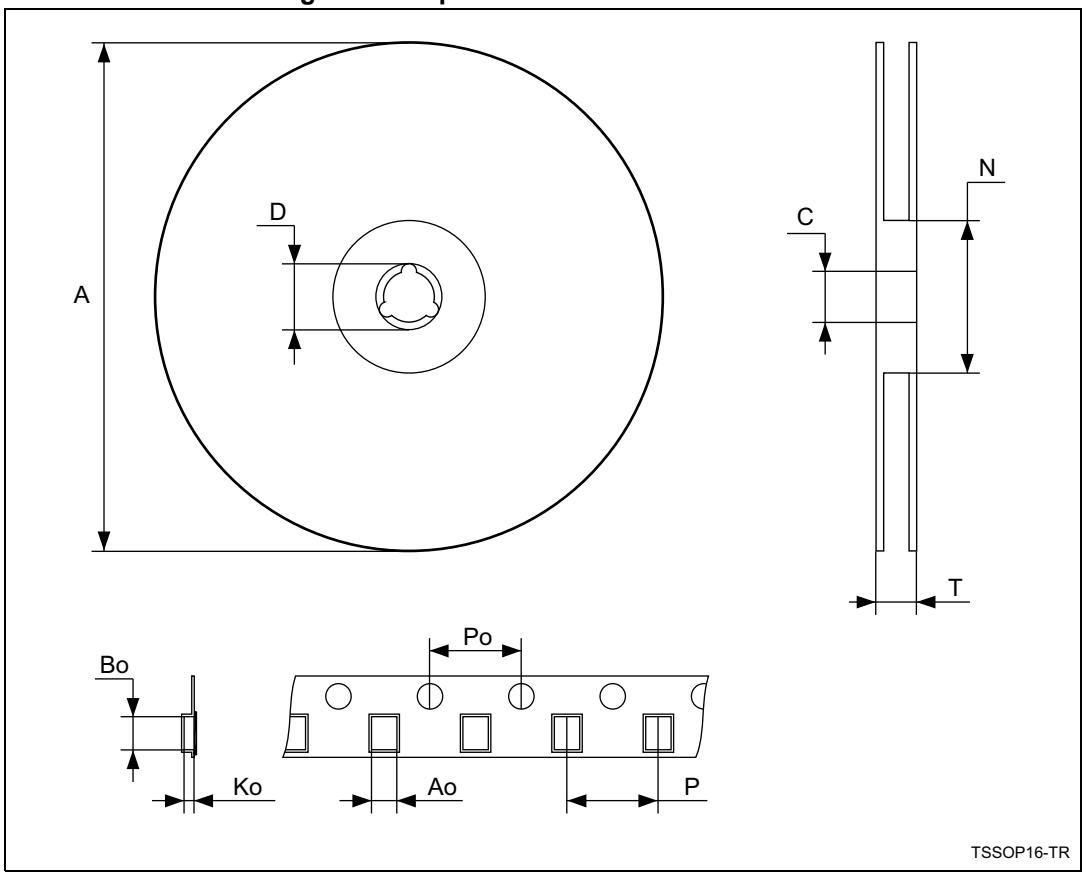


Table 13. TSSOP-16 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5 5	.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 18. Tape and reel TSSOP-16 outline



1. Drawing is not in scale.

Table 14. Tape and reel TSSOP-16 mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

5 Revision history

Table 15. Document revision history

Date	Revision	Changes
18-Apr-2013	5	Added *Applications* to page 1. Updated *Table 1* (updated data, removed M74HC595M1R order code, added M74HC595RM13TR, M74HC595YRM13TR, M74HC595TTR, and M74HC595YTTR order code, temperature range, marking, updated package and packaging). Redrawn *Figure 1* to *Figure 4* and *Figure 7* to *Figure 13*. Moved *Figure 1* to page 3. Added *Contents*. Added titles to *Section 1* to *Section 5* (reformatted *Section 1* and *Section 2*). Added title to *Table 9*. Added cross-reference to note *1.* below *Table 8*. Added ECOPACK text to *Section 4*, reformatted *Section 4* (reversed order of figures and tables, added titles to *Figure 14* to *Figure 18* and *Table 10* to *Table 14*, moved notes below *Figure 16* and *Figure 18*). Added *Table 15*. Minor corrections throughout document.

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