Clock Buffer/Clock Multiplier With Optional SSC

FEATURES

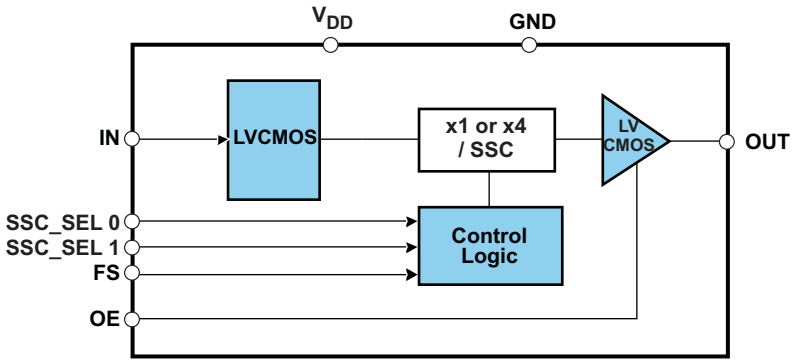
- **Part of a Family of Easy to use Clock Generator Devices With Optional SSC**
- **Clock Multiplier With Selectable Output Frequency and Selectable SSC**
- **SSC Controllable via 2 External Pins**
  - **±0%, ±0.5%, ±1%, ±2% Center Spread**
- **Frequency Multiplication Selectable Between x1 or x4 With One External Control Pin**
- **Output Disable via Control Pin**
- **Single 3.3V Device Power Supply**
- **Wide Temperature Range –40°C to 85°C**
- **Low Space Consumption by 8 Pin TSSOP Package**

APPLICATIONS

- **Consumer and Industrial Applications requiring EMI reduction through Spread Spectrum Clocking and/ or Clock Multiplication**

PACKAGE

BLOCK DIAGRAM



DESCRIPTION

The CDCS503 is a spread spectrum capable, LVCMOS Input Clock Buffer with selectable frequency multiplication.

It shares major functionality with the CDCS502 but utilizes a LVCMOS input stage instead of the crystal input stage of the CDCS502. Also an Output Enable pin has been added to the CDCS503.

The device accepts a 3.3V LVCMOS signal at the input.

The input signal is processed by a PLL, whose output frequency is either equal to the input frequency or multiplied by the factor of 4.

The PLL is also able to spread the clock signal by ±0%, ±0.5%, ±1% or ±2% centered around the output clock frequency with a triangular modulation.

By this, the device can generate output frequencies between 8MHz and 108MHz with or without SSC.

A separate control pin can be used to enable or disable the output. The CDCS503 operates in 3.3V environment.

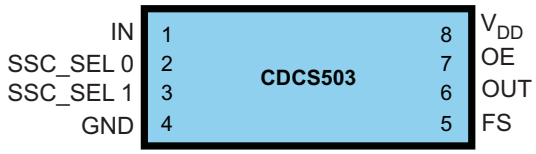
It is characterized for operation from –40°C to 85°C, and available in an 8-pin TSSOP package.

FUNCTION TABLE

OE	FS	SSC_SEL 0	SSC_SEL 1	SSC AMOUNT	f_{OUT}/f_{IN}	f_{OUT} at f_{in} = 27 MHz
0	x	x	x	x	x	3-state
1	0	0	0	±0.00%	1	27 MHz
1	0	0	1	±0.50%	1	27 MHz
1	0	1	0	±1.00%	1	27 MHz
1	0	1	1	±2.00%	1	27 MHz
1	1	0	0	±0.00%	4	108 MHz
1	1	0	1	±0.50%	4	108 MHz
1	1	1	0	±1.00%	4	108 MHz
1	1	1	1	±2.00%	4	108 MHz

DEVICE INFORMATION

PACKAGE



PIN FUNCTIONS

SIGNAL	PIN	TYPE	DESCRIPTION
IN	1	I	LVCMOS Clock input
OUT	6	O	LVCMOS Clock Output
SSC_SEL 0, 1	2, 3	I	Spread Selection Pins, internal pull-up
OE	7	I	Output Enable, internal pull-up
FS	5	I	Frequency Multiplication Selection, internal pull-up
V_{DD}	8	Power	3.3V Power Supply
GND	4	Ground	Ground

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE

over operating free-air temperature range (unless otherwise noted)(1)

CDCS503PW 8-PIN TSSOP			THERMAL AIRFLOW (CFM)				UNIT
			0	150	250	500	
$R_{\theta JA}$	High K		149	142	138	132	°C/W
	Low K		230	185	170	150	
$R_{\theta JC}$	High K	65					°C/W
	Low K	69					

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	Supply voltage range	–0.5 to 4.6	V
V_{IN}	Input voltage range(1)	–0.5 to 4.6	V
V_{out}	Output voltage range(1)	–0.5 to 4.6	V
I_{IN}	Input current (V_I < 0, V_I > VDD)	20	mA
I_{out}	Continuous output current	50	mA
T_{ST}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3.0		3.6	V
f_{IN}	Input frequency	FS = 0	8		32	MHz
		FS = 1	8		27	
V_{IL}	Low level input voltage LVCMOS				0.3 V_{DD}	V
V_{IH}	High level input voltage LVCMOS		0.7 V_{DD}			V
V_I	Input voltage threshold LVCMOS			0.5 V_{DD}		V
C_L	Output load test LVCMOS				15	pF
I_{OH}/I_{OL}	Output current				±12	mA
T_A	Operating free-air temperature		-40		85	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device supply current	f_{out} = 20 MHz; FS = 0, no SSC		19		mA
		f_{out} = 70 MHz; FS = 1, SSC = 2%		22		
f_{OUT}	Output frequency	FS = 0	8		32	MHz
		FS = 1	32		108	
I_{IH}	LVCMOS input current	V_I = VDD; VDD = 3.6 V			10	µA
I_{IL}	LVCMOS input current	V_I = 0 V; VDD = 3.6 V			–10	µA
V_{OH}	LVCMOS high-level output voltage	I_{OH} = - 0.1mA	2.9			V
		I_{OH} = - 8mA	2.4			
		I_{OH} = - 12mA	2.2			
V_{OL}	LVCMOS low-level output voltage	I_{OL} = 0.1mA			0.1	V
		I_{OL} = 8mA			0.5	
		I_{OL} = 12mA			0.8	
I_{OZ}	High- impedance-state output current	OE = Low	–2		2	µA
$t_{JIT(C-C)}$	Cycle to cycle jitter(1)	f_{out} = 108 MHz; FS = 1, SSC = 1%, 10000 Cycles		110		ps
t_r/t_f	Rise and fall time(1)	20%–80%		0.75		ns
O_{dc}	Output duty cycle		45%		55%	
f_{MOD}	Modulation frequency			30		kHz

(1) Measured with Test Load, see Figure 2.

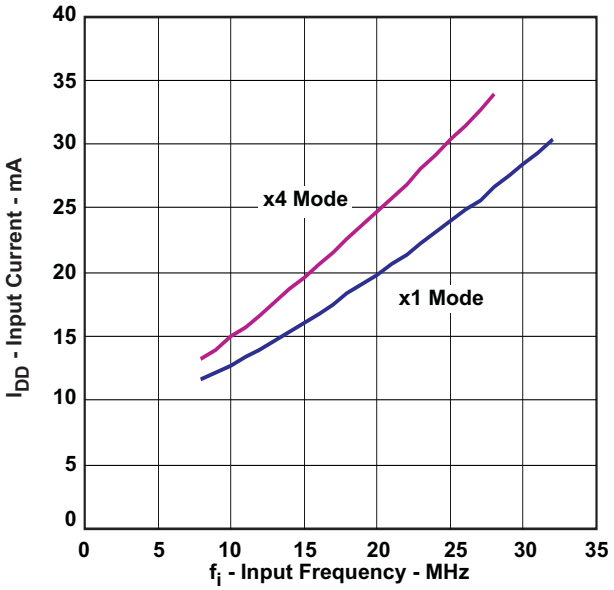


Figure 1. IDD vs Input Frequency, VCC = 3.3V, SSC = 2%, Output Loaded With Test Load

APPLICATION INFORMATION

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS503 uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using one of the below formulas chosen by frequency multiplication mode.

FS = 0: $f_{mod} = f_{IN} / 708$
FS = 1: $f_{mod} = f_{IN} / 620$

PARAMETER MEASUREMENT INFORMATION

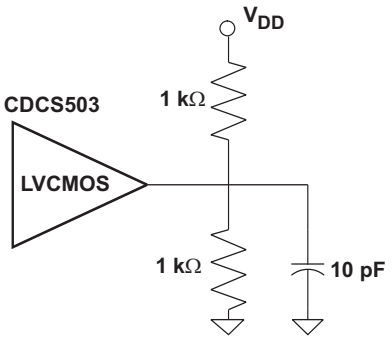


Figure 2. Test Load

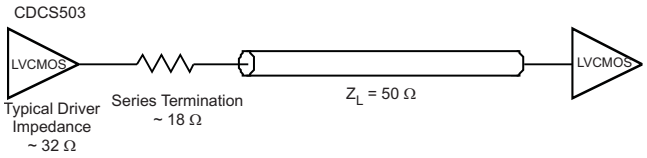
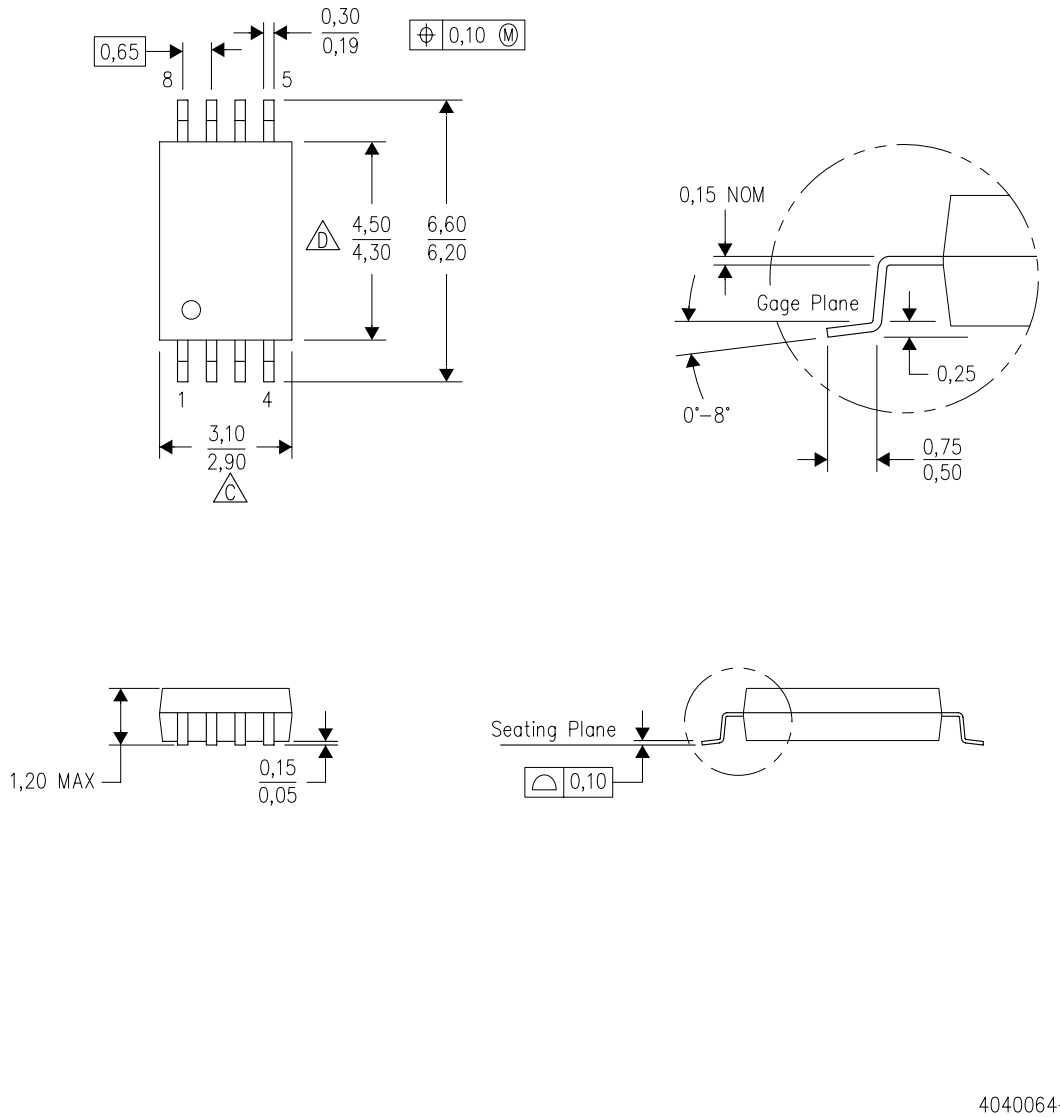


Figure 3. Load for 50-Ω Board Environment

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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