Miniature, 2W, Isolated UNREGULATED DC/DC CONVERTERS

FEATURES

- **Up To 89% Efficiency**
- **Thermal Protection**
- **Device-to-Device Synchronization**
- **SO-28 Power Density of 106W/in^3 (6.5W/cm^3)**
- **EN55022 Class B EMC Performance**
- **UL1950 Recognized Component**
- **JEDEC 14-Pin and SO-28 Packages**

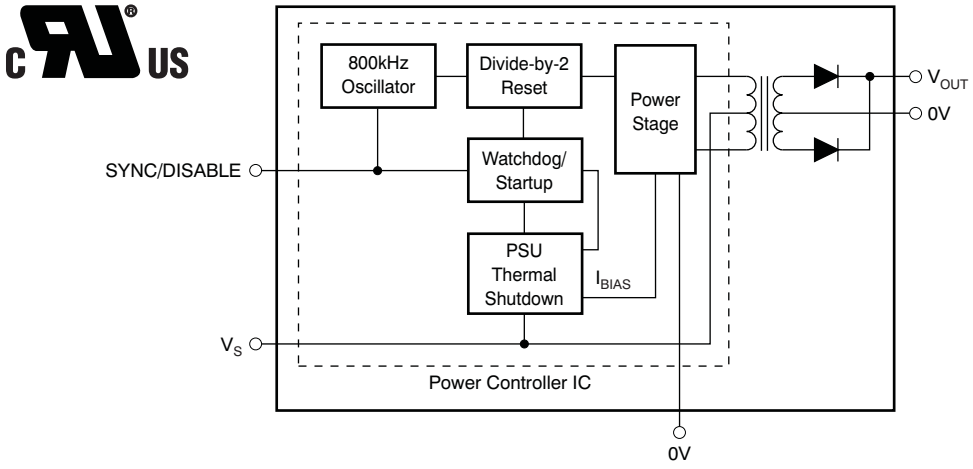
APPLICATIONS

- **Point-of-Use Power Conversion**
- **Ground Loop Elimination**
- **Data Acquisition**
- **Industrial Control and Instrumentation**
- **Test Equipment**

DESCRIPTION

The DCP02 series is a family of 2W, isolated, unregulated DC/DC converters. Requiring a minimum of external components and including on-chip device protection, the DCP02 series provides extra features such as output disable and synchronization of switching frequencies.

The use of a highly integrated package design results in highly reliable products with power densities of 79W/in^3 (4.8W/cm^3) for DIP-14, and 106W/in^3 (6.5W/cm^3) for SO-28. This combination of features and small size makes the DCP02 suitable for a wide range of applications.



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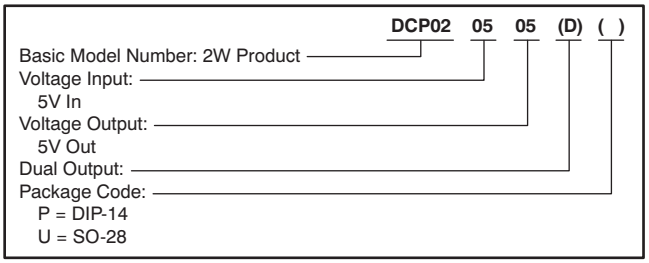
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

Supplemental Ordering Information



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		DCP02 Series	UNIT
Input Voltage	5V input models	7	V
	12V input models	15	V
	15V input models	18	V
	24V input models	29	V
Storage temperature range		–60 to +125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT						
Power	100% full load			2		W
Ripple	Output capacitor = 1µF, 50% load			20		mV_{PP}
Voltage vs. Temperature	Room to cold			0.046		%/°C
	Room to hot			0.016		%/°C
INPUT						
Voltage range on V_S			–10		10	%
ISOLATION						
Voltage	1s Flash test		1			kVrms
	60s test, UL1950(1)		1			kVrms
LINE REGULATION						
Output Voltage	I_O = constant(2)	V_S (min) to V_S (typ)		1	15	%
		V_S (typ) to V_S (max)		1	15	%

(1) During UL1950 recognition tests only.
(2) I_{OUT} ≥ 10% load current

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING/SYNCHRONIZATION					
Oscillator frequency (f_{OSC})	Switching frequency = f_{OSC}/2		800		kHz
Sync input low		0		0.4	V
Sync input current	V_{SYNC} = +2V		75		µA
Disable time			2		µs
Capacitance loading on SYNC pin	External			3(3)	pF
RELIABILITY					
Demonstrated	T_A = +55°C	75			FITS
THERMAL SHUTDOWN					
IC temperature at shutdown			+150		°C
Shutdown current			3		mA
TEMPERATURE RANGE					
Operating		–40		+85	°C

(3) For more information, refer to application report SBAA035, available for download at www.ti.com.

ELECTRICAL CHARACTERISTICS PER DEVICE

At T_A = +25°C, V_S = nominal, C_{IN} = 2.2µF, C_{OUT} = 1.0 µF, unless otherwise noted.

	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)			LOAD REGULATION (%)		NO LOAD CURRENT (mA)	EFFICIENCY (%)	BARRIER CAPACITANCE (pF)
	V_S			V_{NOM} AT V_S (TYP)					I_Q		C_{ISO}
				75% LOAD(1)			10% TO 100% LOAD(2)		0% LOAD	100% LOAD	V_{ISO} = 750Vrms
PRODUCT	MIN	TYP	MAX	MIN	TYP	MAX	TYP	MAX	TYP	TYP	TYP
DCP020503P, U	4.5	5	5.5	3.13	3.3	3.46	19	30	18	74	26
DCP020505P, U	4.5	5	5.5	4.75	5	5.25	14	20	18	80	22
DCP020507P, U	4.5	5	5.5	6.65	7	7.35	14	25	20	81	30
DCP020509P, U	4.5	5	5.5	8.55	9	9.45	12	20	23	82	31
DCP020515DP, U	4.5	5	5.5	±14.25	±15	±15.75	11	20	27	85	24
DCP021205P, U	10.8	12	13.2	4.75	5	5.25	7	15	14	83	33
DCP021212P, U	10.8	12	13.2	11.4	12	12.6	7	20	15	87	47
DCP021212DP, U	10.8	12	13.2	±11.4	±12	±12.6	6	20	16	88	35
DCP021515P, U	13.5	15	16.5	14.25	15	15.75	6	20	15	88	42
DCP022405P	21.6	24	26.4	4.85	5	5.35	6	10	13	81	33
DCP022405U	21.6	24	26.4	4.75	5	5.25	10	15	13	81	33
DCP022405DP, U	21.6	24	26.4	±4.75	±5	+5.25	6	15	12	80	22
DCP022415DP, U	21.6	24	26.4	±14.25	±15	±15.75	6	25	16	79	44

(1) 100% load current = 2W/V_{NOM} (typ)
(2) Load regulation = (V_{OUT} at 10% load - V_{OUT} at 100%)/V_{OUT} at 75% load

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DEVICE INFORMATION

NVA PACKAGE
DIP-14 (Single-DIP)
(Top View)

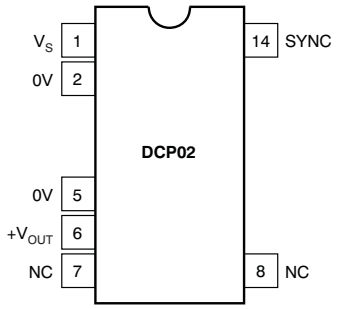

Table 1. Pin Description (Single-DIP)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
NC	7, 8	Not connected
SYNC	14	Synchronization pin

DVB PACKAGE
SO-28 (Single-SO)
(Top View)

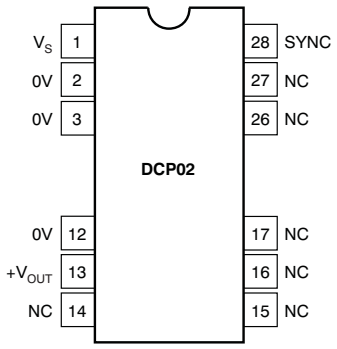

Table 2. TERMINAL FUNCTIONS (Single-SO)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	3	Input side common
0V	12	Output side common
$+V_{OUT}$	13	+Voltage out
NC	14, 15, 16, 17, 26, 27	Not connected
SYNC	28	Synchronization pin

NVA PACKAGE
DIP-14 (Dual-DIP)
(Top View)

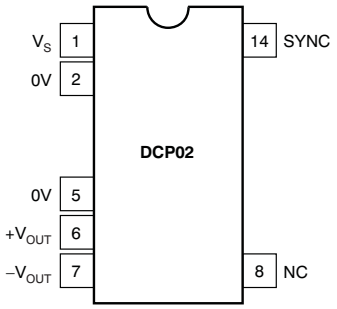

Table 3. TERMINAL FUNCTIONS (Dual-DIP)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
$-V_{OUT}$	7	–Voltage out
NC	8	Not connected
SYNC	14	Synchronization pin

DVB PACKAGE
SO-28 (Dual-SO)
(Top View)

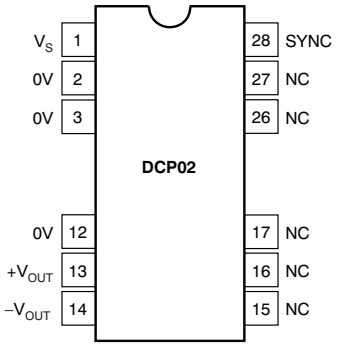

Table 4. TERMINAL FUNCTIONS (Dual-SO)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	3	Input side common
0V	12	Output side common
$+V_{OUT}$	13	+Voltage out
$-V_{OUT}$	14	–Voltage out
NC	15, 16, 17, 26, 27	Not connected
SYNC	28	Synchronization pin

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TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

DCP020505P
CONDUCTED EMISSIONS (500mA Load)

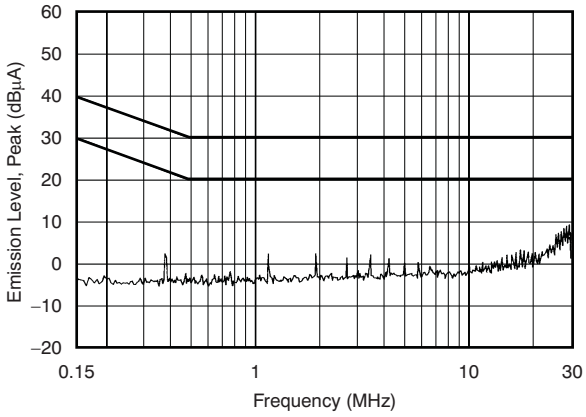

Figure 1.

DCP020505P
V_{OUT} vs TEMPERATURE (75% Load)

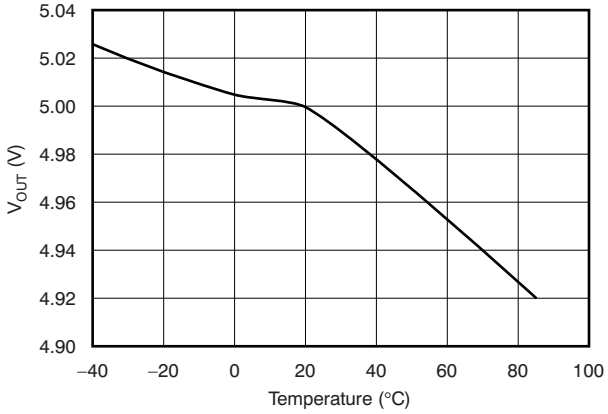

Figure 2.

DCP021205P
V_{OUT} vs LOAD

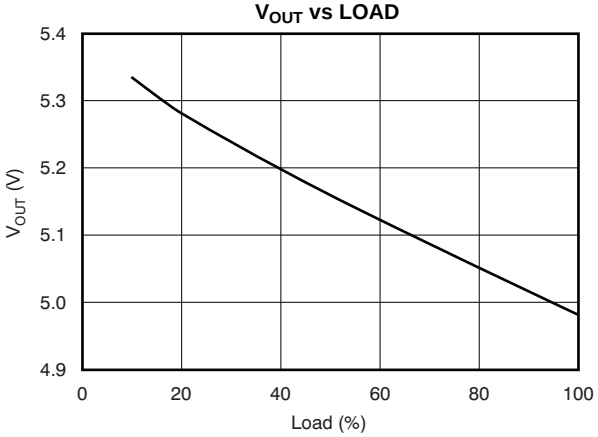

Figure 3.

DCP021205P
POWER OUT vs TEMPERATURE (400mA Load)

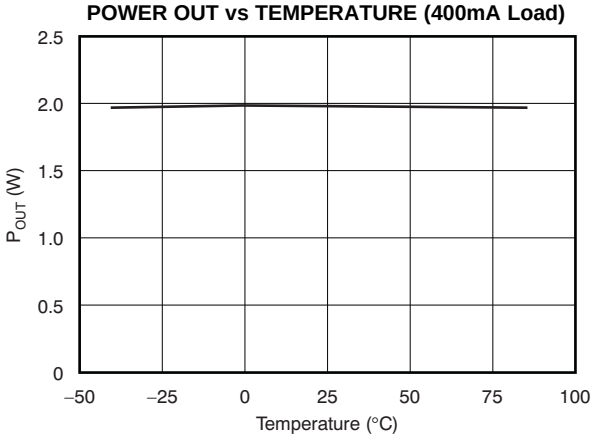

Figure 4.

DCP0212
EFFICIENCY vs LOAD

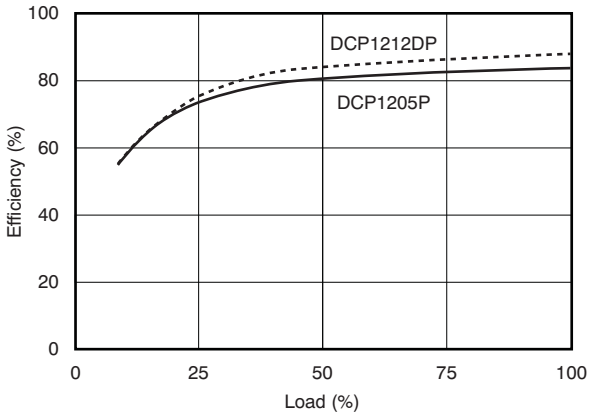

Figure 5.

DCP020505P
OUTPUT AC RIPPLE (20MHz Band)

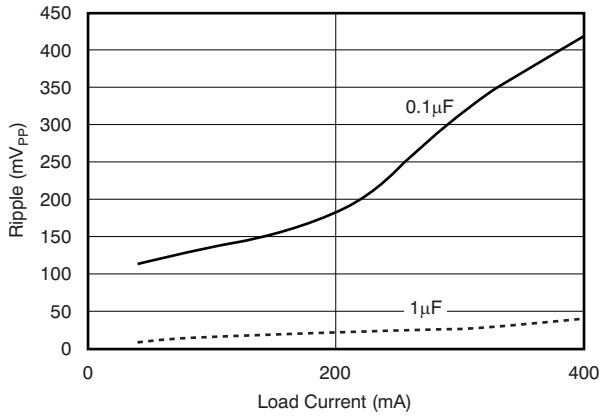

Figure 6.

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FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP02 offers up to 2W of unregulated output power from a 5V, 12V, 15V, or 24V input source with a typical efficiency of up to 89%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design uses an advanced BiCMOS/DMOS process.

POWER STAGE

The DCP02 uses a push-pull, center-tapped topology switching at 400kHz (divide-by-2 from an 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCP02 circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the SYNC pin low. The output pins will be tri-stated, which occurs in 2µs.

THERMAL SHUTDOWN

The DCP02 is protected by a thermal-shutdown circuit. If the on-chip temperature exceeds +150°C, the device will shut down. Once the temperature falls below +150°C, normal operation resumes.

SYNCHRONIZATION

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCP02 overcomes this interference by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, taking care to minimize the capacitance of tracking. Stray capacitance (> 10pF) has the effect of reducing the switching frequency, or even stopping the oscillator circuit. It is also recommended that power and ground lines be star-connected.

It should be noted that if synchronized devices are used at start up, all devices will draw maximum current simultaneously. This configuration can cause the input voltage to dip; if it dips below the minimum input voltage (4.5V), the devices may not start up. A 2.2µF capacitor should be connected close to the input pins.

If more than eight devices are to be synchronized, it is recommended that the SYNC pins be driven by an external device. Details are contained in Application Report SBAA035, External Synchronization of the DCP01/02 Series of DC/DC Converters, available for download from www.ti.com.

CONSTRUCTION

The basic construction of the DCP02 is the same as standard ICs; there is no substrate within the molded package. The DCP02 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Since there is no solder within the package, the DCP02 does not require any special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

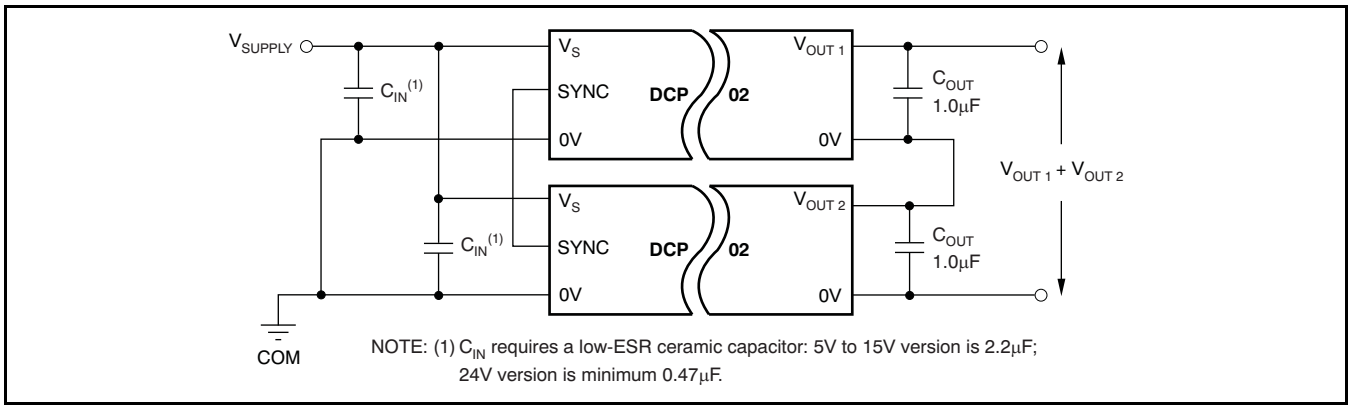

Figure 7. Connecting the DCP02 in Series

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ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP02 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled low, the DCP02 will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2µs. Removal of the pull down causes the DCP02 to be enabled.

Capacitive loading on the SYNC pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

The high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that a 1µF capacitor be used on V_{OUT}. Dual outputs should both be decoupled to pin 5. A 2.2µF capacitor on the input is also recommended.

Connecting the DCP02 in Series

Multiple DCP02 isolated 2W DC/DC converters can be connected in series to provide nonstandard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCP02.

Connect the positive V_{OUT} from one DCP02 to the negative V_{OUT} (0V) of another (see Figure 7). If the SYNC pins are tied together, the self-synchronization feature of the DCP02 prevents beat frequencies on the voltage rails. The SYNC feature of the DCP02 allows easy series connection without external filtering, thus minimizing cost.

The outputs on the dual-output DCP02 versions can also be connected in series to provide two times the magnitude of V_{OUT}, as shown in Figure 8. For example, a dual 15V DCP022415D could be connected to provide a 30V rail.

Connecting the DCP02 in Parallel

If the output power from one DCP02 is not sufficient, it is possible to parallel the outputs of multiple DCP02s, as shown in Figure 9. Again, the SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

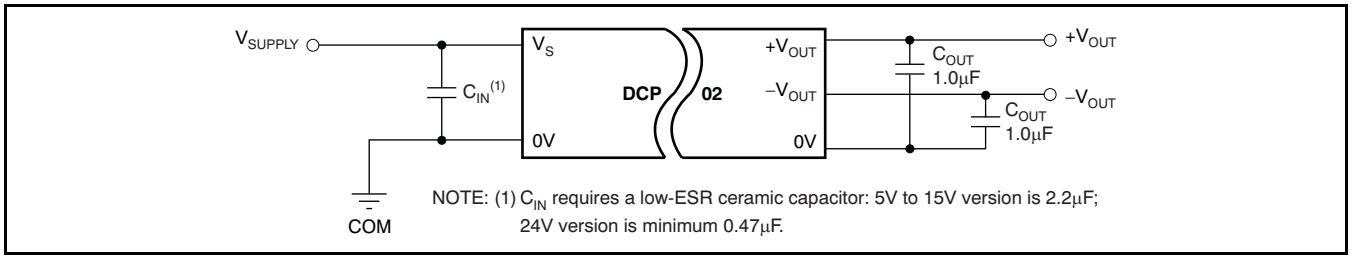

Figure 8. Connecting Dual Outputs in Series

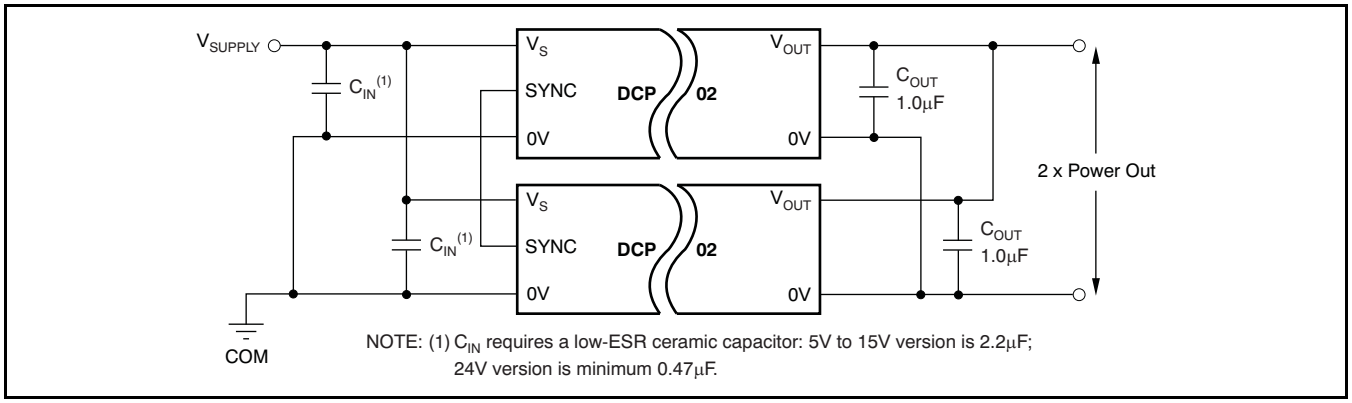

Figure 9. Connecting Multiple DCP02s in Parallel

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APPLICATION INFORMATION

The DCP01B, DCV01, and DCP02 are three families of miniature DC/DC converters providing an isolated unregulated voltage output. All are fabricated using a CMOS/DMOS process with the DCP01B replacing the familiar DCP01 family that was fabricated from a bipolar process. The DCP02 is essentially an extension of the DCP01B family, providing a higher power output with a significantly improved load regulation. The DCV01 is tested to a higher isolation voltage.

TRANSFORMER DRIVE CIRCUIT

Transformer drive transistors have a characteristically low value of transistor *on* resistance (R_{DS}); thus, more power is transferred to the transformer. The transformer drive circuit is limited by the base current available to switch on the power transistors driving the transformer and the characteristic current gain (beta), resulting in a slower turn-on time. Consequently, more power is dissipated within the transistor, resulting in a lower overall efficiency, particularly at higher output load currents.

SELF-SYNCHRONIZATION

The input synchronizations facility ($SYNC_{IN}$) allows for easy synchronizing of multiple devices. If two to eight devices (maximum) have their respective $SYNC_{IN}$ pins connected together, then all devices will be synchronized.

Each device has its own onboard oscillator. This oscillator is generated by charging a capacitor from a constant current and producing a ramp. When this ramp passes a threshold, an internal switch is activated that discharges the capacitor to a second threshold before the cycle is repeated.

When several devices are connected together, all the internal capacitors are charged simultaneously.

When one device passes its threshold during the charge cycle, it starts the discharge cycle. All the other devices sense this falling voltage and, likewise, initiate a discharge cycle so that all devices discharge together. A subsequent charge cycle is only restarted when the last device has finished its discharge cycle.

OPTIMIZING PERFORMANCE

Optimum performance can only be achieved if the device is correctly supported. The very nature of a switching converter requires power to be instantly available when it switches on. If the converter has DMOS switching transistors, the fast edges will create a high current demand on the input supply. This transient load placed on the input is supplied by the external input decoupling capacitor, thus maintaining the input voltage. Therefore, the input supply does not see this transient (this is an analogy to high-speed digital circuits). The positioning of the capacitor is critical and must be placed as close as possible to the input pins and connected via a low-impedance path.

The optimum performance primarily depends on two factors:

1. Connection of the input and output circuits for minimal loss.
2. The ability of the decoupling capacitors to maintain the input and output voltages at a constant level.

PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes (tracks) where possible. If that is not possible, use wide tracks to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the track must be deployed; devices must not be connected in series, as this will cascade the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See the PCB Layout section for more details.

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Decoupling Ceramic Capacitors

All capacitors have losses because of internal equivalent series resistance (ESR), and to a lesser degree, equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of frequency versus capacitor impedance. These graphs typically show the capacitor impedance falling as frequency is increased (as shown in Figure 10). As the frequency increases, the impedance stops decreasing and begins to rise. The point of minimum impedance indicates the resonant frequency of the capacitor. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.

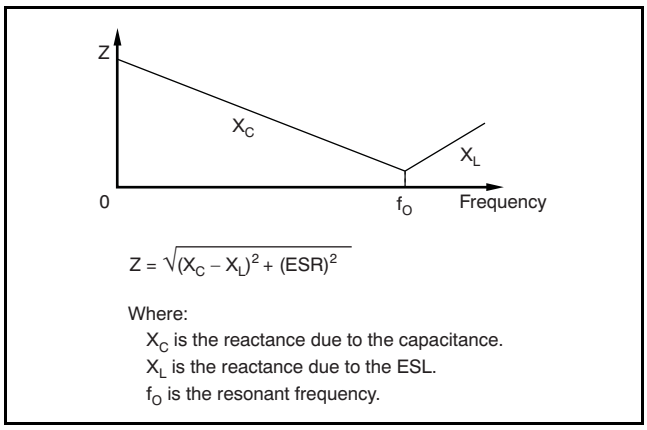

Figure 10. Capacitor Impedance vs Frequency

At f_O, $X_C = X_L$; however, there is a 180° phase difference resulting in cancellation of the imaginary component. The resulting effect is that the impedance at the resonant point is the real part of the complex impedance; namely, the value of the ESR. The resonant frequency must be well above the 800kHz switching frequency of the DCP and DCVs.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current, as shown:

$$V_{IN} = V_{PK} - (ESR \times I_{TR}) \quad (1)$$

Where:

V_{IN} is the voltage at the device input.

V_{PK} is the maximum value of the voltage on the capacitor during charge.

I_{TR} is the transient load current.

The other factor that affects the performance is the value of the capacitance. However, for the input and the full wave outputs (single-output voltage devices), ESR is the dominant factor.

Input Capacitor and the Effects of ESR

If the input decoupling capacitor is not ceramic with <20mΩ ESR, then at the instant the power transistors switch on, the voltage at the input pins falls momentarily. Should the voltage fall below approximately 4V, the DCP detects an under-voltage condition and switches the DCP drive circuits to the off state. This detection is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. A slow-down or stoppage would result in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value. Then the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process is repeated until the capacitor is charged sufficiently to start the device correctly. Otherwise, the device will be caught up in a loop.

Normal startup should occur in approximately 1ms from power being applied to the device. If a considerably longer startup duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5V to 15V input devices, a 2.2µF low-ESR ceramic capacitor ensures a good startup performance. For the remaining input voltage ranges, 0.47µF ceramic capacitors are recommended. Tantalum capacitors are not recommended, since most do not have low-ESR values and will degrade performance. If tantalum capacitors must be used, close attention must be paid to both the ESR and voltage as derated by the vendor.

Output Ripple Calculation Example

DCP020505: Output voltage 5V, Output current 0.4A. At full output power, the load resistor is 12.5Ω. Output capacitor of 1µF, ESR of 0.1Ω. Capacitor discharge time 1% of 800kHz (ripple frequency):

$t_{DIS} = 0.0125\mu s$

$\tau = C \times R_{LOAD}$

$\tau = 1 \times 10^{-6} \times 12.5 = 12.5\mu s$

$V_{DIS} = V_O(1 - EXP(-t_{DIS}/\tau))$

$V_{DIS} = 5mV$

By contrast, the voltage dropped because of ESR:

$V_{ESR} = I_{LOAD} \times ESR$

$V_{ESR} = 40mV$

Ripple voltage = 45mV

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Clearly, increasing the capacitance has a much smaller effect on the output ripple voltage than does reducing the value of the ESR for the filter capacitor.

DUAL OUTPUT VOLTAGE DCP AND DCVs

The voltage output for the dual DCPs is half wave rectified; therefore, the discharge time is 1.25µs. Repeating the above calculations using the 100% load resistance of 25Ω (0.2A per output), the results are:

τ = 25µs

t_{DIS} = 1.25µs

V_{DIS} = 244mV

V_{ESR} = 20mV

Ripple Voltage = 266mV

This time, it is the capacitor discharging that contributes to the largest component of ripple. Changing the output filter to 10µF, and repeating the calculations, the result is:

Ripple Voltage = 45mV.

This value is composed of almost equal components.

The previous calculations are given only as a guide. Capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

PCB LAYOUT

Figure 11 and Figure 12 illustrate a printed circuit board (PCB) layout for the two conventional (DCP01/02, DCV01), and two SO-28 surface-mount packages (DCP02U). Figure 13 shows the schematic.

Input power and ground planes have been used, providing a low-impedance path for the input power. For the output, the common or 0V has been connected via a ground plane, while the connections for the positive and negative voltage outputs are conducted via wide traces in order to minimize losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

The $SYNC_{IN}$ pin, when not being used, is best left as a floating pad. A ground ring or annulus connected around the pin prevents noise being conducted onto the pin. If the $SYNC_{IN}$ pin is to be connected to one or more $SYNC_{IN}$ pins, then the linking trace should be narrow and must be kept short in length. In addition, no other trace should be in close proximity to this trace because that will increase the stray capacitance on this pin. In turn, the stray capacitance affects the performance of the oscillator.

Ripple and Noise

Careful consideration should be given to the layout of the PCB in order to obtain the best results.

The DCP02 is a switching power supply, and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to connect the power to the input of DCP02. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

If the $SYNC_{IN}$ pin is being used, then the trace connection between device $SYNC_{IN}$ pins should be short to avoid stray capacitance. If the $SYNC_{IN}$ pin is not being used, it is advisable to place a guard ring (connected to input ground) around this pin to avoid any noise pick up.

The output should be taken from the device using ground and power planes, thereby ensuring minimum losses.

A good quality, low-ESR ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensures a smooth startup.

A good quality. low-ESR capacitor (ceramic preferred) placed as close as practical across the rectifier output terminal and output ground gives the best ripple and noise performance. See Application Bulletin SBVA012, DC-to-DC Converter Noise Reduction, for more information on noise rejection.

THERMAL MANAGEMENT

Due to the high power density of this device, it is advisable to provide ground planes on the input and output.

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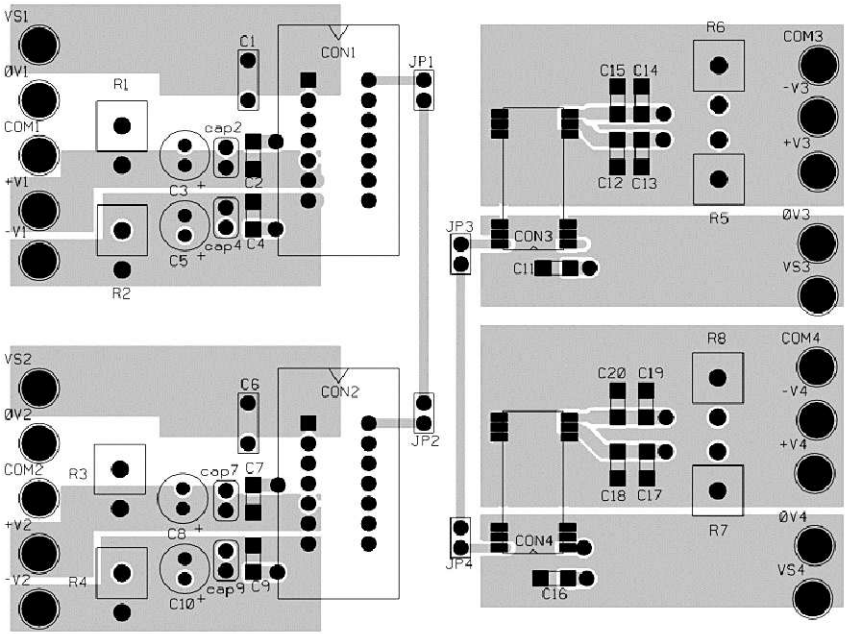


Figure 11. Example of PCB Layout, Component-Side View

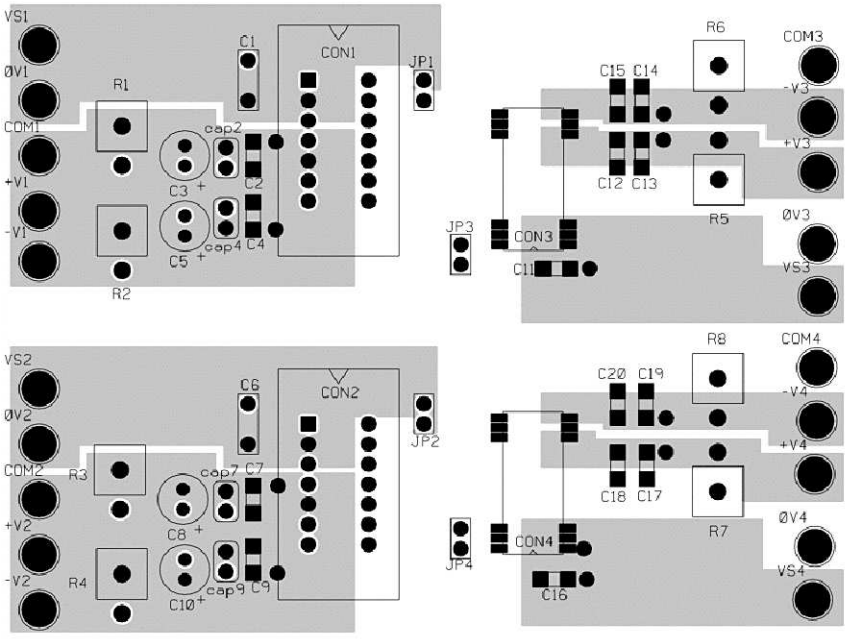
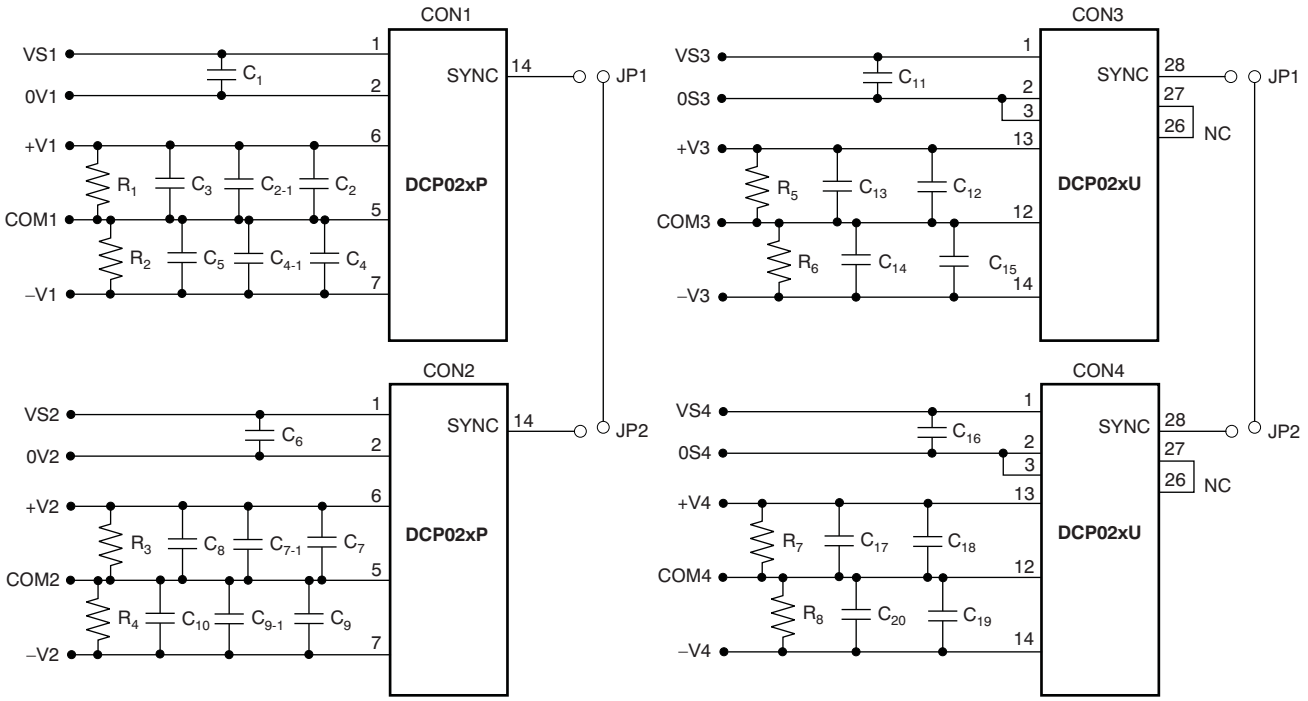


Figure 12. Example of PCB Layout, Non-Component-Side View



(1) Capacitors C_{2-1}, C_{4-1}, C_{7-1}, and C_{9-1} are through-hole plated components connected in parallel with C_2, C_4, C_7, and C_9 (1206 SMD), respectively.
(2) For optimum low-noise performance, use low-ESR capacitors.
(3) Do not connect the SYNC pin jumper (JP1–JP4) if the SYNC function is not being used.
(4) Connections to the power input should be made with a minimum wire of 16/0.2 twisted pair, with the length kept short.
(5) VSx and 0Vx are input supply and ground respectively (x represents the channel).
(6) +Vx and –Vx are the positive and negative outputs, referenced to a common ground COMx.
(7) JPx are the links used for self-synchronization; if this facility is not being used, the links should be unconnected.
(8) R1–R8 are the power output loads; do not fit these if an external load is connected.
(9) CON1 and CON2 are DIL-14; CON3 and CON4 are SO-28 packages.
(10) NC = not connected.

Figure 13. Example of PCB Layout, Schematic Diagram

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP020503P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP020503P	Samples
DCP020503U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020503U	Samples
DCP020505P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP020505P	Samples
DCP020505U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020505U	Samples
DCP020505U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020505U	Samples
DCP020505U/1KE4	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020505U	Samples
DCP020505UE4	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020505U	Samples
DCP020507P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP020507P	Samples
DCP020507U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020507U	Samples
DCP020507U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020507U	Samples
DCP020509P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP020509P	Samples
DCP020509U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020509U	Samples
DCP020509U/1K	OBSOLETE	SOP	DVB	12		TBD	Call TI	Call TI			
DCP020515DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP020515DP	Samples
DCP020515DU	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020515DU	Samples
DCP020515DU/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP020515DU	Samples
DCP021205P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP021205P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP021205PE4	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP021205P	Samples
DCP021205U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021205U	Samples
DCP021205U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021205U	Samples
DCP021212DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP021212DP	Samples
DCP021212DU	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021212DU	Samples
DCP021212DU/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021212DU	Samples
DCP021212P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP021212P	Samples
DCP021212U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021212U	Samples
DCP021212U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021212U	Samples
DCP021515P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP021515P	Samples
DCP021515PE4	ACTIVE	PDIP	NVA	7		TBD	Call TI	Call TI			Samples
DCP021515U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021515U	Samples
DCP021515U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP021515U	Samples
DCP022405DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP022405DP	Samples
DCP022405DU	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP022405DU	Samples
DCP022405P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP022405P	Samples
DCP022405U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP022405U	Samples
DCP022415DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		DCP022415DP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP022415DU	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP022415DU	Samples
DCP022415DU/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR		DCP022415DU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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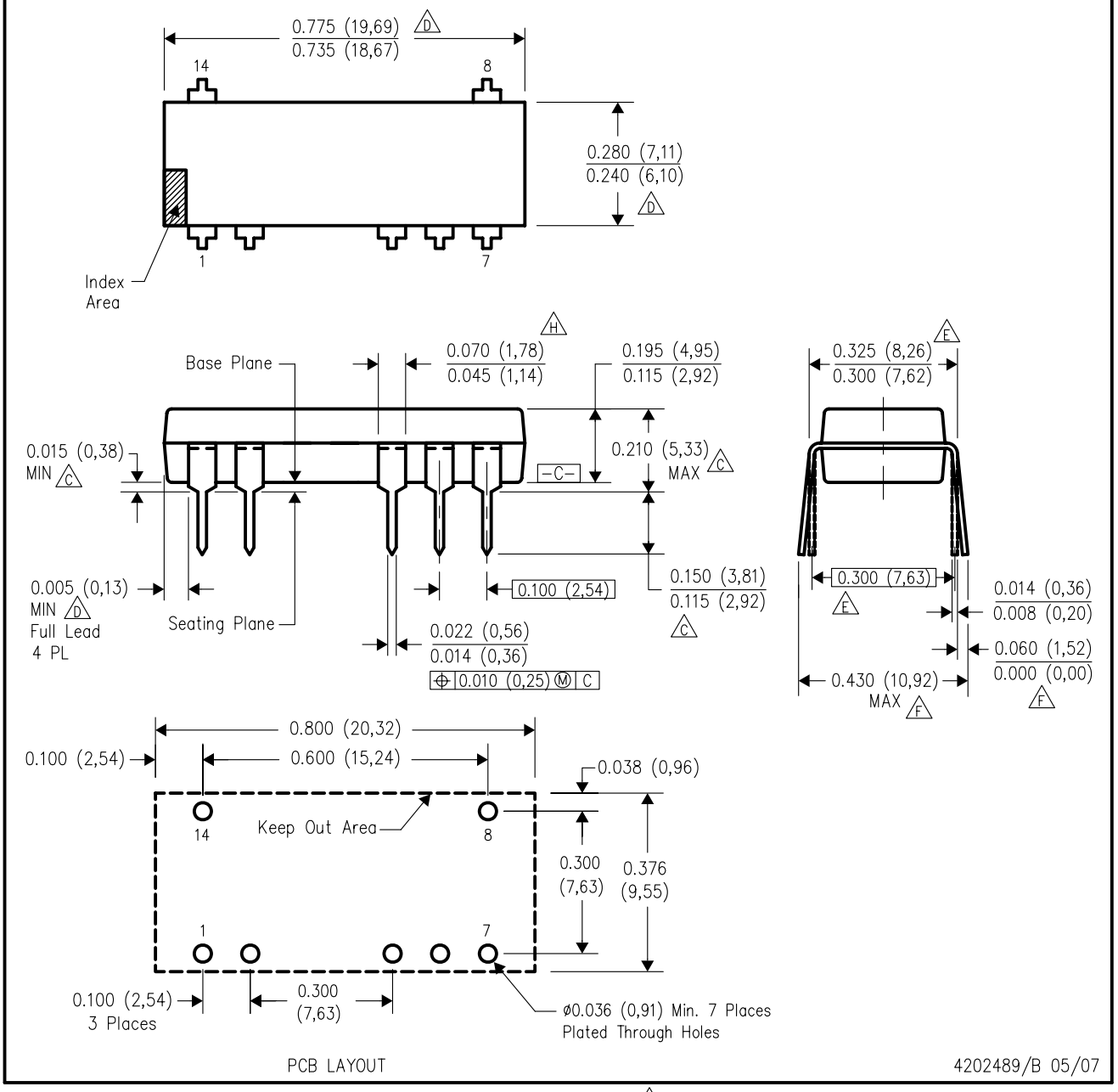
NVA (R–PDIP–T7/14) PLASTIC DUAL–IN–LINE



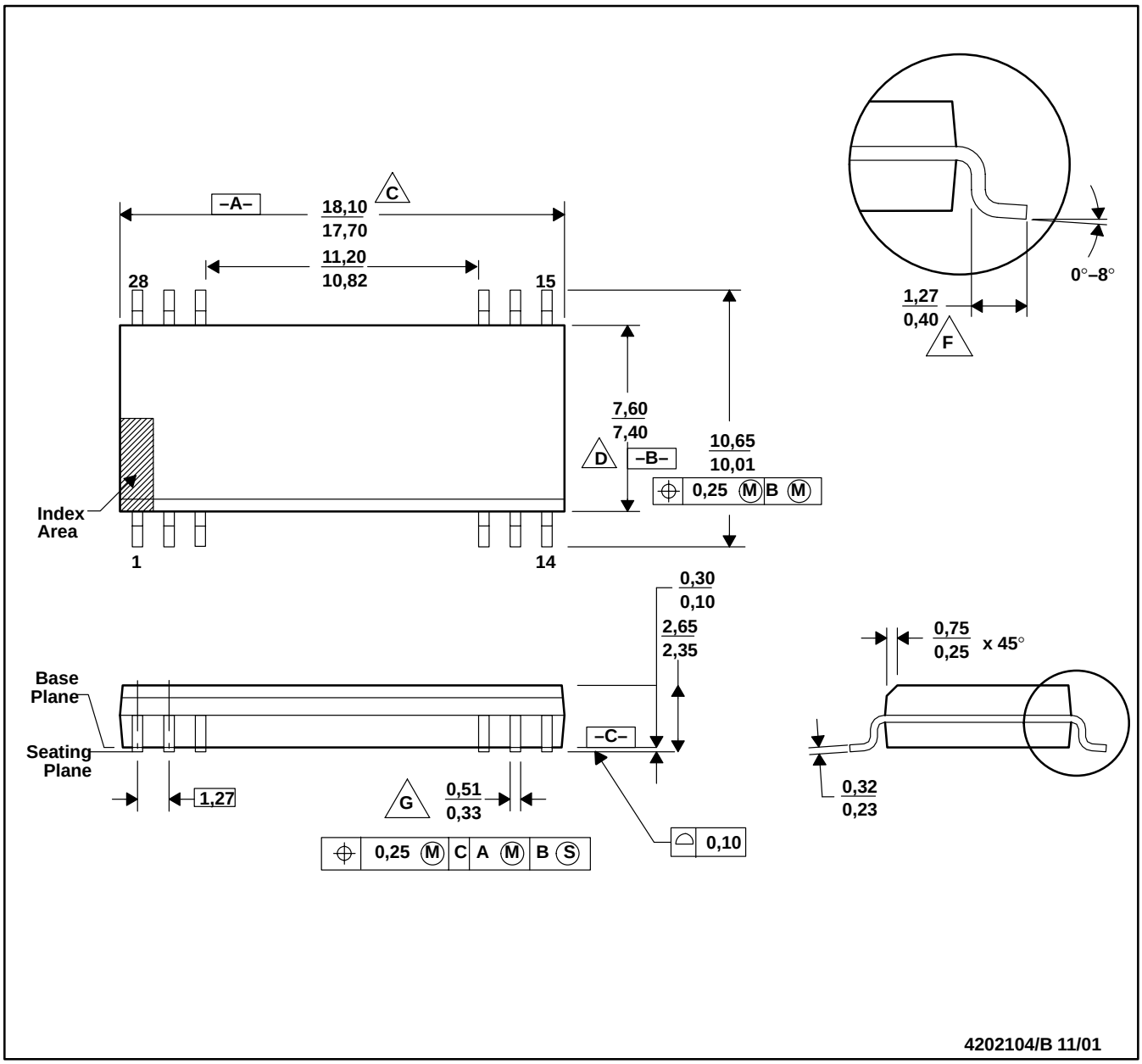
PCB LAYOUT

4202489/B 05/07

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS–3.
- D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
- F. Dimensions are measured at the lead tips with the leads unconstrained.
- G. Pointed or rounded lead tips are preferred to ease insertion.
- H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
- I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- J. A visual index feature must be located within the cross–hatched area.
- K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- L. Falls within JEDEC MS–001–AA.

MPDS106A – AUGUST 2001 – REVISED NOVEMBER 2001

DVB(R-PDSO-G12/28) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.
D. Body width dimension does not include inter-lead flash or portrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.
H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.
I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

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