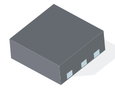


PRECISION ADJUSTABLE CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES

Check for Samples: TPS2556, TPS2557

FEATURES

- **Meets USB Current-Limiting Requirements**
- **Adjustable Current Limit, 500 mA–5 A (typ)**
- **+/- 6.5% Current-Limit Accuracy at 4.5 A**
- **Fast Overcurrent Response - 3.5-μS (typ)**
- **22-mΩ High-Side MOSFET**
- **Operating Range: 2.5 V to 6.5 V**
- **2-μA Maximum Standby Supply Current**
- **Built-in Soft-Start**
- **15 kV / 8 kV System-Level ESD Capable**
- **UL Listed* – File No. E169910**
- **CB & Nemko Certification***
- ***R_{ILIM} ≥ 24.9 kΩ (5A maximum)**

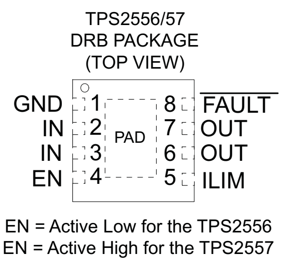
APPLICATIONS

- **USB Ports/Hubs**
- **Digital TV**
- **Set-Top Boxes**
- **VOIP Phones**

DESCRIPTION

The TPS2556/57 power-distribution switches are intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered. These devices offer a programmable current-limit threshold between 500 mA and 5.0 A (typ) via an external resistor. The power-switch rise and fall times are controlled to minimize current surges during turn on/off.

TPS2556/57 devices limit the output current to a safe level by switching into a constant-current mode when the output load exceeds the current-limit threshold. The FAULT logic output asserts low during overcurrent and over temperature conditions.



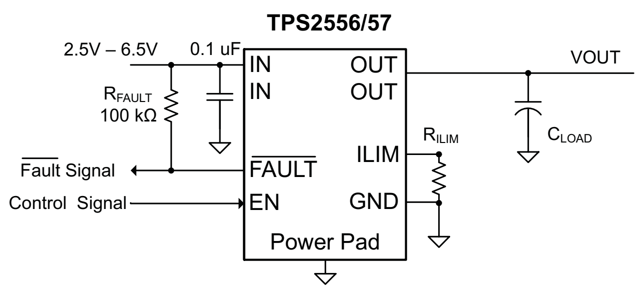


Figure 1. Typical Application as USB Power Switch

GENERAL SWITCH CATALOG						
33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA 0.2 A - 2 A TPS202x 0.2 A - 2 A TPS203x 0.2 A - 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS AND ORDERING INFORMATION

DEVICE(1)	AMBIENT TEMPERATURE (2)	ENABLE	SON (3) (DRB)	MARKING	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT
TPS2556	–40°C to 85°C	Active low	TPS2556DRB	2556	5.0 A
TPS2557		Active high	TPS2557DRB	2557	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Maximum ambient temperature is a function of device junction temperature and system level considerations, such as power dissipation and board layout. See *dissipation rating table* and *recommended operating conditions* for specific information related to these devices.
(3) Add an R suffix to the device type for tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			VALUE	UNIT
	Voltage range on IN, OUT, EN or $\overline{EN}$, ILIM, $\overline{FAULT}$		–0.3 to 7	V
	Voltage range from IN to OUT		–7 to 7	V
I	Continuous output current		Internally Limited	
	Continuous total power dissipation		See the Dissipation Rating Table	
	Continuous $\overline{FAULT}$ sink current		25	mA
	ILIM source current		Internally Limited	mA
	ESD	HBM	2	kV
		CDM	500	V
	ESD – system level (contact/air)(3)		8/15	kV
T_J	Maximum junction temperature		–40 to OTSD2(4)	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.
(3) Surges per EN61000-4-2, 1999 applied between USB and output ground of the TPS2556EVM (HPA423) evaluation module (documentation available on the Web.) These were the test levels, not the failure threshold.
(4) Ambient over temperature shutdown threshold

DISSIPATION RATING TABLE

BOARD	PACKAGE	THERMAL RESISTANCE(1) θ_{JA}	THERMAL RESISTANCE θ_{JC}	$T_A \leq 25°C$ POWER RATING
High-K(2)	DRB	41.6 °C/W	10.7 °C/W	2403 mW

(1) Mounting per the *PowerPAD™ Thermally Enhanced Package* application report (SLMA002).
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage, IN		2.5	6.5	V
V_{EN}	Enable voltage	TPS2556	0	6.5	V
$V_{/EN}$		TPS2557	0	6.5	
V_{IH}	High-level input voltage on EN or $\overline{EN}$		1.1		V
V_{IL}	Low-level input voltage on EN or $\overline{EN}$			0.66	
I_{OUT}	Continuous output current, OUT		0	5	A
	Continuous $\overline{FAULT}$ sink current		0	10	mA
T_J	Operating virtual junction temperature		–40	125	°C
R_{ILIM}	Recommended resistor limit range		20k	187k	Ω

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $V_{/EN}$ = 0 V, or V_{EN} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance	T_J = 25°C			22	25	mΩ
		–40 °C ≤ T_J ≤ 125°C				35	
t_r	Rise time, output	V_{IN} = 6.5 V	C_L = 1 μF, R_L = 100 Ω, (see Figure 2)	2	3	4	ms
		V_{IN} = 2.5 V		1	2	3	
t_f	Fall time, output	V_{IN} = 6.5 V		0.6	0.8	1.0	
		V_{IN} = 2.5 V		0.4	0.6	0.8	
ENABLE INPUT EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.66		1.1	V
	Hysteresis				55(2)		mV
I_{EN}	Input current	V_{EN} = 0 V or 6.5 V, $V_{/EN}$ = 0 V or 6.5 V		–0.5		0.5	μA
t_{on}	Turn-on time	C_L = 1 μF, R_L = 100 Ω, (see Figure 2)				9	ms
t_{off}	Turn-off time					6	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold (Maximum DC output current I_{OUT} delivered to load) & Short-circuit current, OUT connected to GND	R_{ILIM} = 24.9 kΩ		4130	4450	4695	mA
		R_{ILIM} = 61.9 kΩ		1590	1785	1960	
		R_{ILIM} = 100 kΩ		935	1100	1260	
t_{IOS}	Response time to short circuit	V_{IN} = 5.0 V (see Figure 3)			3.5(2)		μs

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) These parameters are provided for reference only, and do no constitute part of TI's published specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, $V_{/EN}$ = 0 V, or V_{EN} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{IN_off}	Supply current, low-level output	V_{IN} = 6.5 V, No load on OUT, $V_{\overline{EN}}$ = 6.5 V or V_{EN} = 0 V			0.1	2.0	μA
I_{IN_on}	Supply current, high-level output	V_{IN} = 6.5 V, No load on OUT	R_{ILIM} = 24.9 kΩ		95	120	μA
			R_{ILIM} = 100 kΩ		85	110	μA
I_{REV}	Reverse leakage current	V_{OUT} = 6.5 V, V_{IN} = 0 V	T_J = 25 °C		0.01	1	μA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.35	2.45	V
	Hysteresis, IN				35(3)		mV
$\overline{FAULT}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULT}$	$I_{/FAULT}$ = 1 mA				180	mV
	Off-state leakage	$V_{/FAULT}$ = 6.5 V				1	μA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to overcurrent condition		6	9	13	ms
THERMAL SHUTDOWN							
OTSD2	Thermal shutdown threshold			155			°C
OTSD	Thermal shutdown threshold in current-limit			135			°C
	Hysteresis				20(3)		°C

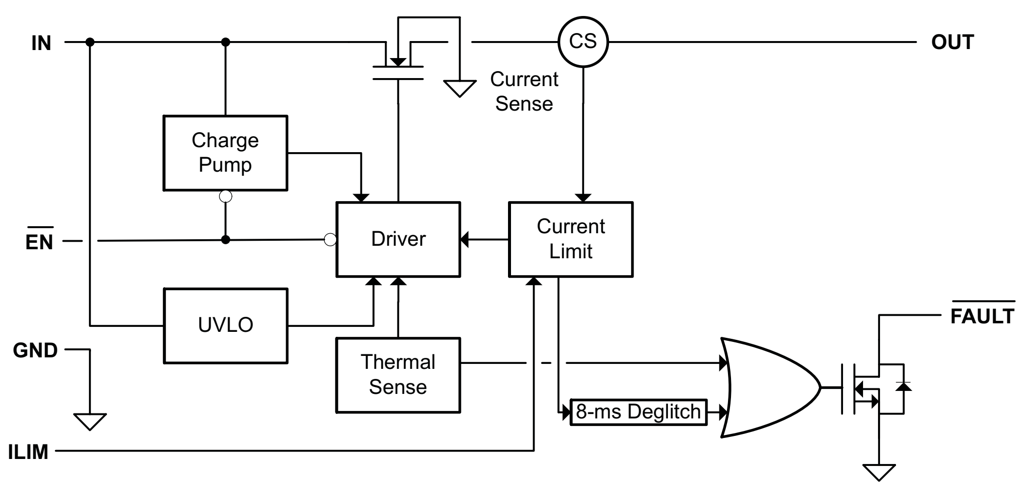
(3) These parameters are provided for reference only, and do no constitute part of TI's published specifications for purposes of TI's product warranty.

DEVICE INFORMATION

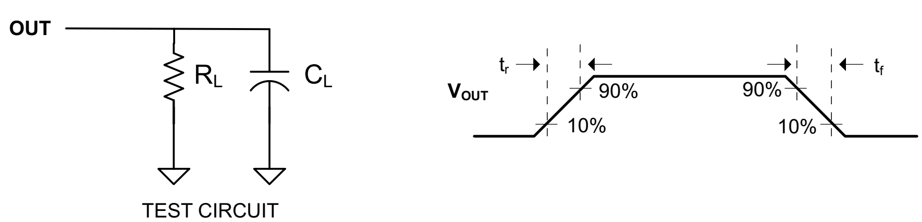
Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS2556	TPS2557		
$\overline{EN}$	4	–	I	Enable input, logic low turns on power switch
EN	–	4	I	Enable input, logic high turns on power switch
GND	1	1		Ground connection; connect externally to PowerPAD
IN	2, 3	2, 3	I	Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{FAULT}$	8	8	O	Active-low open-drain output, asserted during overcurrent or overtemperature conditions.
OUT	6, 7	6, 7	O	Power-switch output
ILIM	5	5	O	External resistor used to set current-limit threshold; recommended 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ.
PowerPAD™	–	–		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



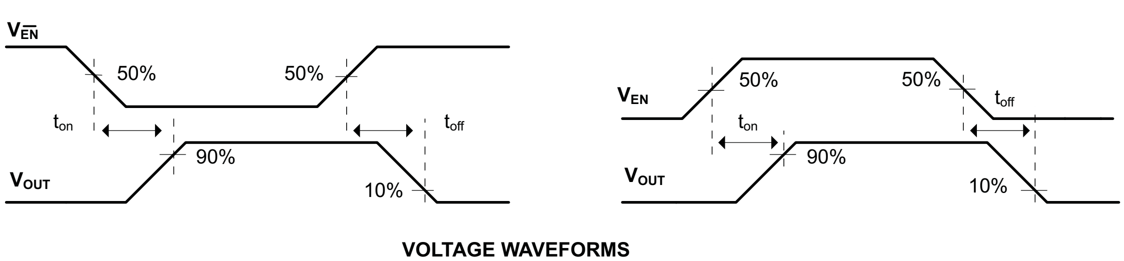


Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

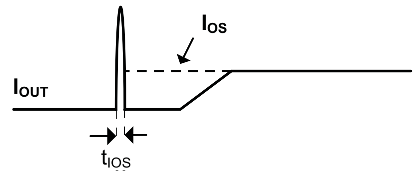


Figure 3. Response Time to Short Circuit Waveform

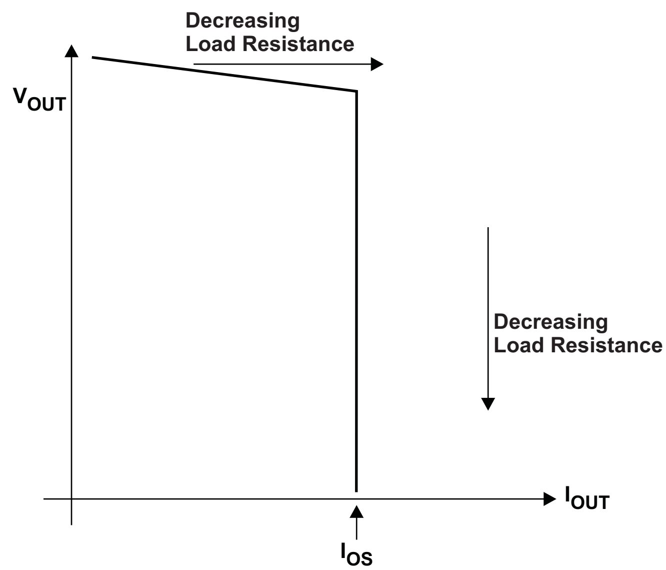


Figure 4. Output Voltage vs. Current-Limit Threshold

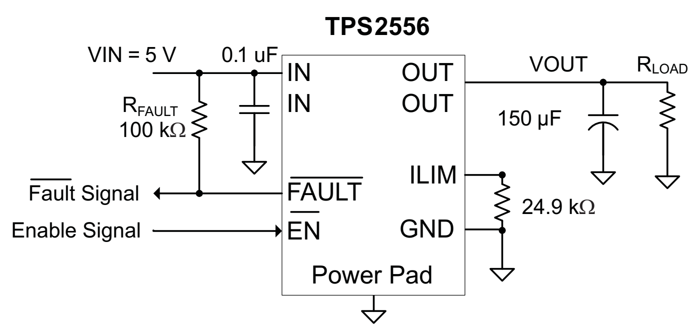


Figure 5. Typical Characteristics Reference Schematic

TYPICAL CHARACTERISTICS

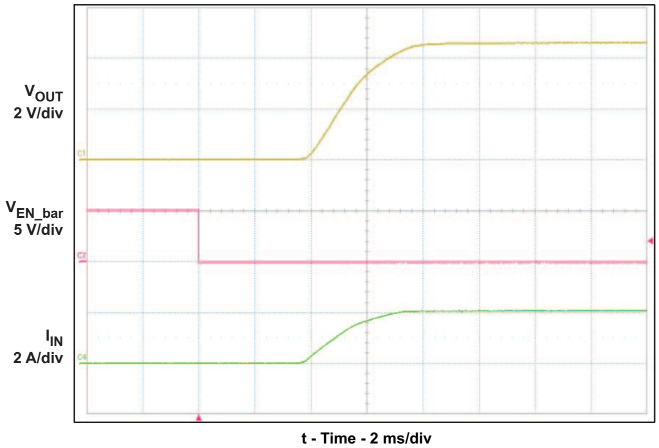


Figure 6. Turn-on Delay and Rise Time

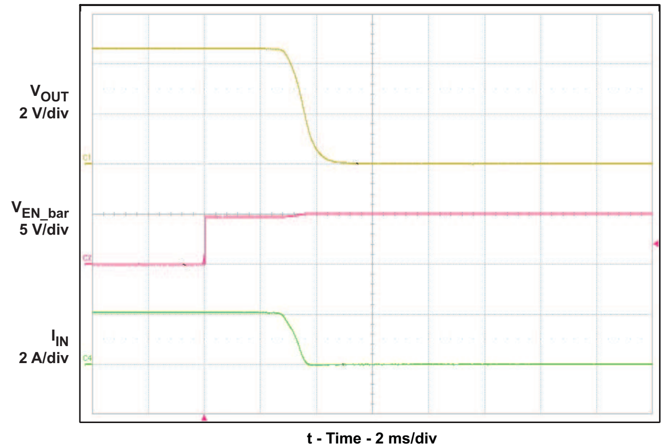


Figure 7. Turn-off Delay and Fall Time

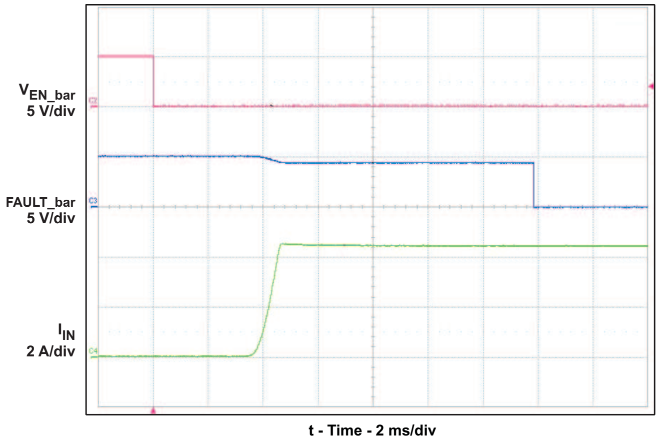


Figure 8. Device Enabled into Short-Circuit

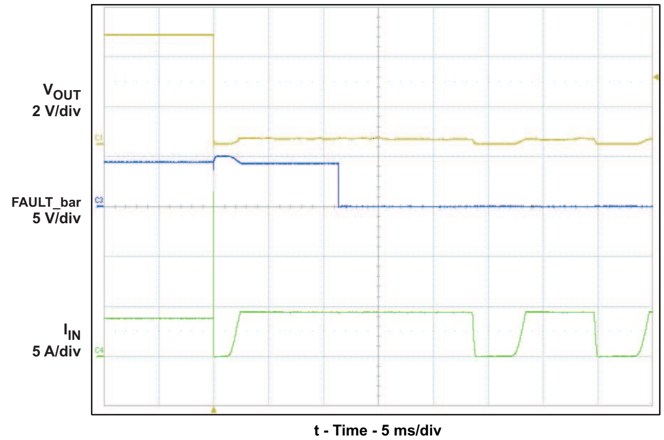


Figure 9. Full-Load to Short-Circuit Transient Response

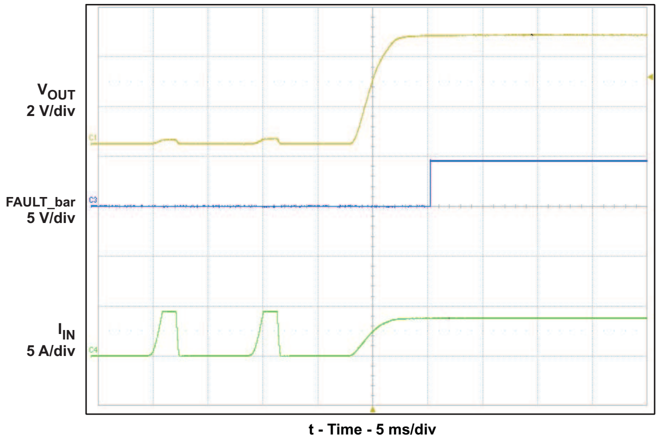


Figure 10. Short-Circuit to Full-Load Recovery Response

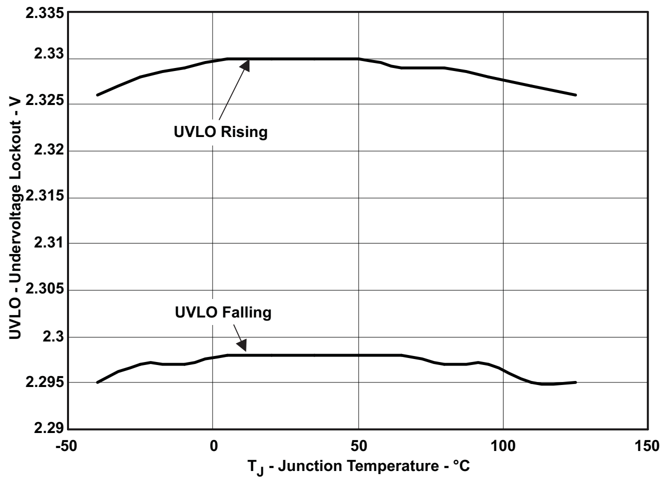


Figure 11. UVLO – Undervoltage Lockout – V

TYPICAL CHARACTERISTICS (continued)

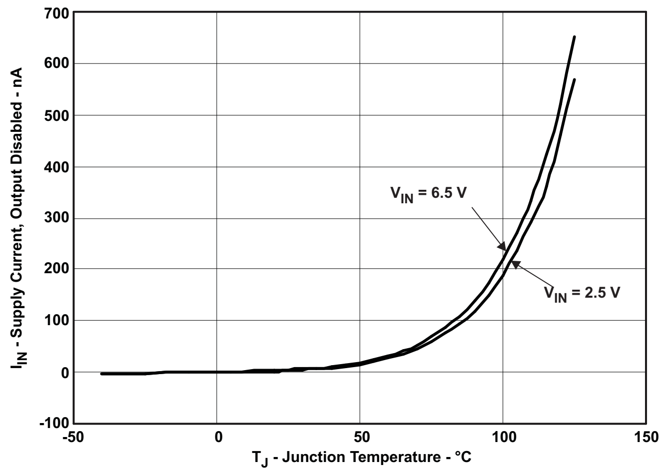


Figure 12. I_{IN} – Supply Current, Output Disabled – nA

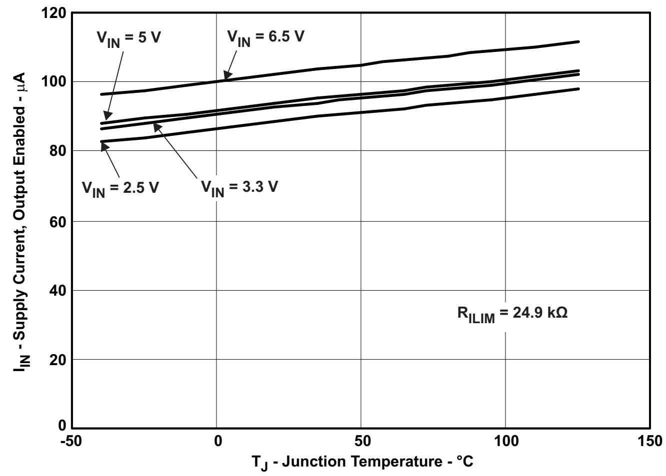


Figure 13. I_{IN} – Supply Current, Output Enabled – µA

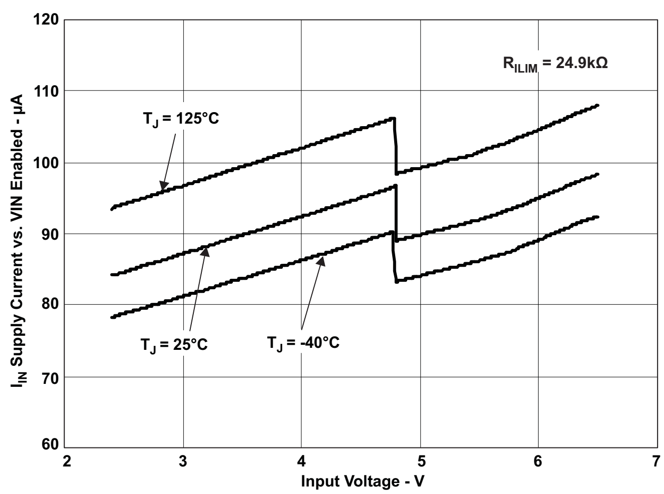


Figure 14. I_{IN} – Supply Current, Output Enabled – µA

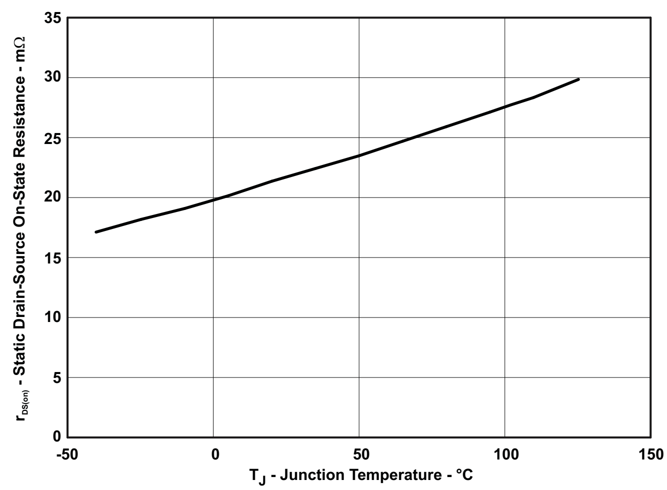


Figure 15. MOSFET $r_{DS(on)}$ Vs. Junction Temperature

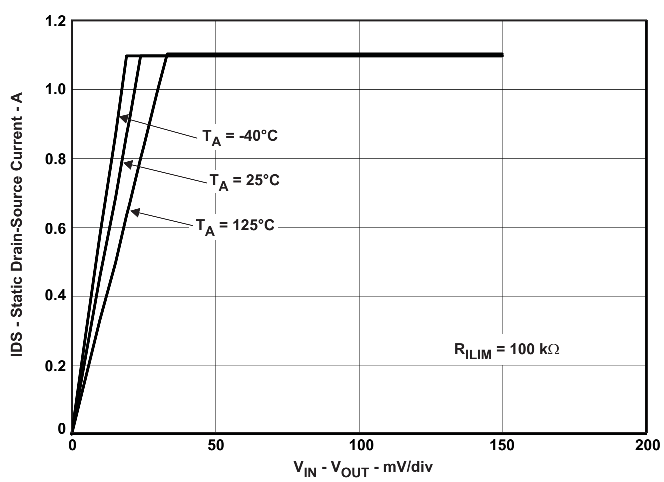


Figure 16. Switch Current Vs. Drain-Source Voltage Across Switch

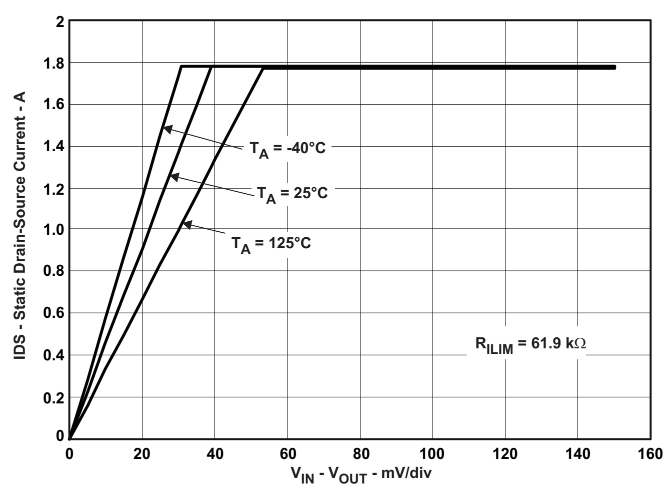


Figure 17. Switch Current Vs. Drain-Source Voltage Across Switch

TYPICAL CHARACTERISTICS (continued)

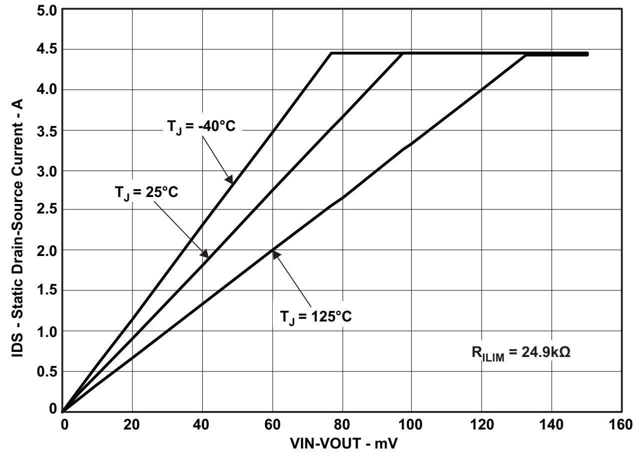


Figure 18. Switch Current vs. Drain-Source Voltage Across Switch

DETAILED DESCRIPTION

OVERVIEW

The TPS2556/57 is a current-limited, power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered. This device allows the user to program the current-limit threshold between 500 mA and 5.0 A (typ) via an external resistor. This device incorporates an internal charge pump and the gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. The TPS2556/57 family limits the output current to the programmed current-limit threshold I_{OS} during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to I_{OS} reduces the output voltage at OUT because N-channel MOSFET is no longer fully enhanced.

OVERCURRENT CONDITIONS

The TPS2556/57 responds to overcurrent conditions by limiting their output current to I_{OS} . When an overcurrent condition is detected, the device maintains a constant output current and the output voltage reduces accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2556/57 ramps the output current to I_{OS}. The TPS2556/57 will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 3). The current-sense amplifier is overdriven during this time and momentarily disables the internal N-channel MOSFET. The current-sense amplifier recovers and ramps the output current to I_{OS}. Similar to the previous case, the TPS2556/57 will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS2556/57 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS2556/57 cycles on/off until the overload is removed (see Figure 10) .

FAULT RESPONSE

The FAULT open-drain output is asserted (active low) during an overcurrent or overtemperature condition. The TPS2556/57 asserts the FAULT signal until the fault condition is removed and the device resumes normal operation. The TPS2556/57 is designed to eliminate false FAULTreporting by using an internal delay "deglitch" circuit for overcurrent (9-ms typ) conditions without the need for external circuitry. This ensures that FAULTis not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions. The FAULTsignal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents FAULT oscillation during an overtemperature event.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

ENABLE (EN OR EN)

The logic enable controls the power switch and device supply current. The supply current is reduced to less than 2-μA when a logic high is present on EN or when a logic low is present on EN. A logic low input on EN or a logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

THERMAL SENSE

The TPS2556/57 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS2556/57 device operates in constant-current mode during an overcurrent conditions, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD) turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20 °C.

The TPS2556/57 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current limit and will turn on the power switch after the device has cooled approximately 20 °C. The TPS2556/57 continues to cycle off and on until the fault is removed.

APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1μF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute-maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

PROGRAMMING THE CURRENT-LIMIT THRESHOLD

The overcurrent threshold is user programmable via an external resistor. The TPS2556/57 uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations approximate the resulting overcurrent threshold for a given external resistor value R_{ILIM}). Consult the Electrical Characteristics table for specific current limit settings. The traces routing the R_{ILIM} resistor to the TPS2556/57 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM}{}^{0.947}k\Omega}$$
$$I_{OSnom}(mA) = \frac{111704V}{R_{ILIM}{}^{1.0028}k\Omega}$$
$$I_{OSmin}(mA) = \frac{127981V}{R_{ILIM}{}^{1.0708}k\Omega} \quad (1)$$

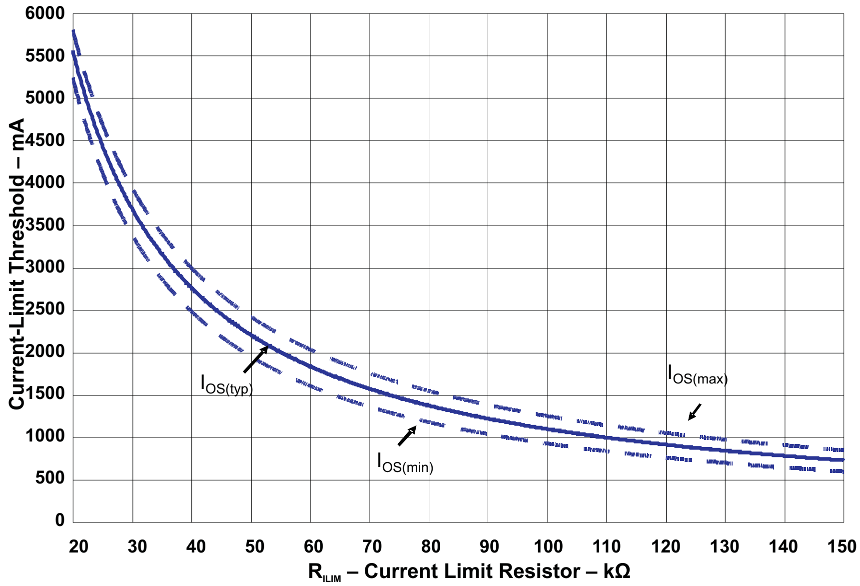


Figure 19. Current-Limit Threshold vs. R_{ILIM}

APPLICATION 1: DESIGNING ABOVE A MINIMUM CURRENT LIMIT

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 3 A must be delivered to the load so that the minimum desired current-limit threshold is 3000 mA. Use the I_{OS} equations and Figure 19 to select R_{ILIM}.

$$I_{OSmin}(mA) = 3000mA$$
$$I_{OSmin}(mA) = \frac{127981V}{R_{ILIM}{}^{1.0708}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{127981V}{I_{OSmin}mA}\right)^{\frac{1}{1.0708}}$$
$$R_{ILIM}(k\Omega) = 33.3k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 33.2 kΩ. This sets the minimum current-limit threshold at 3000 mA . Use the I_{OS} equations, Figure 19, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 33.2k\Omega$$

$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM}^{0.947}k\Omega}$$

$$I_{OSmax}(mA) = \frac{99038V}{33.2^{0.947}k\Omega}$$

$$I_{OSmax}(mA) = 3592mA \tag{3}$$

The resulting maximum current-limit threshold is 3592 mA with a 33.2 kΩ resistor.

APPLICATION 2: DESIGNING BELOW A MAXIMUM CURRENT LIMIT

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 5000 mA to protect an up-stream power supply. Use the I_{OS} equations and Figure 19 to select R_{ILIM}.

$$I_{OSmax}(mA) = 5000mA$$

$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM}^{0.947}k\Omega}$$

$$R_{ILIM}(k\Omega) = \left(\frac{99038V}{I_{OSmax}mA}\right)^{\frac{1}{0.947}}$$

$$R_{ILIM}(k\Omega) = 23.4k\Omega \tag{4}$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 23.7kΩ. This sets the maximum current-limit threshold at 5000 mA . Use the I_{OS} equations, Figure 19, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 23.7k\Omega$$

$$I_{OSmin}(mA) = \frac{127981V}{R_{ILIM}^{1.0708}k\Omega}$$

$$I_{OSmin}(mA) = \frac{127981V}{23.7^{1.0708}k\Omega}$$

$$I_{OSmin}(mA) = 4316mA \tag{5}$$

The resulting minimum current-limit threshold is 4316 mA with a 23.7 kΩ resistor.

ACCOUNTING FOR RESISTOR TOLERANCE

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2556/57 performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired.

Table 1. Common R_{ILIM} Resistor Selections

Desired Nominal Current Limit (mA)		Ideal Resistor (kΩ)	Closest 1% Resistor (kΩ)	Resistor Tolerance			Actual Limits		
				1% low (kΩ)	1% high (kΩ)		IOS MIN (mA)	IOS Nom (mA)	IOS MAX (mA)
750		146.9	147	145.5	148.5		605	749	886
1000		110.2	110	108.9	111.1		825	1002	1166
1250		88.2	88.7	87.8	89.6		1039	1244	1430
1500		73.6	73.2	72.5	73.9		1276	1508	1715

Table 1. Common R_{ILIM} Resistor Selections (continued)

1750		63.1	63.4	62.8	64.0		1489	1742	1965
2000		55.2	54.9	54.4	55.4		1737	2012	2252
2250		49.1	48.7	48.2	49.2		1975	2269	2523
2500		44.2	44.2	43.8	44.6		2191	2501	2765
2750		40.2	40.2	39.8	40.6		2425	2750	3025
3000		36.9	36.5	36.1	36.9		2689	3030	3315
3250		34.0	34.0	33.7	34.3		2901	3253	3545
3500		31.6	31.6	31.3	31.9		3138	3501	3800
3750		29.5	29.4	29.1	29.7		3390	3764	4068
4000		27.7	27.4	27.1	27.7		3656	4039	4349
4250		26.0	26.1	25.8	26.4		3851	4241	4554
4500		24.6	24.9	24.7	25.1		4050	4446	4761
4750		23.3	23.2	23.0	23.4		4369	4773	5091
5000		22.1	22.1	21.9	22.3		4602	5011	5331
5250		21.1	21.0	20.8	21.2		4861	5274	5595
5500		20.1	20.0	19.8	20.2		5121	5539	5859

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}{}^2$$

Where:

P_D = Total power dissipation (W)

$r_{DS(on)}$ = Power switch on-resistance (Ω)

I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

T_A = Ambient temperature (°C)

θ_{JA} = Thermal resistance (°C/W)

P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout. The Dissipating Rating Table provides examples of thermal resistance for specific packages and board layouts.

AUTO-RETRY FUNCTIONALITY

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{FAULT}$ pulls low EN. The part is disabled when EN is pulled below the turn-off theshold, and $\overline{FAULT}$ goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on EN reaches the turn-on threshold. The auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

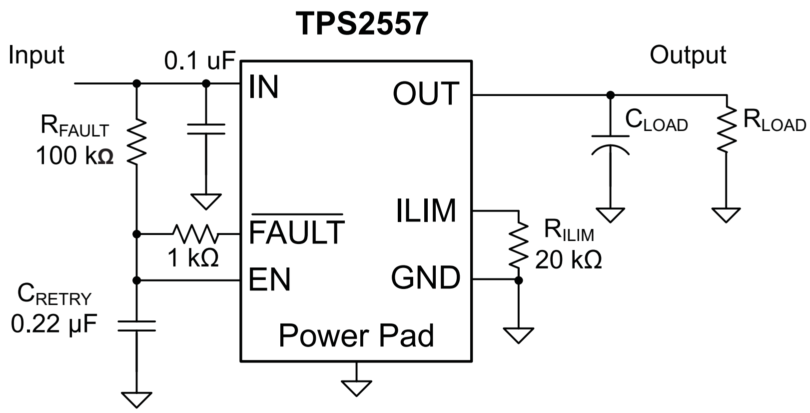


Figure 20. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. The figure below shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

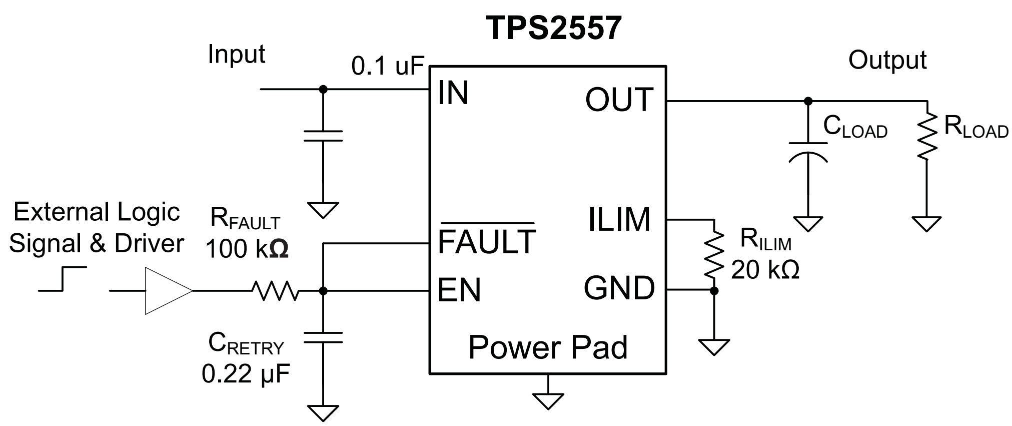


Figure 21. Auto-Retry Functionality With External EN Signal

TWO-LEVEL CURRENT-LIMIT CIRCUIT

Some applications require different current-limit thresholds depending on external system conditions. Figure 22 shows an implementation for an externally-controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see previously discussed "Programming the Current-Limit Threshold" section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

NOTE

ILIM should never be driven directly with an external signal.

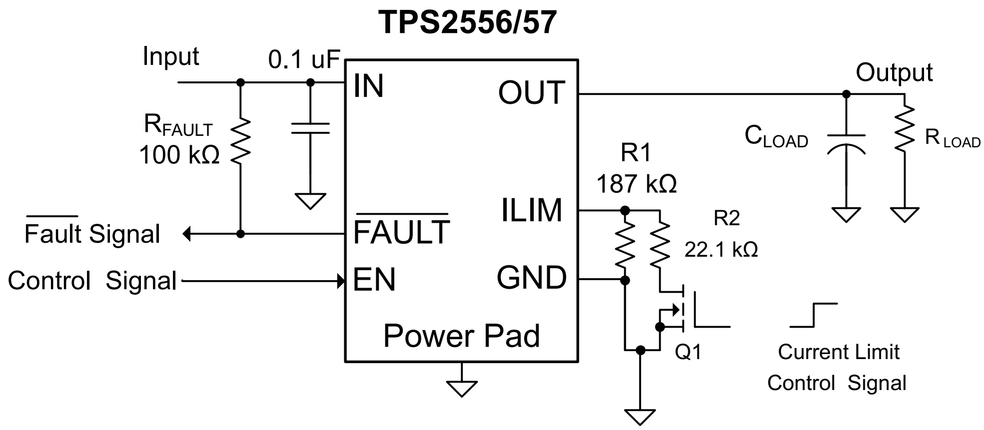


Figure 22. Two-Level Current-Limit Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2556DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2556	Samples
TPS2556DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2556	Samples
TPS2557DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2557	Samples
TPS2557DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2557	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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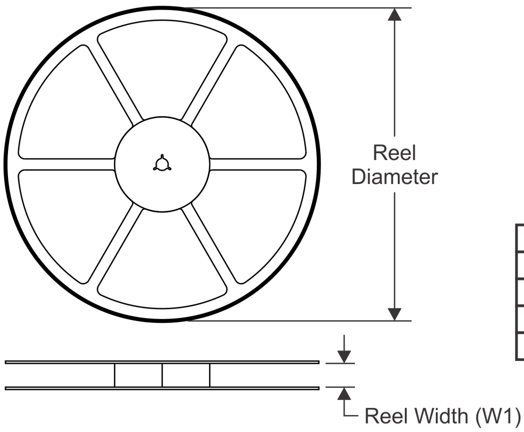
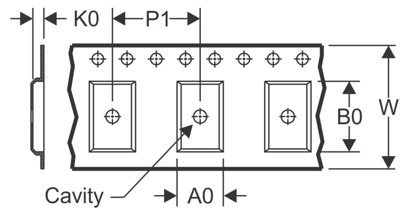
TAPE AND REEL INFORMATION

REEL DIMENSIONS

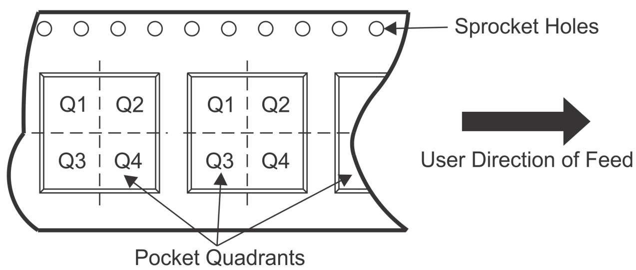


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

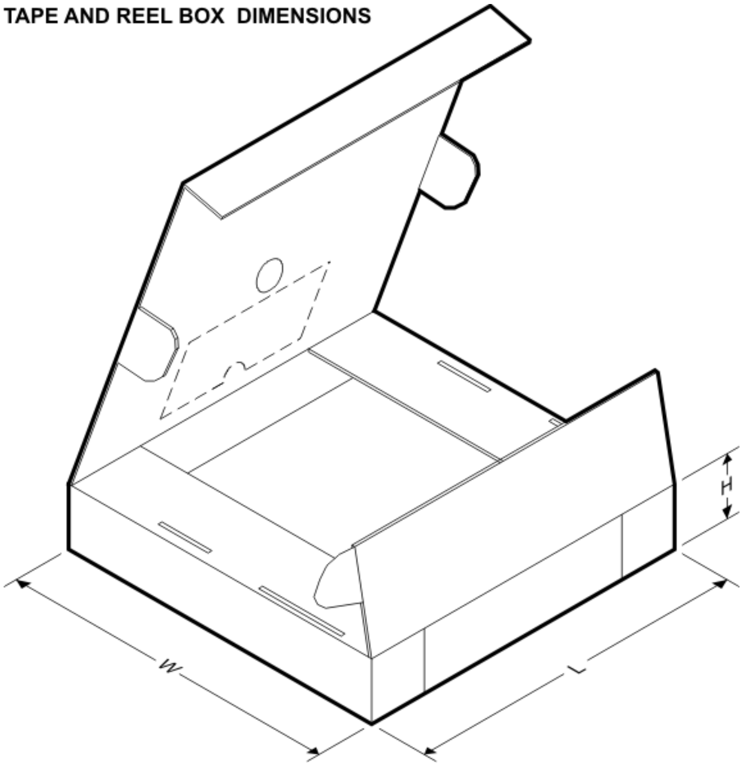
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2556DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2556DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2557DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2557DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

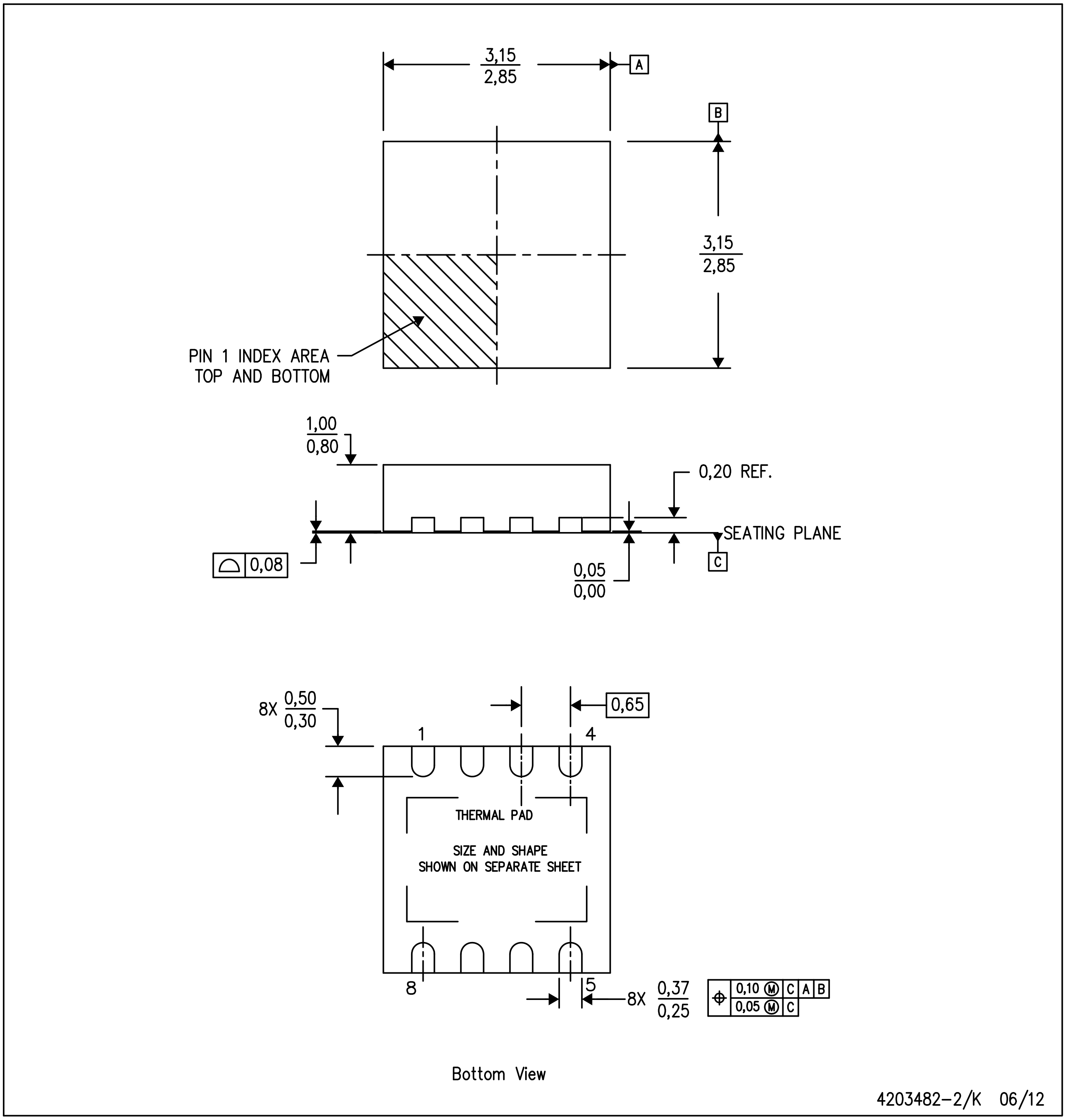
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2556DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS2556DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS2557DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS2557DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

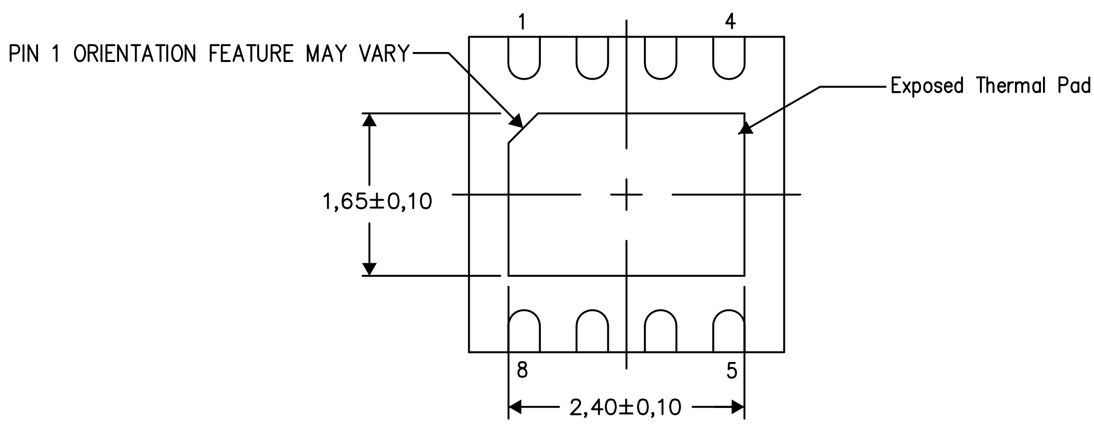
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



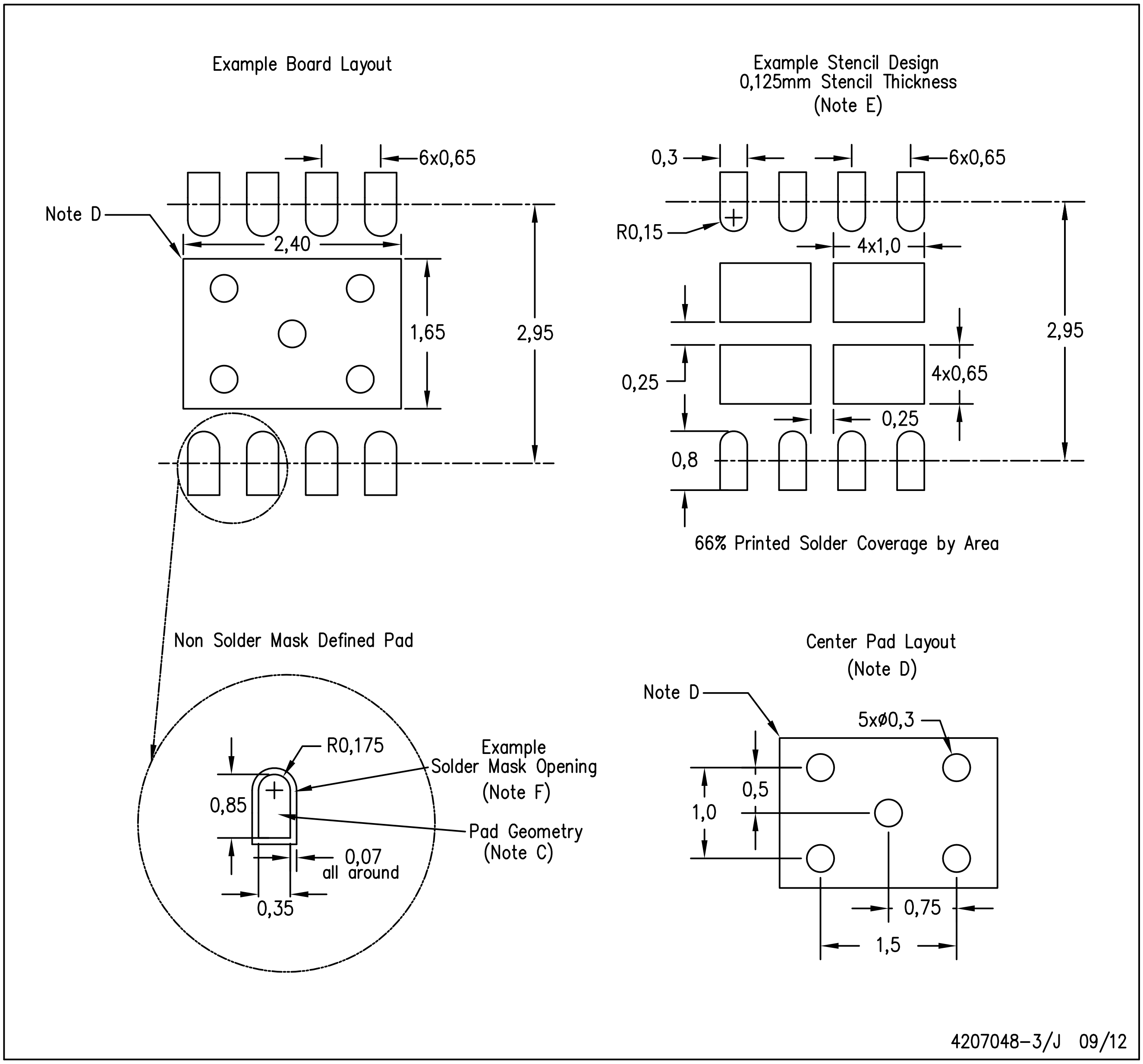
Bottom View

Exposed Thermal Pad Dimensions

4206340-3/N 09/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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