INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors

1 Features

- Wide Common-Mode Range: –0.3 V to 26 V
- Offset Voltage: ±35 µV (Max, INA210) (Enables Shunt Drops of 10-mV Full-Scale)
- Accuracy:
  - ±1% Gain Error (Max over Temperature)
  - 0.5-µV/°C Offset Drift (Max)
  - 10-ppm/°C Gain Drift (Max)
- Choice of Gains:
  - INA210: 200 V/V
  - INA211: 500 V/V
  - INA212: 1000 V/V
  - INA213: 50 V/V
  - INA214: 100 V/V
  - INA215: 75 V/V
- Quiescent Current: 100 µA (max)
- SC70 Package: All Models
- Thin UQFN Package: INA210, INA213, INA214

2 Applications

- Notebook Computers
- Cell Phones
- Telecom Equipment
- Power Management
- Battery Chargers
- Welding Equipment

3 Description

The INA210, INA211, INA212, INA213, INA214, and INA215 are voltage-output, current-shunt monitors that can sense drops across shunts at common-mode voltages from –0.3 V to 26 V, independent of the supply voltage. Five fixed gains are available: 50 V/V, 75 V/V, 100 V/V, 200 V/V, 500 V/V, or 1000 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

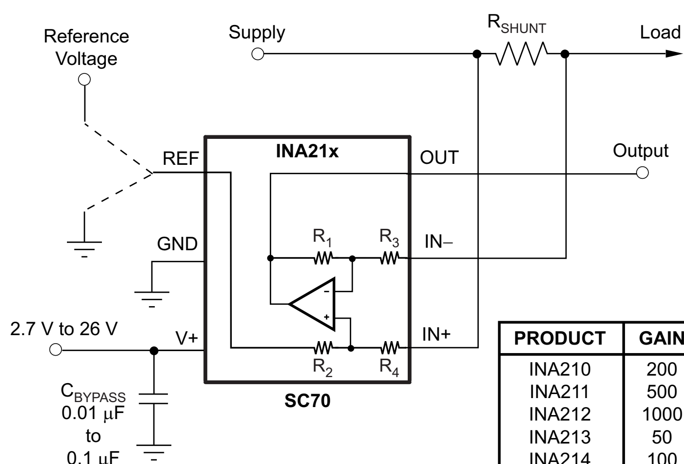
These devices operate from a single 2.7-V to 26-V power supply, drawing a maximum of 100 µA of supply current. All versions are specified over the extended operating temperature range (–40°C to 125°C), and offered in an SC70 package. The INA210, INA213, and INA214 are also offered in a thin UQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA210	SC70 (6)	2.00 mm × 1.25 mm
	UQFN (10)	1.80 mm × 1.40 mm
INA211	SC70 (6)	2.00 mm × 1.25 mm
INA212	SC70 (6)	2.00 mm × 1.25 mm
INA213	SC70 (6)	2.00 mm × 1.25 mm
	UQFN (10)	1.80 mm × 1.40 mm
INA214	SC70 (6)	2.00 mm × 1.25 mm
	UQFN (10)	1.80 mm × 1.40 mm
INA215	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



PRODUCT	GAIN	R_3 and R_4	R_1 and R_2
INA210	200	5 kΩ	1 MΩ
INA211	500	2 kΩ	1 MΩ
INA212	1000	1 kΩ	1 MΩ
INA213	50	20 kΩ	1 MΩ
INA214	100	10 kΩ	1 MΩ
INA215	75	13.3 kΩ	1 MΩ

$V_{OUT} = (I_{LOAD} \times R_{SHUNT})\ Gain + V_{REF}$

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (June 2014) to Revision G — **Page**

- Changed Simplified Schematic: added equation below gain table 1
- Changed $V_{(ESD)}$ *HBM* specifications for version A in Handling Ratings table 5

Changes from Revision E (June 2013) to Revision F — **Page**

- Changed format to meet latest data sheet standards; added Pin Functions, Recommended Operating Conditions, and Thermal Information tables, *Overview*, *Functional Block Diagram*, *Application Information*, *Power Supply Recommendations*, and *Layout* sections, and moved existing sections 1
- Added INA215 to document 1
- Added INA215 sub-bullet to fourth Features bullet 1
- Added INA215 to simplified schematic table 1
- Changed title of Device Options table 4
- Added Thermal Information table 5
- Added INA215 to Figure 7 8
- Added INA215 to Figure 15 9
- Added INA215 to Figure 25 16

Changes from Revision D (November 2012) to Revision E — **Page**

- Deleted Package Marking column from Package/Ordering Information table 4

Changes from Revision C (August 2012) to Revision D — **Page**

- Changed Frequency Response, *Bandwidth* parameter in Electrical Characteristics table 5

Changes from Revision B (June 2009) to Revision C	Page
• Changed Package/Ordering table to show both silicon versions A and B	4
• Added silicon version B ESD ratings to Abs Max table	5
• Added silicon version B row to Input, *Common-Mode Input Range* parameter in Electrical Characteristics table	5
• Corrected typo in Figure 9	8
• Updated Figure 12	8
• Changed *Input Filtering* section	14
• Added *Improving Transient Robustness* section	19

Changes from Revision A (June 2008) to Revision B	Page
• Added RSW package to device photo	1
• Added UQFN package to *Features* list	1
• Updated front page graphic	1
• Added RSW ordering information to *Package/Ordering Information* table	4
• Added RSW package pin out drawing	4
• Added footnote 3 to *Electrical Characteristics* table	5
• Added UQFN package information to *Temperature Range* section of *Electrical Characteristics* table	5
• Changed Figure 2 to reflect operating temperature range	8
• Changed Figure 4 to reflect operating temperature range	8
• Changed Figure 6 to reflect operating temperature range	8
• Changed Figure 13 to reflect operating temperature range	9
• Changed Figure 14 to reflect operating temperature range	9
• Added RSW description to the *Basic Connections* section	13
• Changed 60μV to 100μV in last sentence of the *Selecting RS* section	13

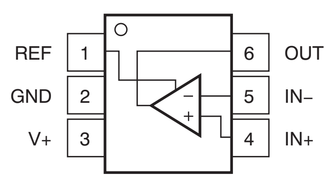
Changes from Original (May 2008) to Revision A	Page
• Changed availability of INA211 and INA212 to currently available in *Package/Ordering Information* table	4
• Deleted first footnote of *Electrical Characteristics* table	5
• Changed Figure 7	8
• Changed Figure 15	9

5 Device Options

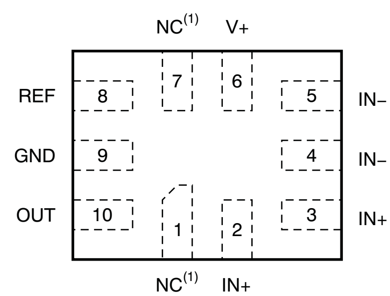
PRODUCT	GAIN (V/V)	PACKAGE	PACKAGE DESIGNATOR
INA210A	200	SC70-6	DCK
	200	Thin UQFN-10	RSW
INA210B	200	SC70-6	DCK
	200	Thin UQFN-10	RSW
INA211A	500	SC70-6	DCK
INA211B	500	SC70-6	DCK
INA212A	1000	SC70-6	DCK
INA212B	1000	SC70-6	DCK
INA213A	50	SC70-6	DCK
	50	Thin UQFN-10	RSW
INA213B	50	SC70-6	DCK
	50	Thin UQFN-10	RSW
INA214A	100	SC70-6	DCK
	100	Thin UQFN-10	RSW
INA214B	100	SC70-6	DCK
	100	Thin UQFN-10	RSW
INA215A	75	SC70-6	DCK

6 Pin Configurations and Functions

DCK Package
SC70-6
(Top View)



RSW Package
Thin UQFN-10
(Top View)



(1) NC denotes no internal connection. These pins can be left floating or connected to any voltage between V– and V+.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DCK	RSW		
GND	2	9	Analog	Ground
IN–	5	4, 5	Analog input	Connect to load side of shunt resistor.
IN+	4	2, 3	Analog input	Connect to supply side of shunt resistor
NC	—	1, 7	—	Not internally connected. Leave floating or connect to ground.
OUT	6	10	Analog output	Output voltage
REF	1	8	Analog input	Reference voltage, 0 V to V+
V+	3	6	Analog	Power supply, 2.7 V to 26 V

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_S			26	V
Analog inputs, V_{IN+}, $V_{IN–}$ (2)	Differential $(V_{IN+}) – (V_{IN–})$	–26	26	V
	Common-mode (3)	GND – 0.3	26	V
REF input		GND – 0.3	(V_S) + 0.3	V
Output(3)		GND – 0.3	(V_S) + 0.3	V
Input current into any terminal(3)			5	mA
Operating temperature		–55	150	°C
Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– terminals, respectively.
(3) Input voltage at any terminal may exceed the voltage shown if the current at that terminal is limited to 5 mA.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge (version A)	Human body model (HBM) ESD stress voltage(1)	–2000	2000	V
		Charged-device model (CDM) ESD stress voltage(2)	–1000	1000	
		Machine model (MM) ESD stress voltage	–200	200	
$V_{(ESD)}$	Electrostatic discharge (version B)	Human body model (HBM) ESD stress voltage(1)	–1500	1500	V
		Charged-device model (CDM) ESD stress voltage(2)	–1000	1000	
		Machine model (MM) ESD stress voltage	–100	100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		INA210-INA215 DCK (SC70) 6 PINS	INA210-INA215 RSW (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	107.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	18.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.4	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At T_A = 25°C, $V_{SENSE} = V_{IN+} – V_{IN–}$.
INA210, INA213, INA214, and INA215: V_S = 5 V, V_{IN+} = 12 V, and $V_{REF} = V_S$ / 2, unless otherwise noted.
INA211 and INA212: V_S = 12 V, V_{IN+} = 12 V, and $V_{REF} = V_S$ / 2, unless otherwise noted.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{CM}	Common-mode input range		Version A, T_A = –40°C to 125°C	–0.3		26	V
			Version B, T_A = –40°C to 125°C	–0.1		26	V
CMRR	Common-mode rejection ratio	INA210, INA211, INA212, INA214, INA215	V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV, T_A = –40°C to 125°C	105	140		dB
		INA213	V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV, T_A = –40°C to 125°C	100	120		dB
V_O	Offset voltage, RTI[1]	INA210, INA211, INA212	V_{SENSE} = 0 mV		±0.55	±35	μV
		INA213	V_{SENSE} = 0 mV		±5	±100	μV
		INA214, INA215	V_{SENSE} = 0 mV		±1	±60	μV
dV_{OS}/dT	RTI vs temperature		V_{SENSE} = 0 mV, T_A = –40°C to 125°C		0.1	0.5	μV/°C
PSRR	RTI vs power supply ratio		V_S = 2.7 V to 18 V, V_{IN+} = 18 V, V_{SENSE} = 0 mV		±0.1	±10	μV/V
I_{IB}	Input bias current		V_{SENSE} = 0 mV	15	28	35	μA
I_{IO}	Input offset current		V_{SENSE} = 0 mV		±0.02		μA
OUTPUT							
G	Gain	INA210			200		V/V
		INA211			500		V/V
		INA212			1000		V/V
		INA213			50		V/V
		INA214			100		V/V
		INA215			75		V/V
E_G	Gain error		V_{SENSE} = –5 mV to 5 mV, T_A = –40°C to 125°C		±0.02%	±1%	
	Gain error vs temperature		T_A = –40°C to 125°C		3	10	ppm/°C
	Nonlinearity error		V_{SENSE} = –5 mV to 5 mV		±0.01%		
	Maximum capacitive load		No sustained oscillation		1		nF

(1) RTI = referred-to-input.

Electrical Characteristics (continued)

At T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$.
INA210, INA213, INA214, and INA215: V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.
INA211 and INA212: V_S = 12 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE OUTPUT(2)							
	Swing to V+ power-supply rail		R_L = 10 kΩ to GND, T_A = –40°C to 125°C		(V+) – 0.05	(V+) – 0.2	V
	Swing to GND		R_L = 10 kΩ to GND, T_A = –40°C to 125°C		(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth		C_{LOAD} = 10 pF, INA210		14		kHz
			C_{LOAD} = 10 pF, INA211		7		kHz
			C_{LOAD} = 10 pF, INA212		4		kHz
			C_{LOAD} = 10 pF, INA213		80		kHz
			C_{LOAD} = 10 pF, INA214		30		kHz
			C_{LOAD} = 10 pF, INA215		40		kHz
SR	Slew rate				0.4		V/µs
NOISE, RTI(1)							
	Voltage noise density				25		nV/√Hz
POWER SUPPLY							
V_S	Operating voltage range		T_A = –40°C to 125°C	2.7		26	V
I_Q	Quiescent current		V_{SENSE} = 0 mV		65	100	µA
	I_Q over temperature		T_A = –40°C to 125°C			115	µA
TEMPERATURE RANGE							
	Specified range			–40		125	°C
	Operating range			–55		150	°C
θ_{JA}	Thermal resistance	SC70			250		°C/W
		Thin UQFN			80		°C/W

(2) See Typical Characteristic curve, *Output Voltage Swing vs Output Current* (Figure 10).

7.6 Typical Characteristics

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

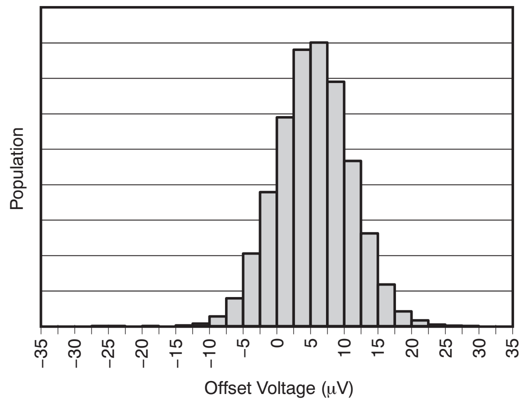


Figure 1. Input Offset Voltage Production Distribution

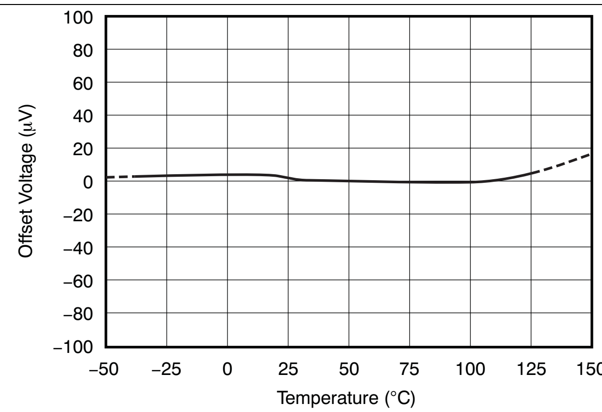


Figure 2. Offset Voltage vs Temperature

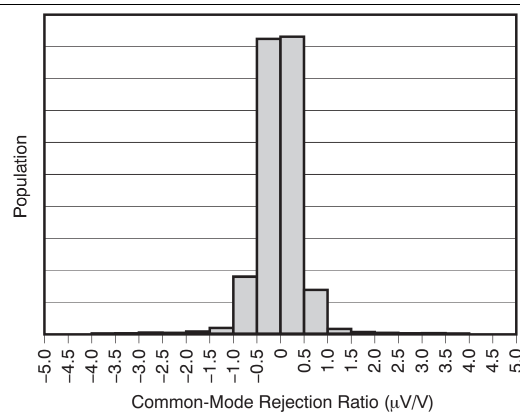


Figure 3. Common-Mode Rejection Production Distribution

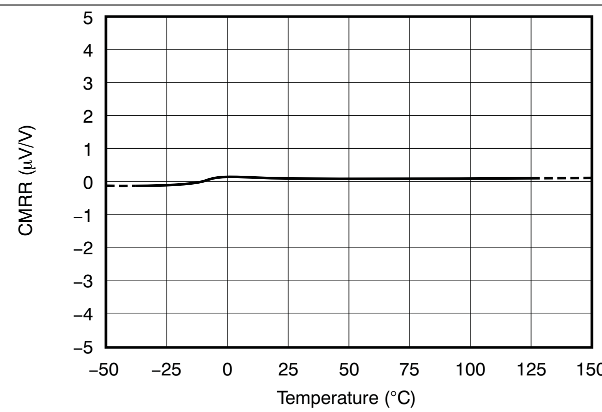


Figure 4. Common-Mode Rejection Ratio vs Temperature

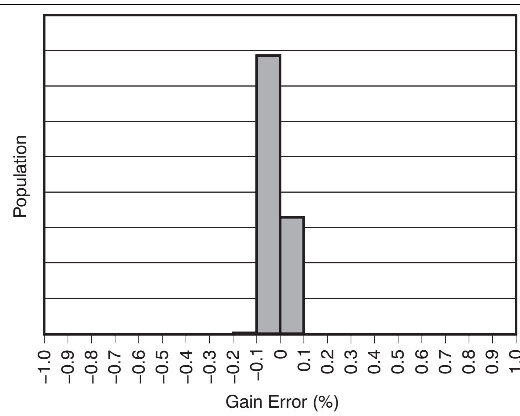


Figure 5. Gain Error Production Distribution

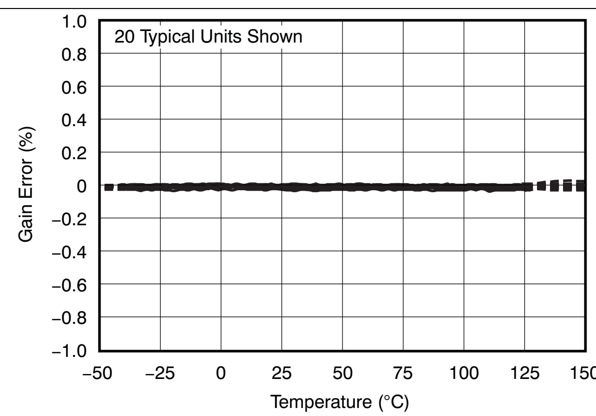


Figure 6. Gain Error vs Temperature

Typical Characteristics (continued)

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

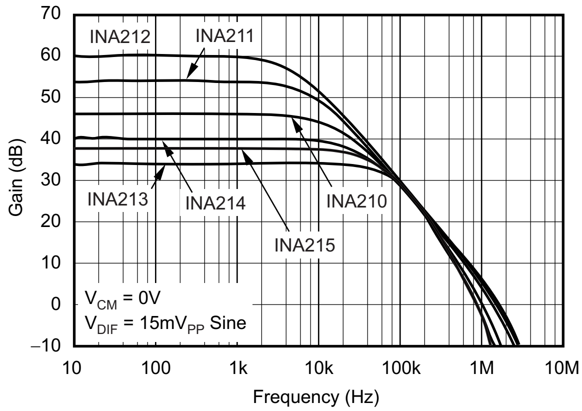


Figure 7. Gain vs Frequency

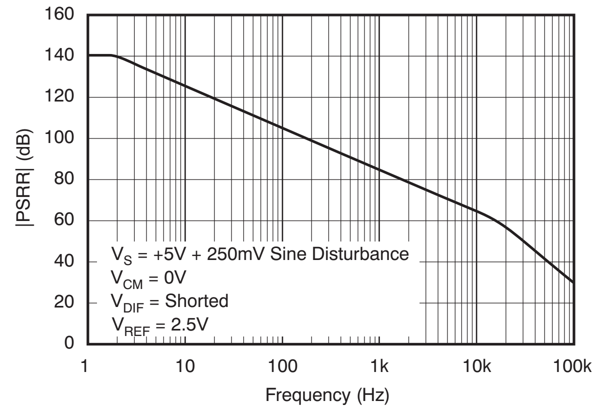


Figure 8. Power-Supply Rejection Ratio vs Frequency

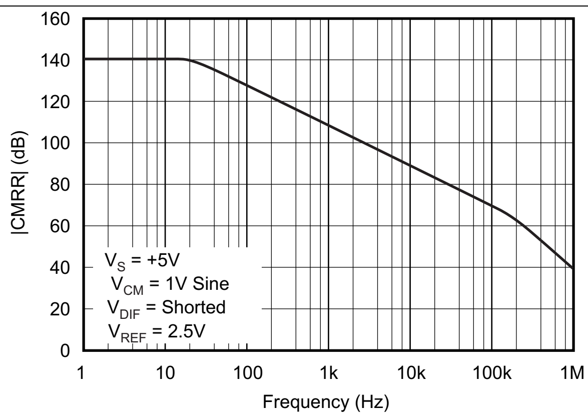


Figure 9. Common-Mode Rejection Ratio vs Frequency

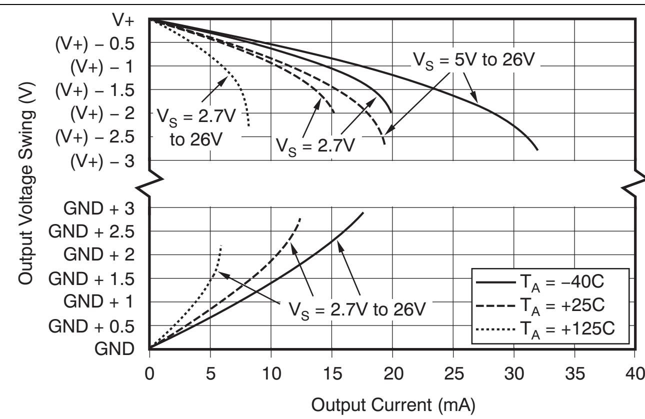


Figure 10. Output Voltage Swing vs Output Current

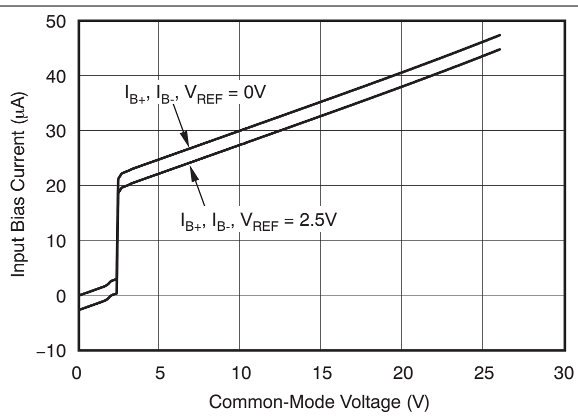


Figure 11. Input Bias Current vs Common-Mode Voltage with Supply Voltage = 5 V

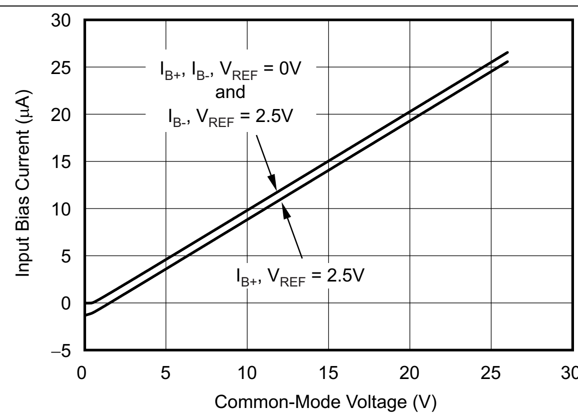


Figure 12. Input Bias Current vs Common-Mode Voltage with Supply Voltage = 0 V (Shutdown)

Typical Characteristics (continued)

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

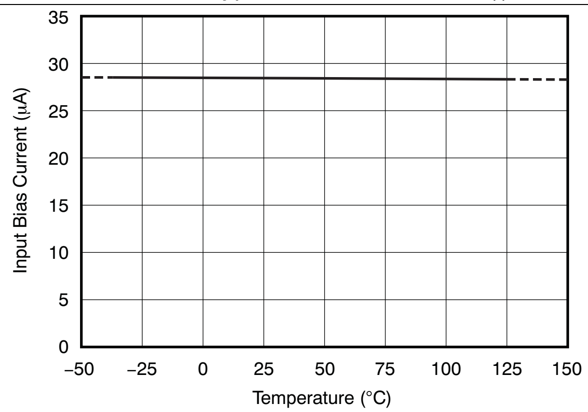


Figure 13. Input Bias Current vs Temperature

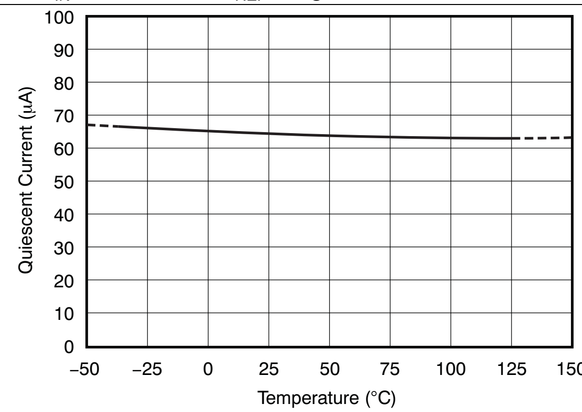


Figure 14. Quiescent Current vs Temperature

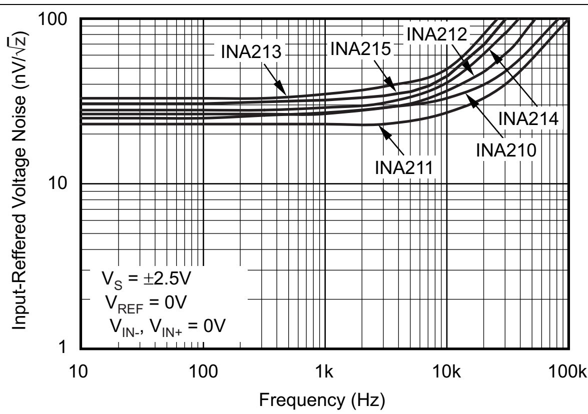


Figure 15. Input-Referred Voltage Noise vs Frequency

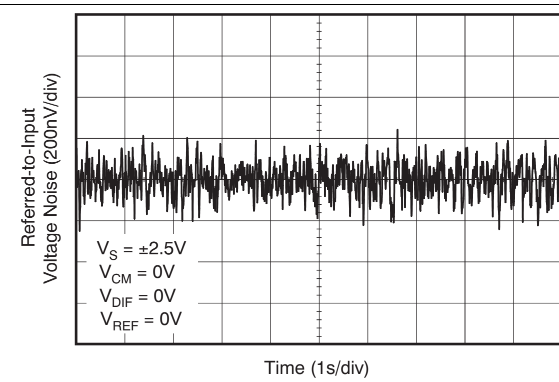


Figure 16. 0.1-Hz to 10-Hz Voltage Noise (Referred-To-Input)

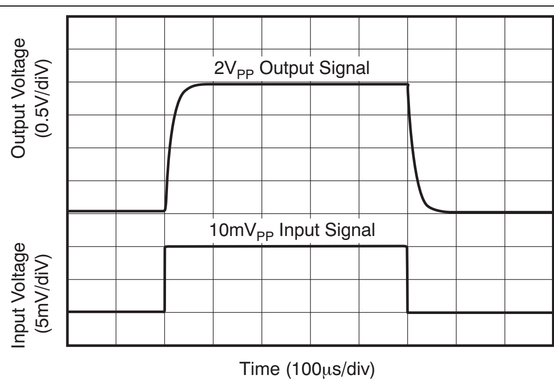


Figure 17. Step Response (10-mV_{PP} Input Step)

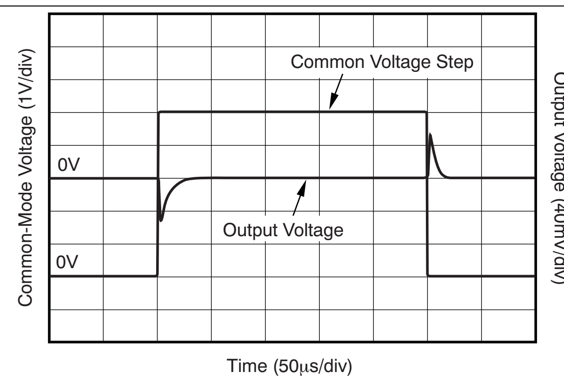


Figure 18. Common-Mode Voltage Transient Response

Typical Characteristics (continued)

The INA210 is used for typical characteristics at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

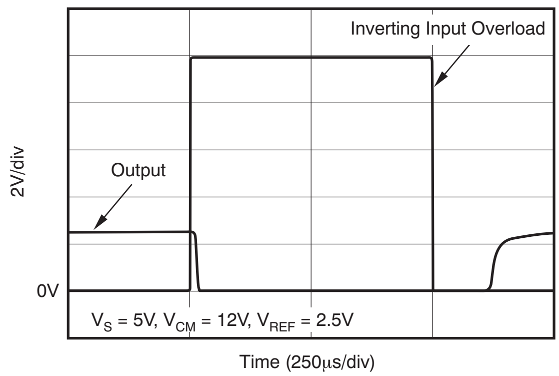


Figure 19. Inverting Differential Input Overload

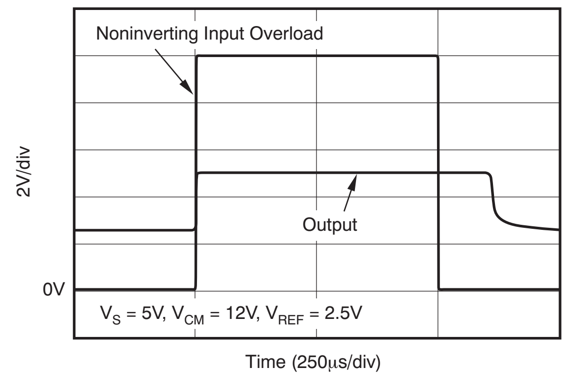


Figure 20. Noninverting Differential Input Overload

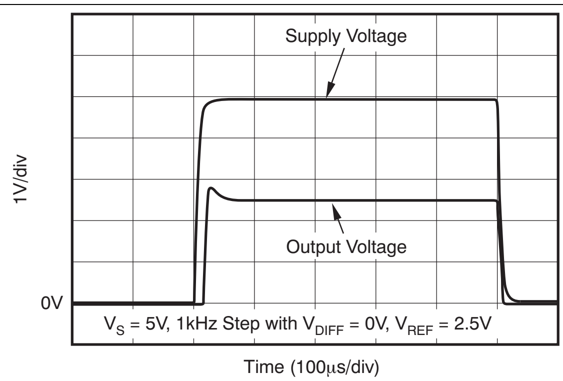


Figure 21. Start-Up Response

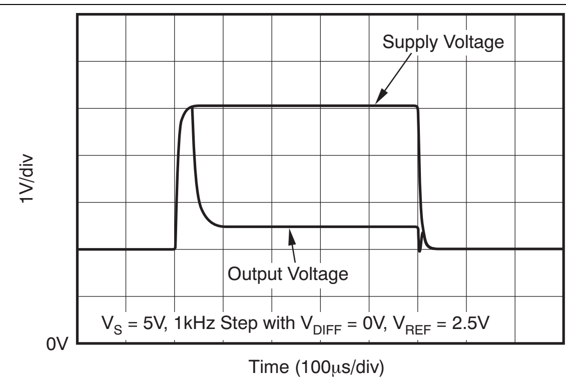


Figure 22. Brownout Recovery

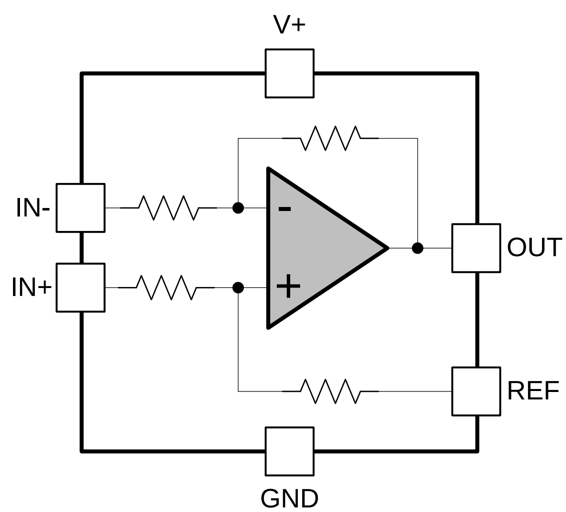
8 Detailed Description

8.1 Overview

The INA210-INA215 are 26-V, common-mode, zero-drift topology, current-sensing amplifiers that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V while the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 35 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40°C to 125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Basic Connections

Figure 23 shows the basic connections of the INA210-INA215. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

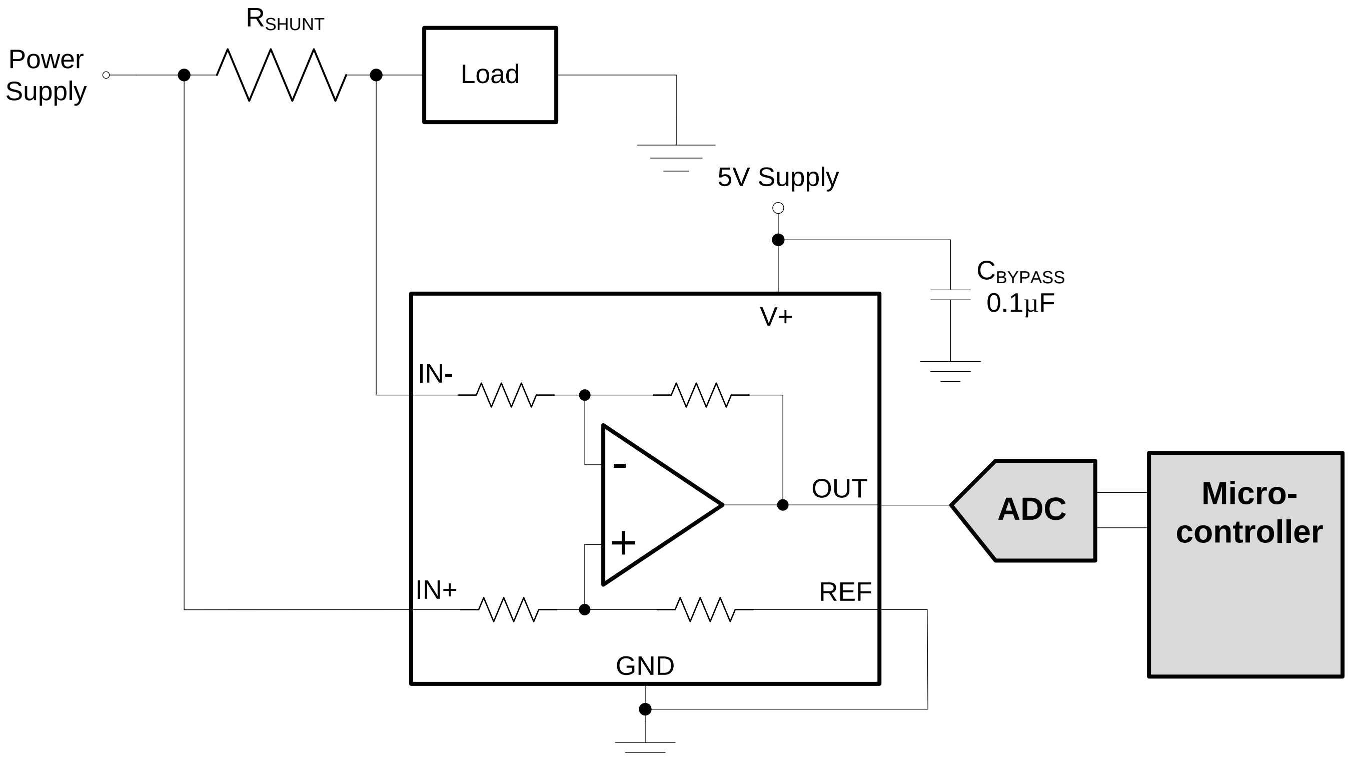


Figure 23. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

On the RSW package options, two pins are provided for each input. These pins should be tied together (that is, tie IN+ to IN+ and tie IN– to IN–).

8.3.2 Selecting R_S

The zero-drift offset performance of the INA210-INA215 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100 mV.

The INA210-INA215 series gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the INA213, INA214 or INA215 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA213 operating on a 3.3-V supply could easily handle a full-scale shunt drop of 60 mV, with only 100 µV of offset.

8.4 Device Functional Modes

8.4.1 Input Filtering

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. Figure 24 shows a filter placed at the inputs pins.

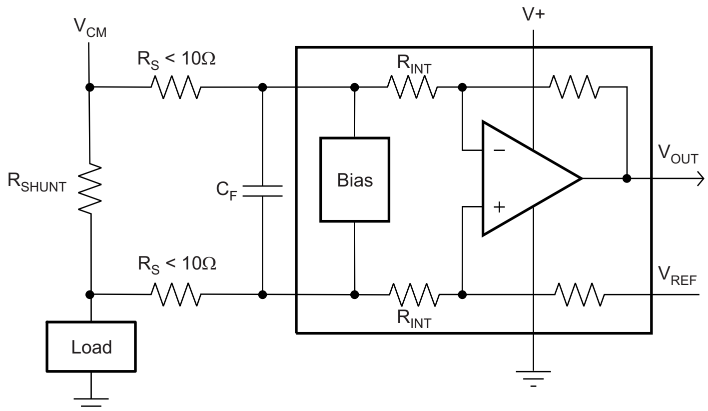


Figure 24. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors should be kept to 10Ω or less if possible to reduce impact to accuracy. The internal bias network shown in Figure 24 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as shown in Figure 24). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 1:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})}$$

where:

- R_{INT} is the internal input resistor (R3 and R4), and
- R_S is the external series resistance. (1)

Device Functional Modes (continued)

With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as shown in Table 1. Each individual device gain error factor is shown in Table 2.

Table 1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA210	200	5
INA211	500	2
INA212	1000	1
INA213	50	20
INA214	100	10
INA215	75	13.3

Table 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA210	$\frac{1000}{R_S + 1000}$
INA211	$\frac{10,000}{(13 \times R_S) + 10,000}$
INA212	$\frac{5000}{(9 \times R_S) + 5000}$
INA213	$\frac{20,000}{(17 \times R_S) + 20,000}$
INA214	$\frac{10,000}{(9 \times R_S) + 10,000}$
INA215	$\frac{8,000}{(7 \times R_S) + 8,000}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

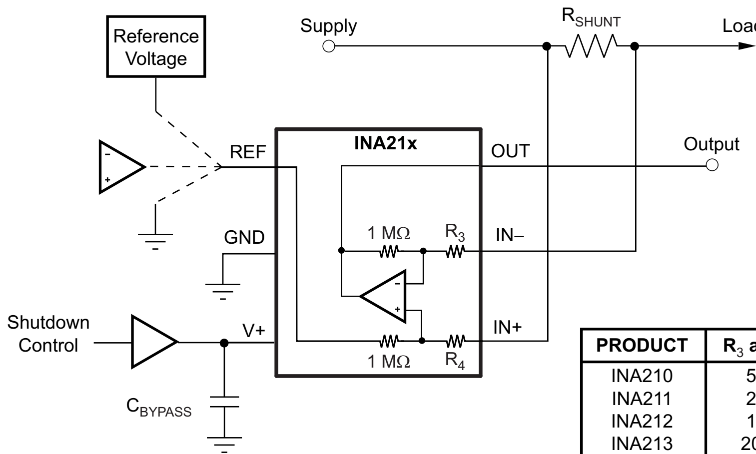
$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (2)$$

For example, using an INA212 and the corresponding gain error equation from Table 2, a series resistance of 10 Ω results in a gain error factor of 0.982. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 1.77% solely because of the external 10-Ω series resistors. Using an INA213 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

8.4.2 Shutting Down the INA210-INA215 Series

While the INA210-INA215 series does not have a shutdown pin, its low power consumption allows powering from the output of a logic gate or transistor switch that can turn on and turn off the INA210-INA215 power-supply quiescent current.

However, in current shunt monitoring applications. there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INA210-INA215 in shutdown mode shown in Figure 25.



PRODUCT	R_3 and R_4
INA210	5 kΩ
INA211	2 kΩ
INA212	1 kΩ
INA213	20 kΩ
INA214	10 kΩ
INA215	13.3 kΩ

NOTE: 1-MΩ paths from shunt inputs to reference and INA21x outputs.

Figure 25. Basic Circuit for Shutting Down the INA210-INA215 with a Grounded Reference

Note that there is typically slightly more than 1-MΩ impedance (from the combination of 1-MΩ feedback and 5-kΩ input resistors) from each input of the INA210-INA215 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or op amp is powered while the INA210-INA215 is shut down, the calculation is direct; instead of assuming 1 MΩ to ground, however, assume 1 MΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source behaves as an open circuit when is not powered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled INA210-INA215 does constitute a good path to ground; consequently, this current is directly proportional to a shunt common-mode voltage impressed across a 1-MΩ resistor.

As a final note, when the device is powered up, there is an additional, nearly constant, and well-matched 25 µA that flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the only current effects are the result of the 1-MΩ resistors.

8.4.3 REF Input Impedance Effects

As with any difference amplifier, the INA210-INA215 series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin should be buffered by an op amp.

In systems where the INA210-INA215 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 26 depicts a method of taking the output from the INA210-INA215 by using the REF pin as a reference.

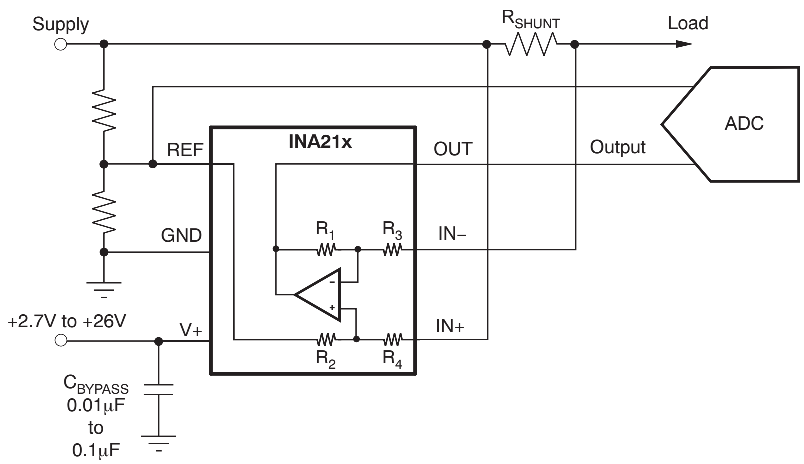


Figure 26. Sensing the INA210-INA215 to Cancel the Effects of Impedance on the REF Input

8.4.4 Using The INA210-INA215 with Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA210-INA215 series can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only zener diode or zener-type transient absorbers (sometimes referred to as *Transzorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the zener; see Figure 27. Keeping these resistors as small as possible is preferable, most often around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Input Filtering* section. Because this circuit is limiting only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

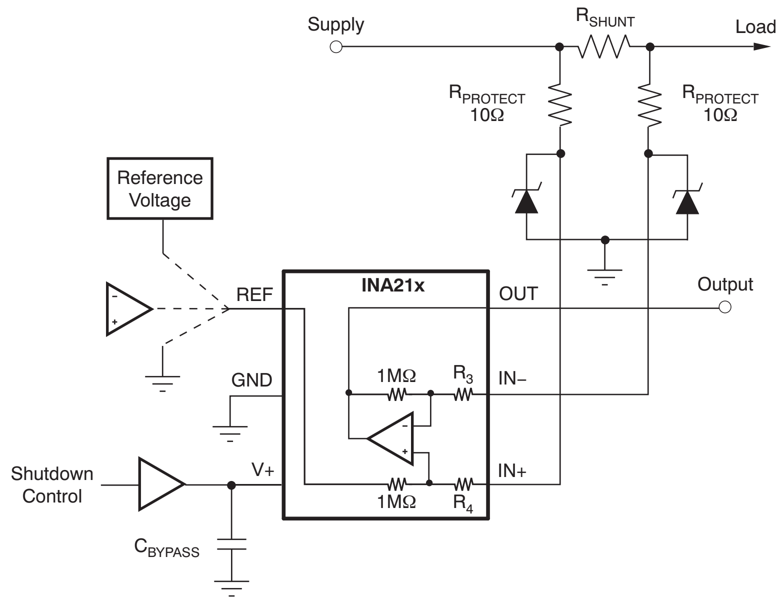


Figure 27. INA210-INA215 Transient Protection using Dual Zener Diodes

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. This method is shown in Figure 28. In either of these examples, the total board area required by the INA210-INA215 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

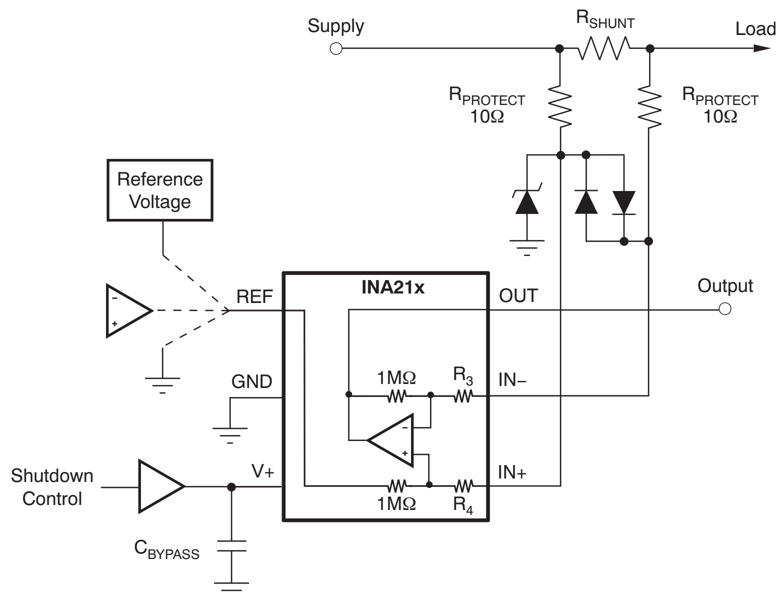


Figure 28. INA210-INA215 Transient Protection using a Single Transzorb and Input Clamps

8.4.5 Improving Transient Robustness

Applications involving large input transients with excessive dV/dt above 2 kV per microsecond present at the device input pins may cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Care must be taken to ensure that external series input resistance does not significantly impact gain error accuracy. For accuracy purposes, these resistances should be kept under 10 Ω if possible. Ferrite beads are recommended for this filter because of their inherently low dc ohmic value. Ferrite beads with less than 10 Ω of resistance at dc and over 600 Ω of resistance at 100 MHz to 200 MHz are recommended. The recommended capacitor values for this filter are between 0.01 µF and 0.1 µF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 29.

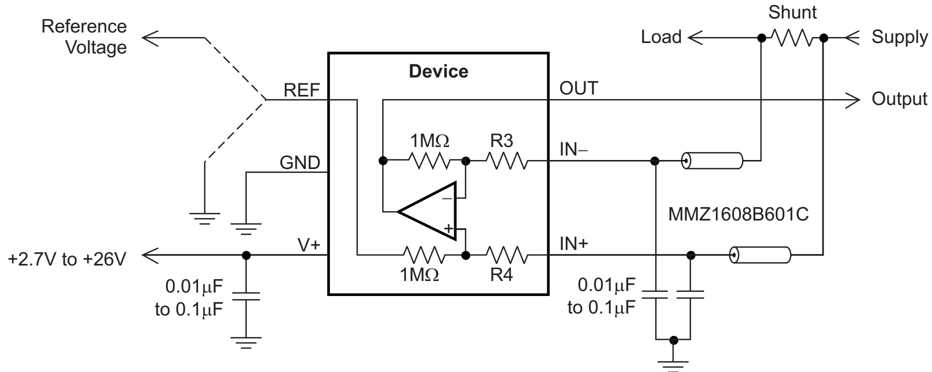


Figure 29. Transient Protection

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B devices are now available with new ESD structures that are not susceptible to this latching condition. Version B devices are incapable of sustaining these damage causing latched conditions so they do not have the same sensitivity to the transients that the version A devices have, thus making the version B devices a better fit for these applications.

9 Application and Implementation

9.1 Application Information

The INA210-INA215 measure the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

9.2 Typical Applications

9.2.1 Unidirectional Operation

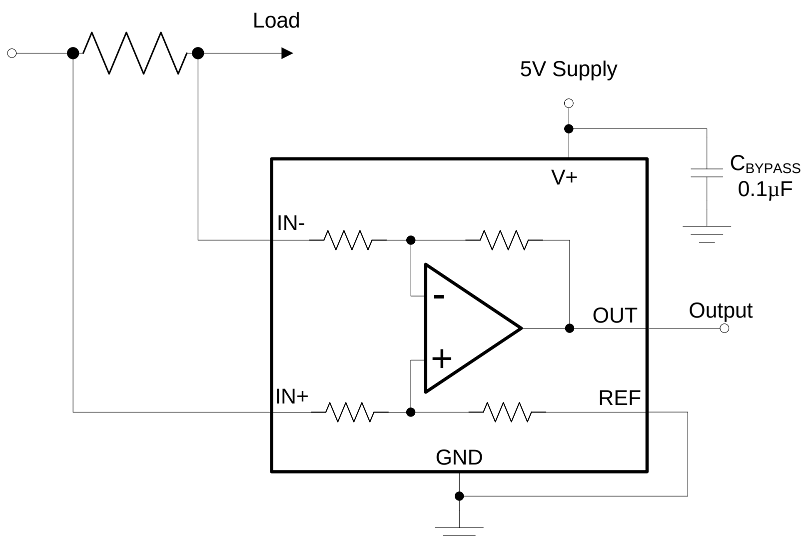


Figure 30. Unidirectional Application Schematic

9.2.1.1 Design Requirements

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 30. When the input signal increases, the output voltage at the OUT pin increases.

9.2.1.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, TI recommends buffering the reference voltage connected to the REF pin.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

Typical Applications (continued)

9.2.1.3 Application Curve

An example output response of a unidirectional configuration is shown in Figure 31. With the REF pin connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

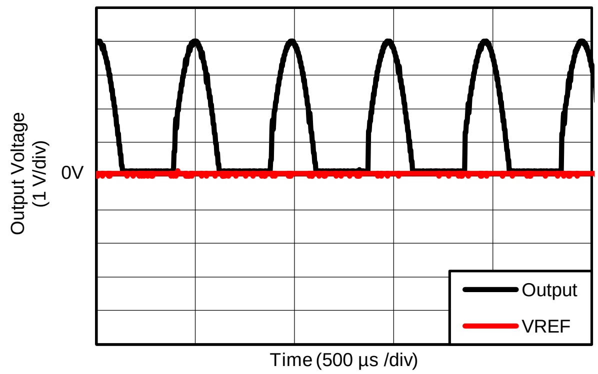


Figure 31. Unidirectional Application Output Response

Typical Applications (continued)

9.2.2 Bidirectional Operation

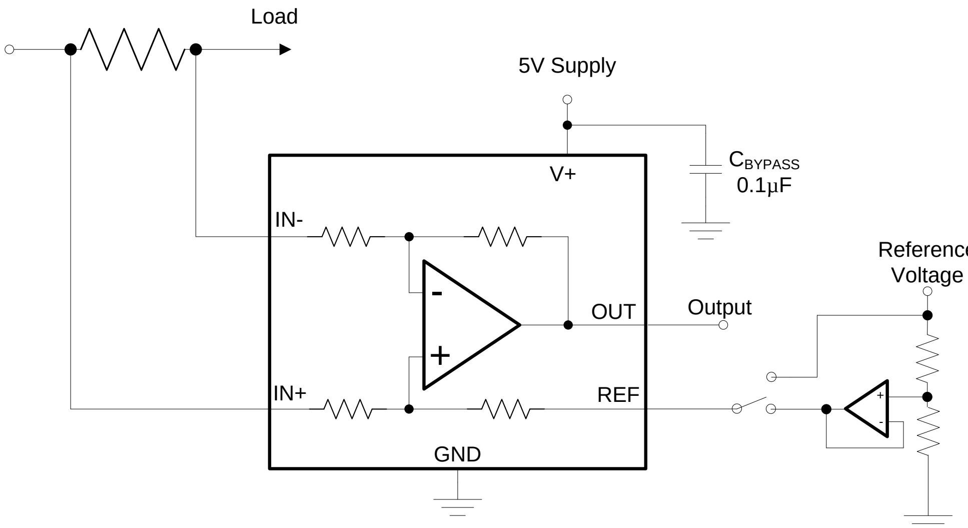


Figure 32. Bidirectional Application Schematic

9.2.2.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

9.2.2.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in Figure 32. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, V_{REF} is typically set at mid-scale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

9.2.2.3 Application Curve

An example output response of a bidirectional configuration is shown in Figure 33. With the REF pin connected to a reference voltage, 2.5 V in this case, the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals and falls below the reference voltage for negative differential input signals.

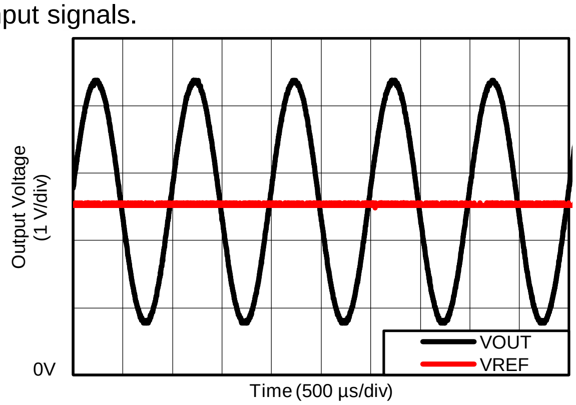


Figure 33. Bidirectional Application Output Response

10 Power Supply Recommendations

The input circuitry of the INA210-INA215 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Note also that the INA210-INA215 can withstand the full input signal range up to 26 V at the input pins, regardless of whether the device has power applied or not.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- The power-supply bypass capacitor should be placed as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

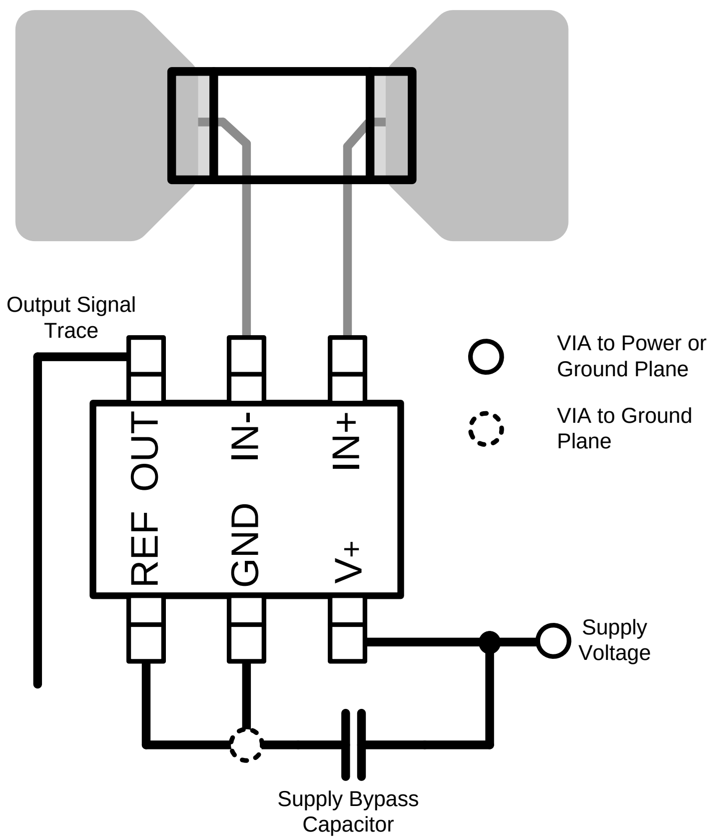


Figure 34. Recommended Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- INA210-215EVM User's Guide, SBOU065

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA210	Click here	Click here	Click here	Click here	Click here
INA211	Click here	Click here	Click here	Click here	Click here
INA212	Click here	Click here	Click here	Click here	Click here
INA213	Click here	Click here	Click here	Click here	Click here
INA214	Click here	Click here	Click here	Click here	Click here
INA215	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA210AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CET	Samples
INA210AIDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CET	Samples
INA210AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CET	Samples
INA210AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CET	Samples
INA210AIRSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KNJ	Samples
INA210AIRSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(KNJ ~ NSJ)	Samples
INA210BIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SED	Samples
INA210BIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SED	Samples
INA210BIRSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHQ	Samples
INA210BIRSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHQ	Samples
INA211AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEU	Samples
INA211AIDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEU	Samples
INA211AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEU	Samples
INA211AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEU	Samples
INA211BIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEE	Samples
INA211BIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEE	Samples
INA212AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA212AIDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEV	Samples
INA212AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEV	Samples
INA212AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEV	Samples
INA212BIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEC	Samples
INA212BIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEC	Samples
INA213AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFT	Samples
INA213AIDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFT	Samples
INA213AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFT	Samples
INA213AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFT	Samples
INA213AIRSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KPJ	Samples
INA213AIRSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KPJ	Samples
INA213BIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEF	Samples
INA213BIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEF	Samples
INA213BIRSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHT	Samples
INA213BIRSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHT	Samples
INA214AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFV	Samples
INA214AIDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFV	Samples
INA214AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA214AIDCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CFV	Samples
INA214AIRSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KRJ	Samples
INA214AIRSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KRJ	Samples
INA214BIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEA	Samples
INA214BIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SEA	Samples
INA214BIRSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHU	Samples
INA214BIRSWT	ACTIVE	UQFN	RSW	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SHU	Samples
INA215AIDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SME	Samples
INA215AIDCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SME	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA212, INA214 :

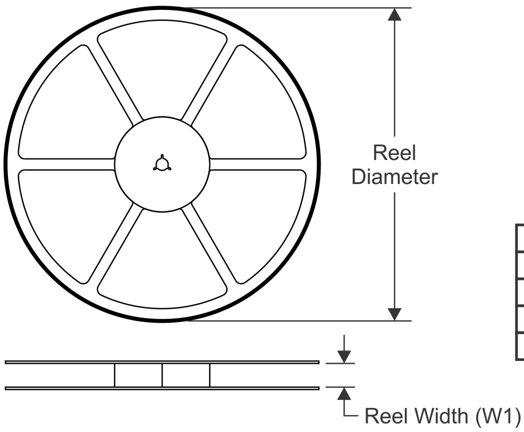
- Automotive: INA212-Q1, INA214-Q1

NOTE: Qualified Version Definitions:

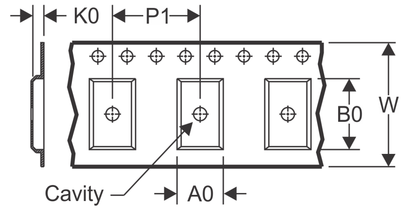
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

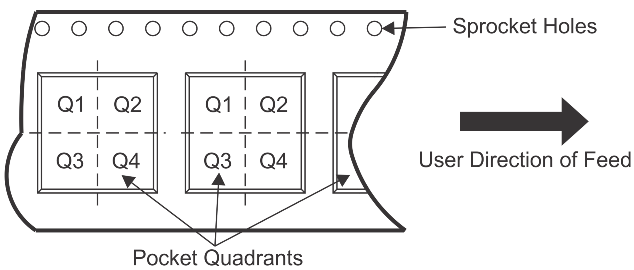


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

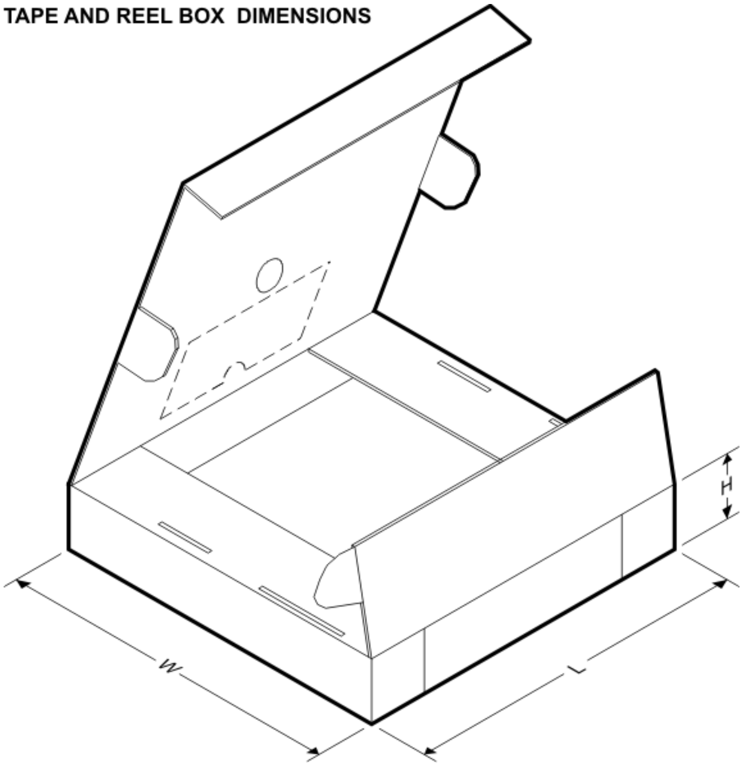


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA210AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA210AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA210AIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA210AIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA210BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210BIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA210BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA211AIDCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
INA211AIDCKT	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA211AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA211BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212AIDCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
INA212AIDCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
INA212BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA212BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA213AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA213AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA213AIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA213BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213BIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA213BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214AIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA214AIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
INA214AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214AIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214AIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214BIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214BIRSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA214BIRSWT	UQFN	RSW	10	250	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
INA215AIDCKR	SC70	DCK	6	3000	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA215AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

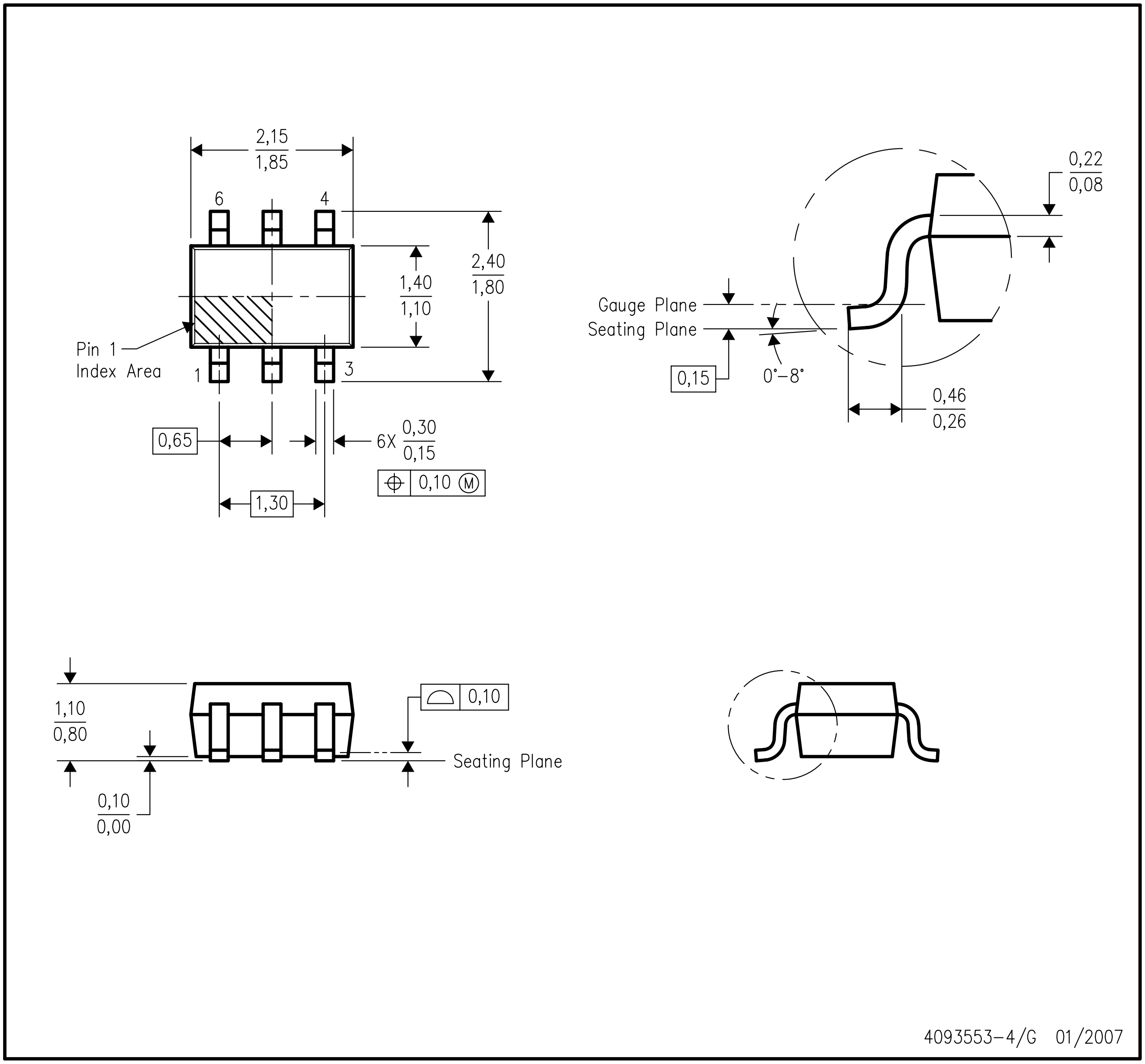


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA210AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA210AIDCKR	SC70	DCK	6	3000	195.0	200.0	45.0
INA210AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA210AIDCKT	SC70	DCK	6	250	195.0	200.0	45.0
INA210AIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA210AIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA210BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA210BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA210BIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA210BIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA211AIDCKR	SC70	DCK	6	3000	202.0	201.0	28.0
INA211AIDCKT	SC70	DCK	6	250	223.0	270.0	35.0
INA211AIDCKT	SC70	DCK	6	250	195.0	200.0	45.0
INA211BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA211BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA212AIDCKR	SC70	DCK	6	3000	202.0	201.0	28.0
INA212AIDCKT	SC70	DCK	6	250	223.0	270.0	35.0
INA212BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA212BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA213AIDCKR	SC70	DCK	6	3000	195.0	200.0	45.0

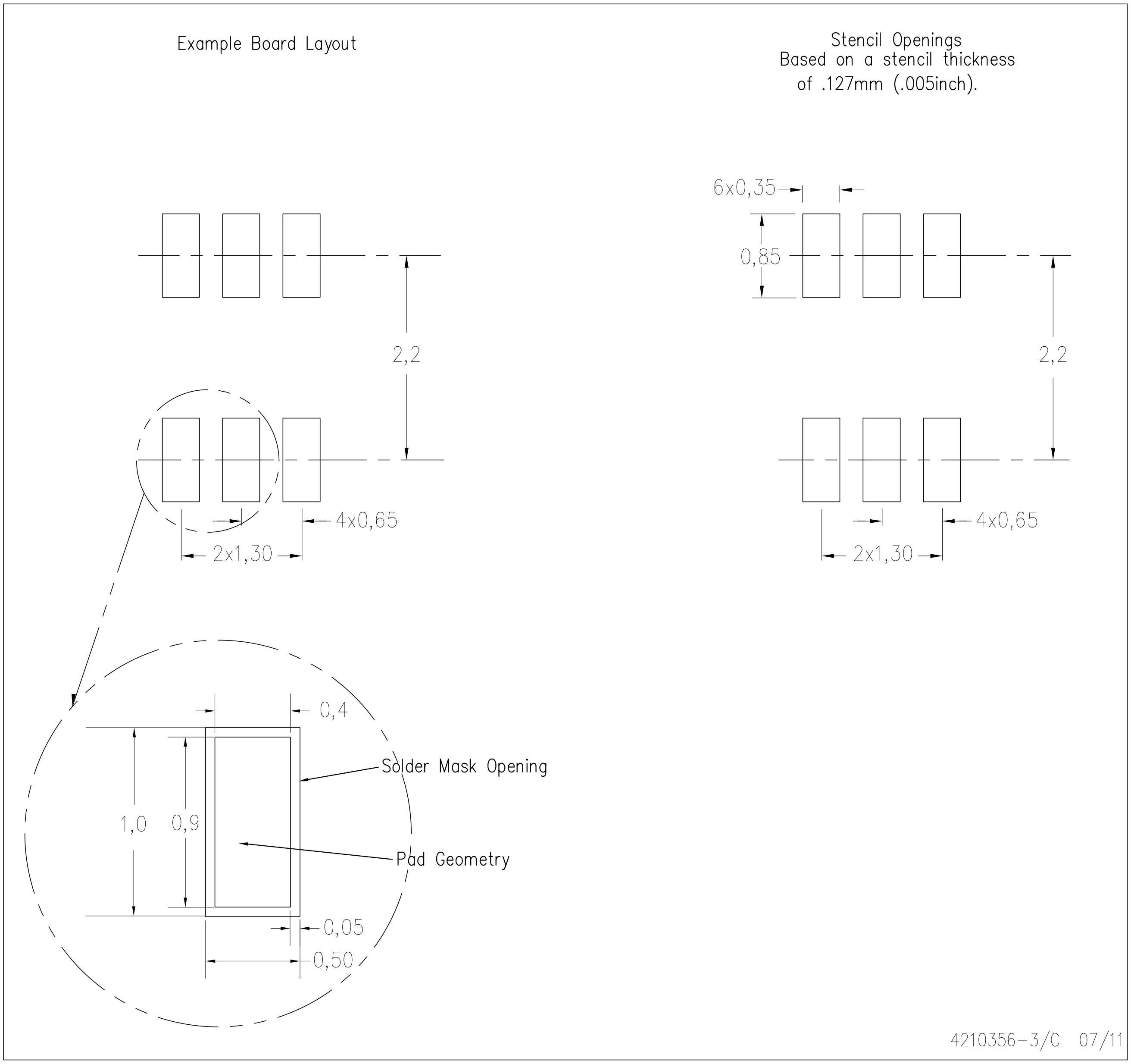
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA213AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA213AIDCKT	SC70	DCK	6	250	195.0	200.0	45.0
INA213AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA213AIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA213AIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA213BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA213BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA213BIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA213BIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA214AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA214AIDCKR	SC70	DCK	6	3000	195.0	200.0	45.0
INA214AIDCKT	SC70	DCK	6	250	195.0	200.0	45.0
INA214AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA214AIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA214AIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA214BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
INA214BIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
INA214BIRSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
INA214BIRSWT	UQFN	RSW	10	250	203.0	203.0	35.0
INA215AIDCKR	SC70	DCK	6	3000	340.0	340.0	38.0
INA215AIDCKT	SC70	DCK	6	250	340.0	340.0	38.0

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



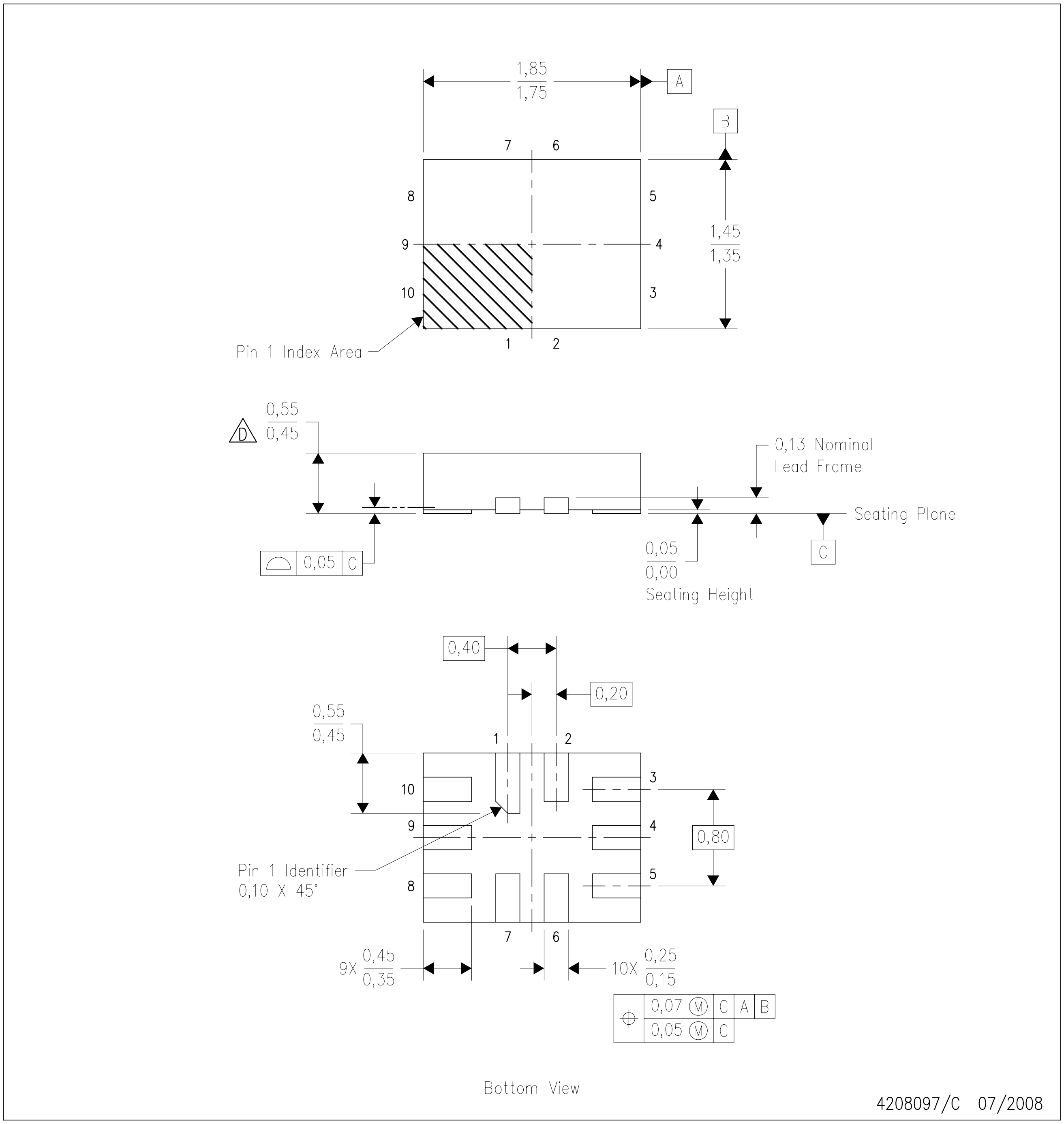
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



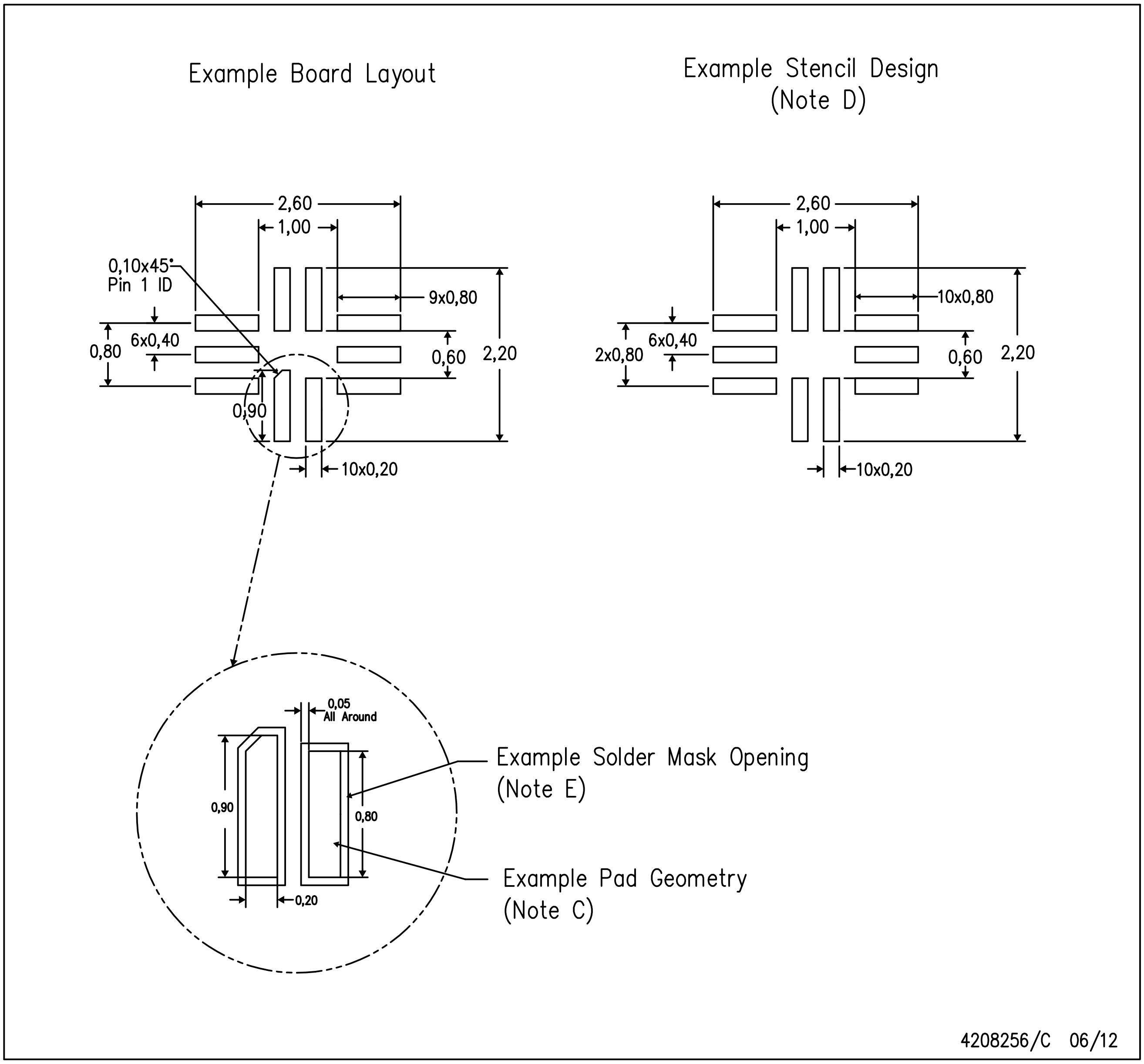
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation UDEE, except minimum package height.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.