

LMH6628

LMH6628 Dual Wideband, Low Noise, Voltage Feedback Op Amp



Literature Number: SNOSA02C

LMH6628

Dual Wideband, Low Noise, Voltage Feedback Op Amp

General Description

The National LMH6628 is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity gain stability and slew enhanced circuitry. The LMH6628's low noise and very low harmonic distortion combine to form a wide dynamic range op amp that operates from a single (5V to 12V) or dual ($\pm 5V$) power supply.

Each of the LMH6628's closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density ($2\text{nV}/\sqrt{\text{Hz}}$). Low 2nd/3rd harmonic distortion ($-65/-74\text{dBc}$ at 10MHz) make the LMH6628 a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi resolution analog-to-digital converters. Combining the LMH6628's two tightly matched amplifiers in a single 8-pin SOIC package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628 is fabricated using National's VIP10™ complimentary bipolar process.

To reduce design times and assist in board layout, the LMH6628 is supported by an evaluation board (CLC730036).

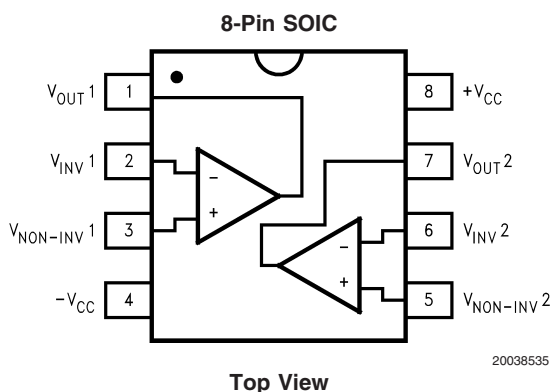
Features

- Wide unity gain bandwidth: 300MHz
- Low noise: $2\text{nV}/\sqrt{\text{Hz}}$
- Low Distortion: $-65/-74\text{dBc}$ (10MHz)
- Settling time: 12ns to 0.1%
- Wide supply voltage range: $\pm 2.5V$ to $\pm 6V$
- High output current: $\pm 85\text{mA}$
- Improved replacement for CLC428

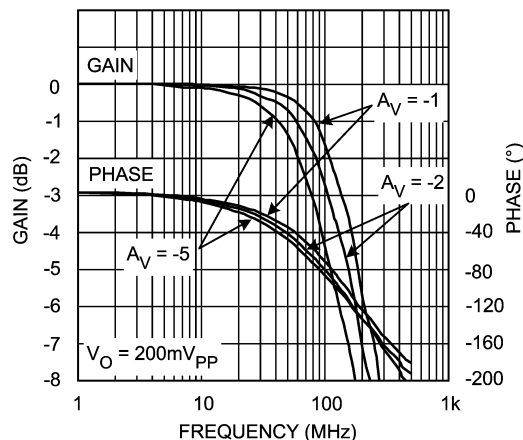
Applications

- High speed dual op amp
- Low noise integrators
- Low noise active filters
- Driver/receiver for transmission systems
- High speed detectors
- I/Q channel amplifiers

Connection Diagram



Inverting Frequency Response



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 4)

Human Body Model	2kV
Machine Model	200V
Supply Voltage	13.5
Short Circuit Current	(Note 3)
Common-Mode Input Voltage	$V^+ - V^-$
Differential Input Voltage	$V^+ - V^-$

Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10 sec)	+300°C

Operating Ratings (Note 1)

Thermal Resistance (Note 5)		
Package	(θ_{JC})	(θ_{JA})
SOIC	65°C/W	145°C/W
Temperature Range	-40°C to +85°C	
Nominal Supply Voltage	±2.5V to ±6V	

Electrical Characteristics (Note 2)

$V_{CC} = \pm 5V$, $A_V = +2V/V$, $R_F = 100\Omega$, $R_G = 100\Omega$, $R_L = 100\Omega$; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GB	Gain Bandwidth Product	$V_O < 0.5V_{PP}$		200		MHz
SSBW	-3dB Bandwidth, $A_V = +1$	$V_O < 0.5V_{PP}$	180	300		MHz
SSBW	-3dB Bandwidth, $A_V = +2$	$V_O < 0.5V_{PP}$		100		MHz
GFL	Gain Flatness	$V_O < 0.5V_{PP}$				
GFP	Peaking	DC to 200MHz		0.0		dB
GFR	Rolloff	DC to 20MHz		.1		dB
LPD	Linear Phase Deviation	DC to 20MHz		.1		deg
Time Domain Response						
TR	Rise and Fall Time	1V Step		4		ns
TS	Settling Time	2V Step to 0.1%		12		ns
OS	Overshoot	1V Step		1		%
SR	Slew Rate	4V Step	300	550		V/ μ s
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	$1V_{PP}$, 10MHz		-65		dBc
HD3	3rd Harmonic Distortion	$1V_{PP}$, 10MHz		-74		dBc
V_N	Equivalent Input Noise Voltage	1MHz to 100MHz		2		nV/ \sqrt{Hz}
	Current	1MHz to 100MHz		2		pA/ \sqrt{Hz}
XTLKA	Crosstalk	Input Referred, 10MHz		-62		dB
Static, DC Performance						
G_{OL}	Open-Loop Gain		56 53	63		dB
V_{IO}	Input Offset Voltage			$\pm .5$	± 2 ± 2.6	mV
DV_{IO}	Average Drift			5		$\mu V/^\circ C$
I_{BN}	Input Bias Current			$\pm .7$	± 20 ± 30	μA
DI_{BN}	Average Drift			150		nA/ $^\circ C$
I_{OS}	Input Offset Current			0.3	± 6	μA
I_{OSD}	Average Drift			5		nA/ $^\circ C$
PSRR	Power Supply Rejection Ratio		60 46	70		dB
CMRR	Common-Mode Rejection Ratio		57 54	62		dB
I_{CC}	Supply Current	Per Channel, $R_L = \infty$	7.5 7.0	9	12 12.5	mA

Electrical Characteristics (Note 2) (Continued)

$V_{CC} = \pm 5V$, $A_V = +2V/V$, $R_F = 100\Omega$, $R_G = 100\Omega$, $R_L = 100\Omega$; unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Miscellaneous Performance						
R_{IN}	Input Resistance	Common-Mode		500		k Ω
		Differential-Mode		200		k Ω
C_{IN}	Input Capacitance	Common-Mode		1.5		pF
		Differential-Mode		1.5		pF
R_{OUT}	Output Resistance	Closed-Loop		.1		Ω
V_O	Output Voltage Range	$R_L = \infty$		± 3.8		V
V_{OL}		$R_L = 100\Omega$	± 3.2 ± 3.1	± 3.5		V
CMIR	Input Voltage Range	Common- Mode		± 3.7		V
I_O	Output Current		± 50	± 85		mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Note 6 for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Note 3: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

Note 4: Human body model, 1.5k Ω in series with 100pF. Machine model, 0 Ω in series with 200pF.

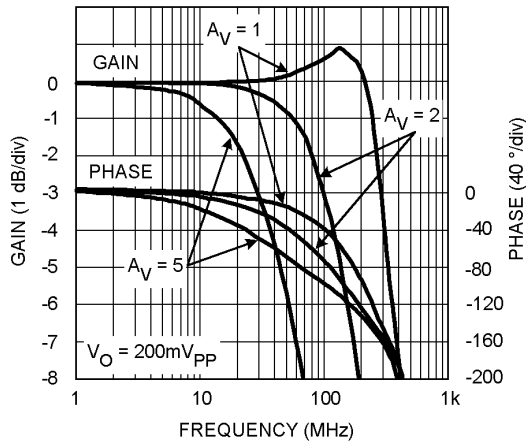
Note 5: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-pin SOIC	LMH6628MA	LMH6628MA	Rails	M08A
	LMH6628MAX		2.5k Units Tape and Reel	

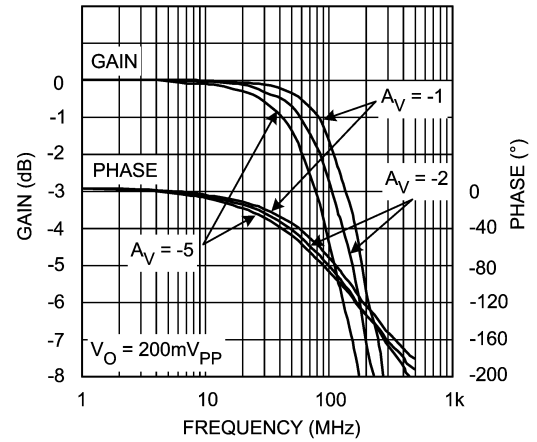
Typical Performance Characteristics ($T_A = +25^\circ$, $A_V = +2$, $V_{CC} = \pm 5V$, $R_f = 100\Omega$, $R_L = 100\Omega$, unless specified)

Non-Inverting Frequency Response



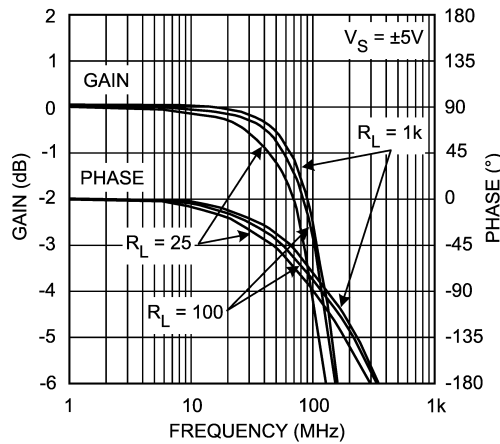
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Inverting Frequency Response



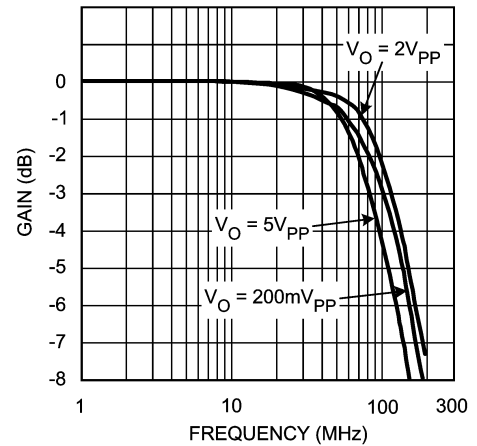
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Frequency Response vs. Load Resistance



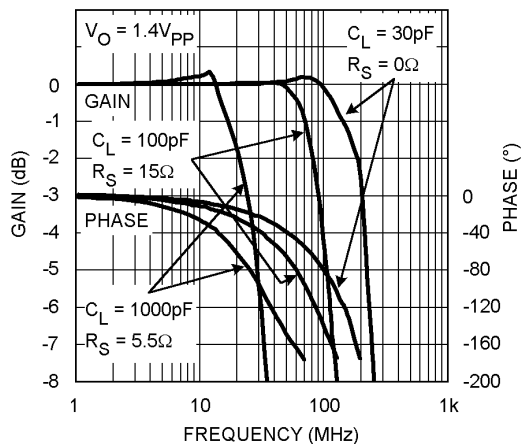
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Frequency Response vs. Output Amplitude



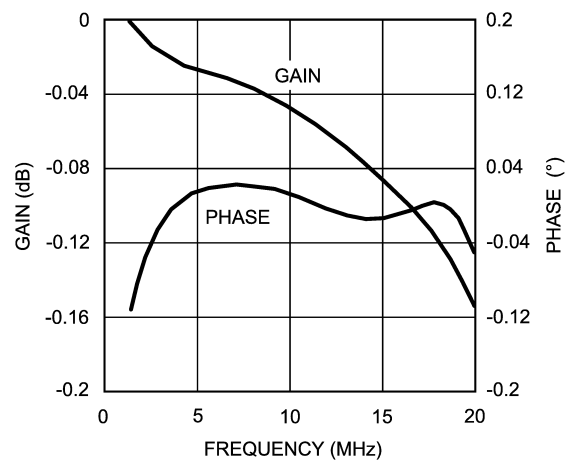
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Frequency Response vs. Capacitive Load



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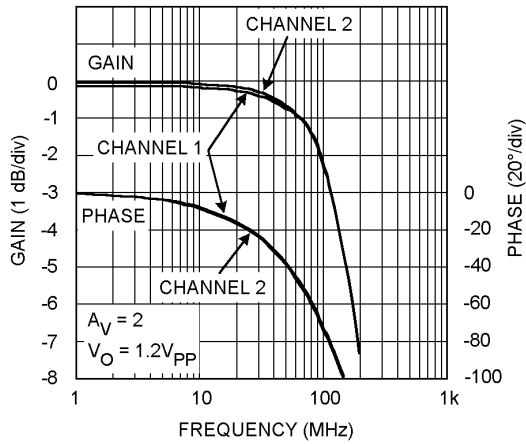
Gain Flatness & Linear Phase



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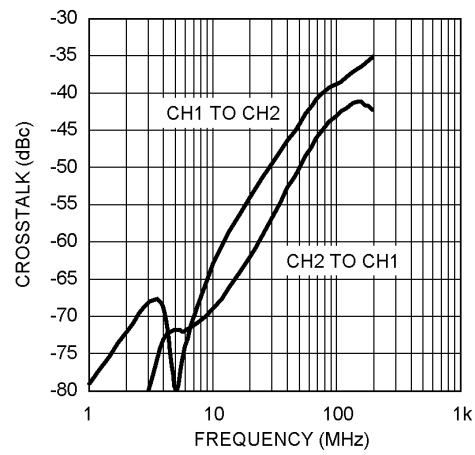
Typical Performance Characteristics $(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_f = 100\Omega, R_L = 100\Omega, \text{ unless specified})$ (Continued)

Channel Matching

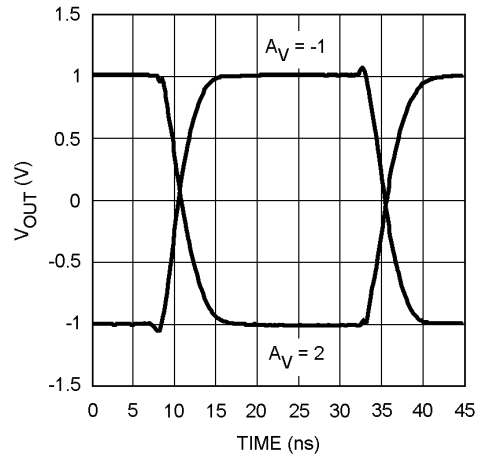


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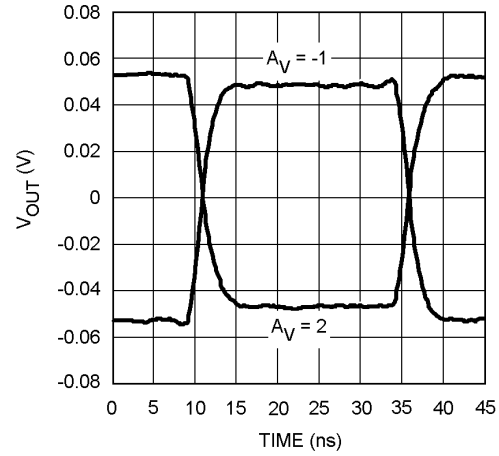
Channel to Channel Crosstalk



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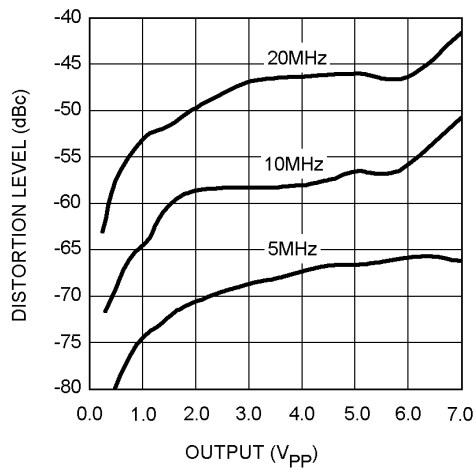
Pulse Response ($V_O = 2V$)

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Pulse Response ($V_O = 100mV$)

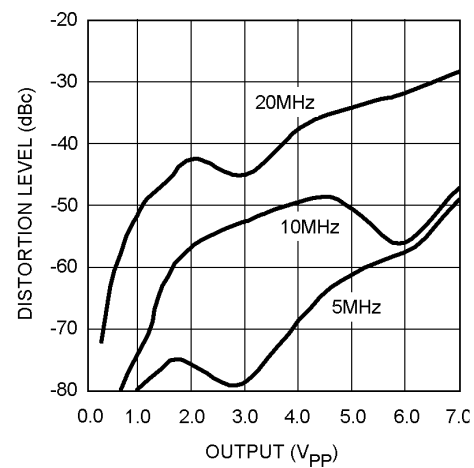
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2nd Harmonic Distortion vs. Output Voltage



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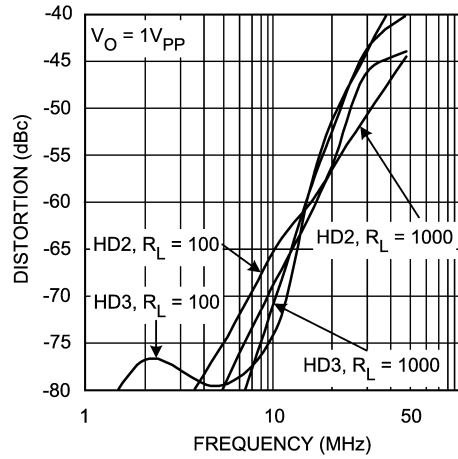
3rd Harmonic Distortion vs. Output Voltage



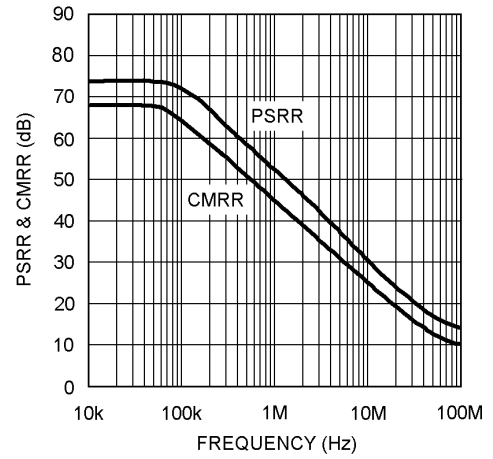
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Typical Performance Characteristics ($T_A = +25^\circ$, $A_V = +2$, $V_{CC} = \pm 5V$, $R_f = 100\Omega$, $R_L = 100\Omega$, unless specified) (Continued)

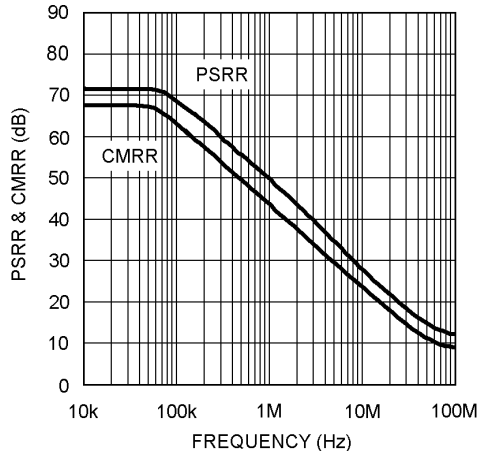
2nd & 3rd Harmonic Distortion vs. Frequency



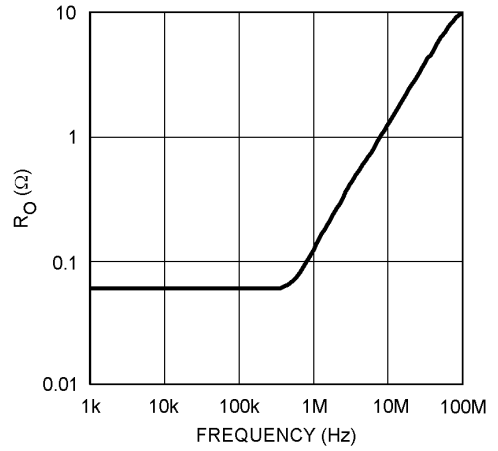
PSRR and CMRR ($\pm 5V$)



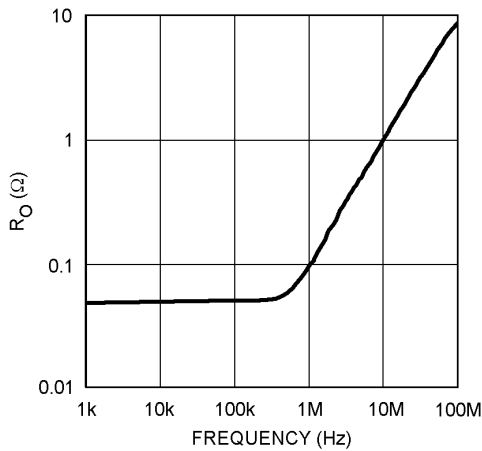
PSRR and CMRR ($\pm 2.5V$)



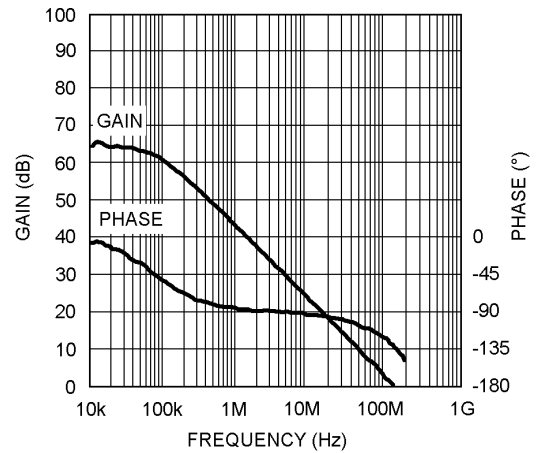
Closed Loop Output Resistance ($\pm 2.5V$)



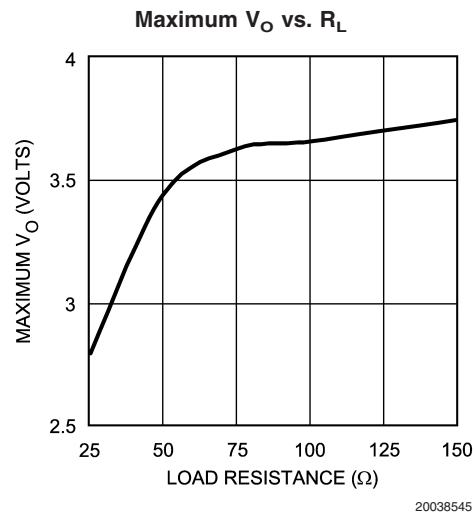
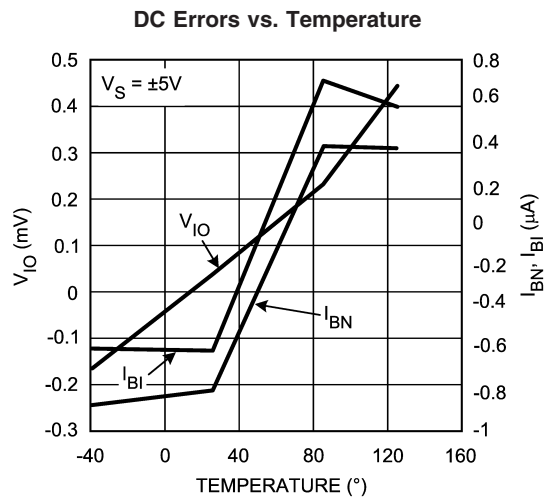
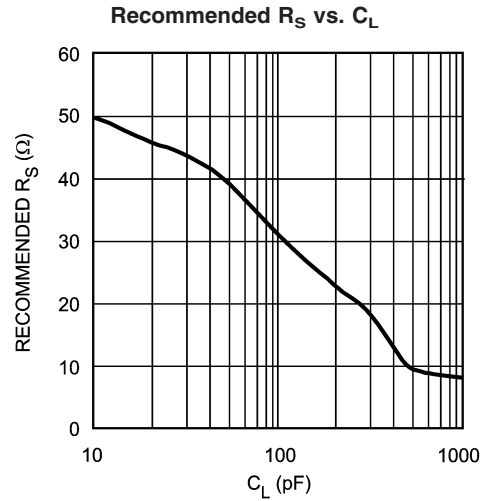
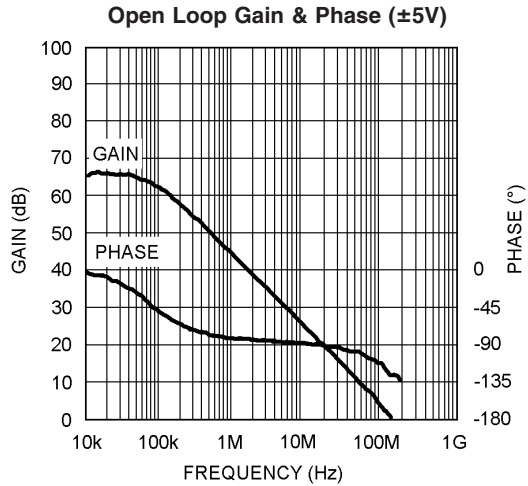
Closed Loop Output Resistance ($\pm 5V$)



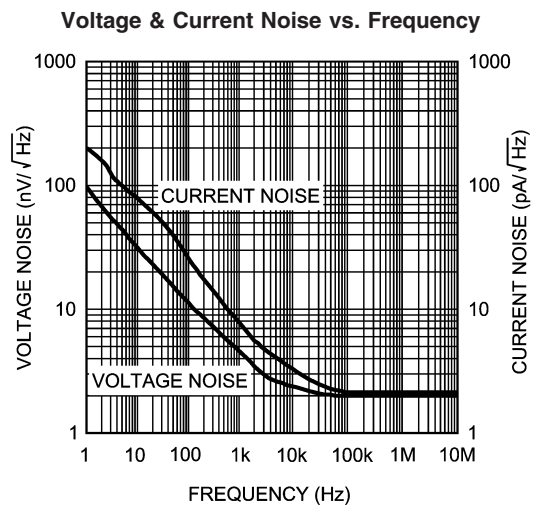
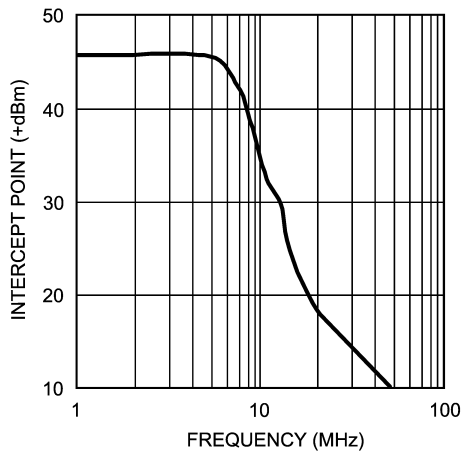
Open Loop Gain & Phase ($\pm 2.5V$)



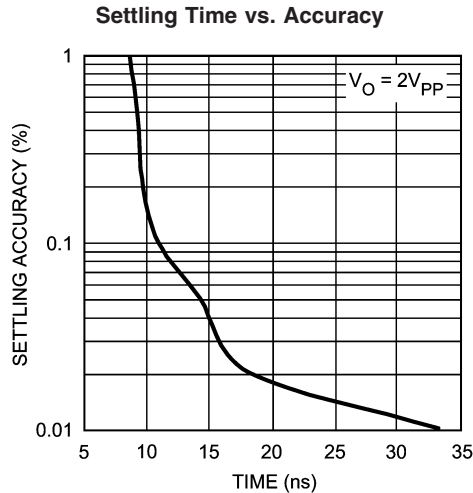
Typical Performance Characteristics $(T_A = +25^\circ, A_V = +2, V_{CC} = \pm 5V, R_f = 100\Omega, R_L = 100\Omega, \text{ unless specified})$ (Continued)



2-Tone, 3rd Order Intermodulation Intercept



Typical Performance Characteristics ($T_A = +25^\circ$, $A_V = +2$, $V_{CC} = \pm 5V$, $R_f = 100\Omega$, $R_L = 100\Omega$, unless specified) (Continued)



20038548

Application Section

LOW NOISE DESIGN

Ultimate low noise performance from circuit designs using the LMH6628 requires the proper selection of external resistors. By selecting appropriate low valued resistors for R_f and R_G , amplifier circuits using the LMH6628 can achieve output noise that is approximately the equivalent voltage input noise of $2nV/\sqrt{Hz}$ multiplied by the desired gain (A_V).

DC BIAS CURRENTS AND OFFSET VOLTAGES

Cancellation of the output offset voltage due to input bias currents is possible with the LMH6628. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (V_{OS}) multiplied by the desired gain (A_V). National Application Note OA-7 offers several solutions to further reduce the output offset.

OUTPUT AND SUPPLY CONSIDERATIONS

With $\pm 5V$ supplies, the LMH6628 is capable of a typical output swing of $\pm 3.8V$ under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω , the output swing will be limited by the LMH6628's output current capability, typically 85mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled " R_S vs. C_L " in the Typical Performance section.

LAYOUT

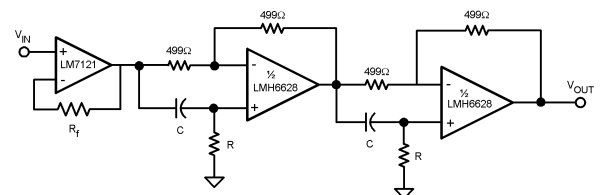
Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of $0.1\mu F$ should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation.

See OA-15 for more information. National suggests the 730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

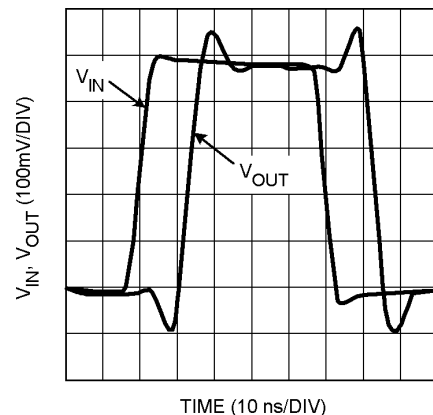
ANALOG DELAY CIRCUIT (ALL-PASS NETWORK)

The circuit in *Figure 1* implements an all-pass network using the LMH6628. A wide bandwidth buffer (LM7121) drives the circuit and provides a high input impedance for the source. As shown in *Figure 2*, the circuit provides a 13.1ns delay (with $R = 40.2\Omega$, $C = 47pF$). R_f and R_G should be of equal and low value for parasitic insensitive operation.



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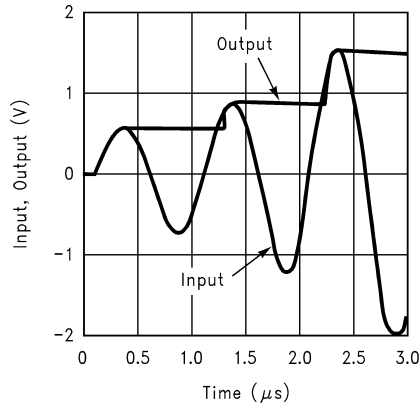
FIGURE 1.



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FIGURE 2. Delay Circuit Response to 0.5V Pulse

Application Section (Continued)



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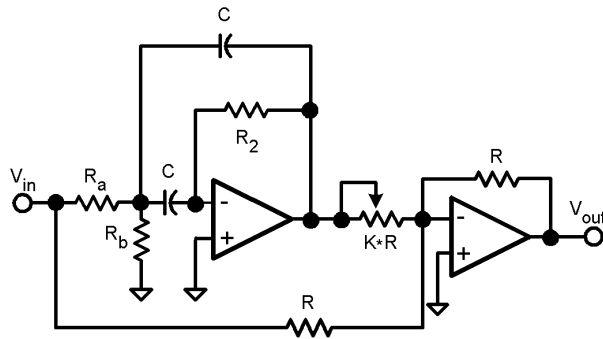
FIGURE 6.

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when V_{IN} is less than V_C . A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

ADJUSTABLE OR BANDPASS EQUALIZER

A "boost" equalizer can be made with the LMH6628 by summing a bandpass response with the input signal, as shown in Figure 7.



20038506

FIGURE 7.

The overall transfer function is shown in Eq. 5.

$$\frac{V_{out}}{V_{in}} = \left[\frac{R_b}{K(R_a + R_b)} \right] \frac{s2Q\omega_o}{s^2 + s \frac{\omega_o}{Q} + \omega_o^2} - 1 \quad (4)$$

To build a boost circuit, use the design equations Eq. 6 and Eq. 7.

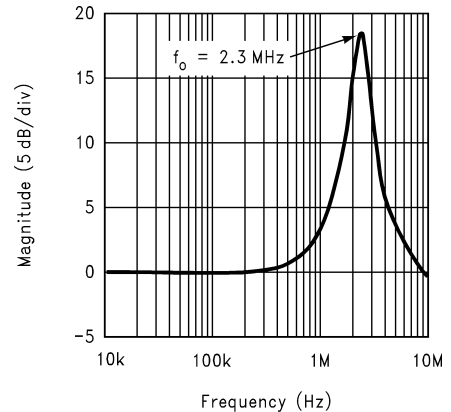
$$\frac{R_2 C}{2} = \frac{Q}{\omega_o} \quad (5)$$

$$2C(R_a \parallel R_b) = \frac{1}{Q\omega_o} \quad (6)$$

Select R_2 and C using Eq. 6. Use reasonable values for high frequency circuits - R_2 between 10Ω and $5k\Omega$, C between $10pF$ and $2000pF$. Use Eq. 7 to determine the parallel combination of R_a and R_b . Select R_a and R_b by either the 10Ω to $5k\Omega$ criteria or by other requirements based on the impedance V_{in} is capable of driving. Finish the design by determining the value of K from Eq. 8.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}}(\omega_o) = \frac{R_2}{2KR_a} - 1 \quad (7)$$

Figure 8 shows an example of the response of the circuit of Figure 9, where f_o is $2.3MHz$. The component values are as follows: $R_a=2.1k\Omega$, $R_b=68.5\Omega$, $R_2=4.22k\Omega$, $R=500\Omega$, $KR=50\Omega$, $C=120pF$.

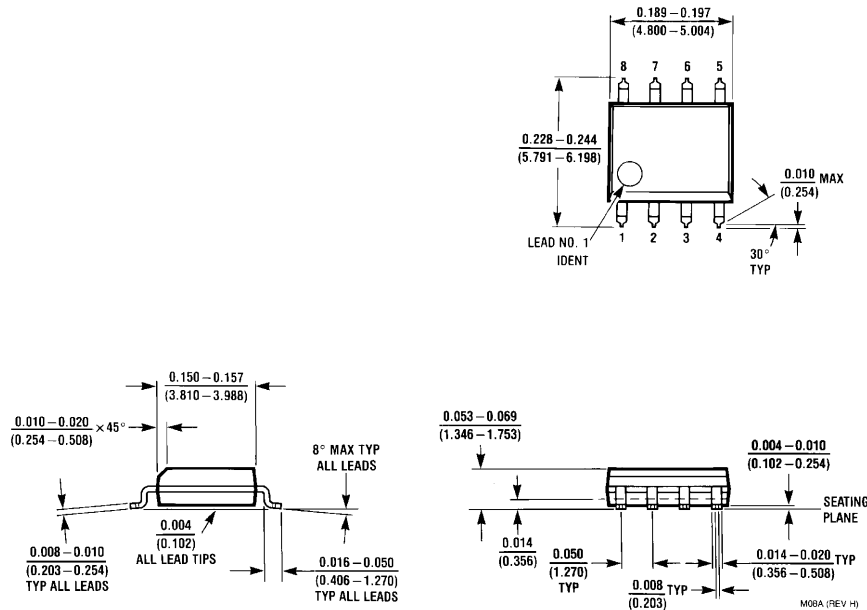


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FIGURE 8.

Physical Dimensions inches (millimeters)

unless otherwise noted



8-Pin SOIC
NS Package Number M08A

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