±1°C Temperature Sensor with Series-R, η-Factor, and Automatic Beta Compensation

Check for Samples: TMP431, TMP432

FEATURES

- **±1°C REMOTE DIODE SENSOR**
- **±1°C LOCAL TEMPERATURE SENSOR**
- **AUTOMATIC BETA COMPENSATION**
- **η-FACTOR CORRECTION**
- **PROGRAMMABLE THRESHOLD LIMITS**
- **TWO-WIRE/ SMBus™ SERIAL INTERFACE**
- **MINIMUM AND MAXIMUM TEMPERATURE MONITORS**
- **MULTIPLE INTERFACE ADDRESSES**
- **$\overline{\text{ALERT}}/\overline{\text{THERM2}}$ PIN CONFIGURATION**
- **DIODE FAULT DETECTION**

APPLICATIONS

- **LCD/DLP®/LCOS PROJECTORS**
- **SERVERS**
- **INDUSTRIAL CONTROLLERS**
- **CENTRAL OFFICE TELECOM EQUIPMENT**
- **DESKTOP AND NOTEBOOK COMPUTERS**
- **STORAGE AREA NETWORKS (SAN)**
- **INDUSTRIAL AND MEDICAL EQUIPMENT**
- **PROCESSOR/FPGA TEMPERATURE MONITORING**

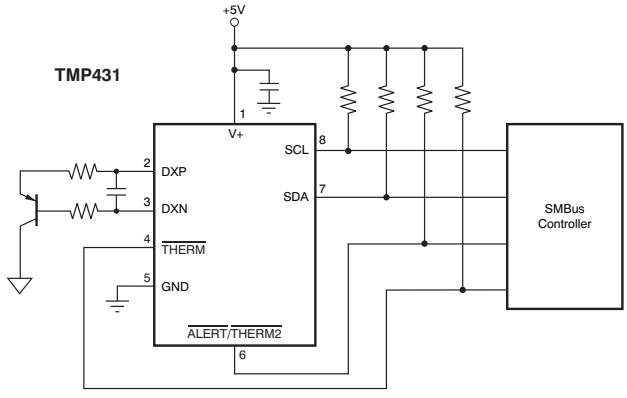
DESCRIPTION

The TMP431 and TMP432 are remote temperature sensor monitors with a built-in local temperature sensor. The remote temperature sensor diode-connected transistors are typically low-cost, NPN- or PNP-type transistors or diodes that are an integral part of microcontrollers, microprocessors, or FPGAs.

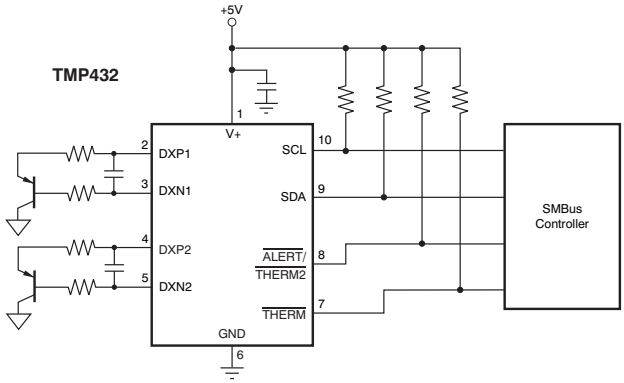
Remote accuracy is ±1°C for multiple IC manufacturers, with no calibration needed. The Two-Wire serial interface accepts SMBus write byte, read byte, send byte, and receive byte commands to program the alarm thresholds and to read temperature data.

The TMP431/32 include beta compensation (correction), series resistance cancellation, programmable non-ideality factor, programmable resolution, programmable threshold limits, minimum and maximum temperature monitors, wide remote temperature measurement range (up to +150°C), and diode fault detection and temperature alert function.

The TMP431 is available in a VSSOP-8 package and the TMP432 is available in a VSSOP-10 package.



One Channel Local
One Channel Remote



One Channel Local
Two Channels Remote

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	TWO-WIRE ADDRESS	THERM HIGH LIMIT
TMP431A	100 1100	+85°C
TMP431B	100 1101	+85°C
TMP431C	100 1100	+105°C
TMP431D	100 1101	+105°C
TMP432A	100 1100	+85°C
TMP432B	100 1101	+85°C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Power Supply, V_S		+7.0	V
TMP431 Input Voltage	Pins 2, 3, and 6 only	–0.5 to V_S + 0.5	V
	Pins 4, 7, and 8 only	–0.5 to 7	V
TMP432 Input Voltage	Pins 2, 3, 4, 5, and 8 only	–0.5 to V_S + 0.5	V
	Pins 7, 9, and 10 only	–0.5 to 7	V
Input Current		10	mA
Operating Temperature Range		–55 to +127	°C
Storage Temperature Range		–60 to +130	°C
Junction Temperature (T_J max)		+150	°C
ESD Rating	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C and V_S = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		CONDITIONS	TMP431 TMP432 MIN	TYP	MAX	UNIT
TEMPERATURE ERROR						
Local Temperature Sensor	TE_{LOCAL}	T_A = –40°C to +125°C		±1.25	±2.5	°C
		T_A = +0°C to +100°C, V_S = 3.3V		±0.25	±1	°C
Remote Temperature Sensor(1)	TE_{REMOTE}	T_A = 0°C to +100°C, T_{DIODE} = –40°C to +150°C, V_S = 3.3V		±0.25	±1	°C
		T_A = –40°C to +100°C, T_{DIODE} = –40°C to +150°C, V_S = 3.3V		±0.5	±1.5	°C
		T_A = –40°C to +125°C, T_{DIODE} = –40°C to +150°C		±3	±5	°C
vs Supply (Local/Remote)		V_S = 2.7V to 5.5V		±0.2	±0.5	°C/V
TEMPERATURE MEASUREMENT						
Conversion Time (per channel)						
Local Channel			12	15	17	ms
Remote Channel						
Beta Correction Enabled (2)		RC = 1	97	126	137	ms
		RC = 0	36	47	52	ms
Beta Correction Disabled (3)		RC = 1	72	93	100	ms
		RC = 0	33	44	47	ms
Resolution						
Local Channel				12		Bits
Remote Channel				12		Bits
Remote Sensor Source Currents						
High		Series Resistance (beta correction) (4)		120		µA
Medium High				60		µA
Medium Low				12		µA
Low				6		µA
Remote Transistor Ideality Factor	η	TMP431/32 optimized ideality factor		1.000(2)		
				1.008(3)		
Beta Correction Range	β		0.1		27	
SMBus INTERFACE						
Logic Input High Voltage (SCL, SDA)	V_{IH}		2.1			V
Logic Input Low Voltage (SCL, SDA)	V_{IL}				0.8	V
Hysteresis				500		mV
SMBus Output Low Sink Current			6			mA
SDA Output Low Voltage	V_{OL}	I_{OUT} = 6mA		0.15	0.4	V
Logic Input Current		0 ≤ V_{IN} ≤ 6V	–1		+1	µA
SMBus Input Capacitance (SCL, SDA)				3		pF
SMBus Clock Frequency					3.4	MHz
SMBus Timeout			25	32	35	ms
SCL Falling Edge to SDA Valid Time					1	µs
DIGITAL OUTPUTS						
Output Low Voltage	V_{OL}	I_{OUT} = 6mA		0.15	0.4	V
High-Level Output Leakage Current	I_{OH}	V_{OUT} = V_S		0.1	1	µA
$\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ Output Low Sink Current		$\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ Forced to 0.4V	6			mA
$\overline{\text{THERM}}$ Output Low Sink Current		$\overline{\text{THERM2}}$ Forced to 0.4V	6			mA

(1) Tested with less than 5Ω effective series resistance and 100pF differential input capacitance. T_A is the ambient temperature of the TMP431/32. T_{DIODE} is the temperature at the remote diode sensor.
(2) Beta correction configuration set to '1000' and sensor is GND collector-connected (PNP collector to ground).
(3) Beta correction configuration set to '0111' or sensor is diode-connected (base shorted to collector).
(4) If beta correction is disabled ('0111'), then up to 1kΩ of series line resistance is cancelled; if beta correction is enabled ('1xxx'), up to 300Ω is cancelled.

ELECTRICAL CHARACTERISTICS (continued)

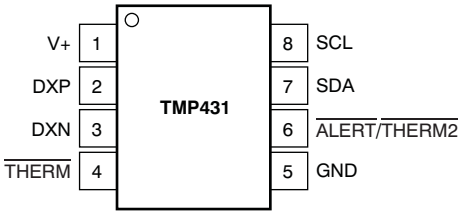
At T_A = –40°C to +125°C and V_S = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		CONDITIONS	TMP431 TMP432			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
Specified Voltage Range	V_S		2.7		5.5	V
Quiescent Current	I_Q	0.0625 Conversions per Second, V_S = 3.3V		35	45	µA
		Eight Conversions per Second, V_S = 3.3V(5)		0.7	1	mA
		Serial Bus Inactive, Shutdown Mode		3	10	µA
		Serial Bus Active, f_S = 400kHz, Shutdown Mode		90		µA
		Serial Bus Active, f_S = 3.4MHz, Shutdown Mode		350		µA
Undervoltage Lockout	UVLO		2.3	2.4	2.6	V
Power-On Reset Threshold	POR			1.6	2.3	V
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Storage Range			–60		+130	°C
Thermal Resistance						
VSSOP-8	θ_{JA}			215		°C/W
VSSOP-10	θ_{JA}			165		°C/W

(5) Beta correction disabled.

PIN CONFIGURATIONS

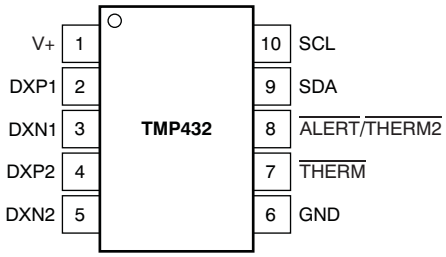
DGK PACKAGE
VSSOP-8
(TOP VIEW)



TMP431 PIN ASSIGNMENTS

TMP431		
NO.	**NAME**	**DESCRIPTION**
1	V+	Positive supply (2.7V to 5.5V)
2	DXP	Positive connection to remote temperature sensor
3	DXN	Negative connection to remote temperature sensor
4	$\overline{\text{THERM}}$	Thermal flag, active low, open-drain; requires pull-up resistor to V+
5	GND	Ground
6	$\overline{\text{ALERT}}/\overline{\text{THERM2}}$	Alert (reconfigurable as second thermal flag), active low, open-drain; requires pull-up resistor to V+
7	SDA	Serial data line for SMBus, open-drain; requires pull-up resistor to V+
8	SCL	Serial clock line for SMBus, open-drain; requires pull-up resistor to V+

DGS PACKAGE
VSSOP-10
(TOP VIEW)



TMP432 PIN ASSIGNMENTS

TMP432		
NO.	**NAME**	**DESCRIPTION**
1	V+	Positive supply (2.7V to 5.5V)
2	DXP1	Channel 1 positive connection to remote temperature sensor
3	DXN1	Channel 1 negative connection to remote temperature sensor
4	DXP2	Channel 2 positive connection to remote temperature sensor
5	DXN2	Channel 2 negative connection to remote temperature sensor
6	GND	Ground
7	$\overline{\text{THERM}}$	Thermal flag, active low, open-drain; requires pull-up resistor to V+
8	$\overline{\text{ALERT}}/\overline{\text{THERM2}}$	Alert (reconfigurable as second thermal flag), active low, open-drain; requires pull-up resistor to V+
9	SDA	Serial data line for SMBus, open-drain; requires pull-up resistor to V+
10	SCL	Serial clock line for SMBus, open-drain; requires pull-up resistor to V+

TYPICAL CHARACTERISTICS

At T_A = +25°C and V_S = 3.3V, unless otherwise noted.

REMOTE TEMPERATURE ERROR vs TEMPERATURE

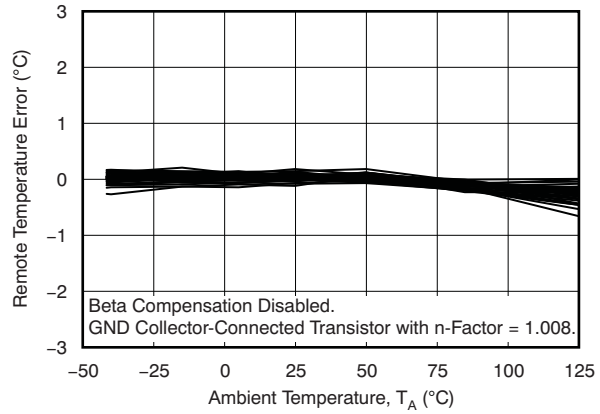


Figure 1.

LOCAL TEMPERATURE ERROR vs TEMPERATURE

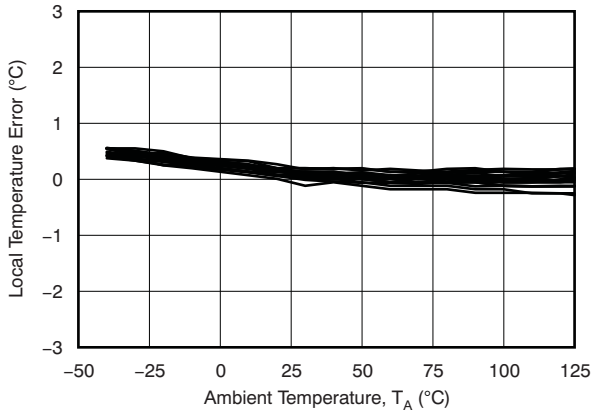


Figure 2.

REMOTE TEMPERATURE ERROR vs LEAKAGE RESITANCE

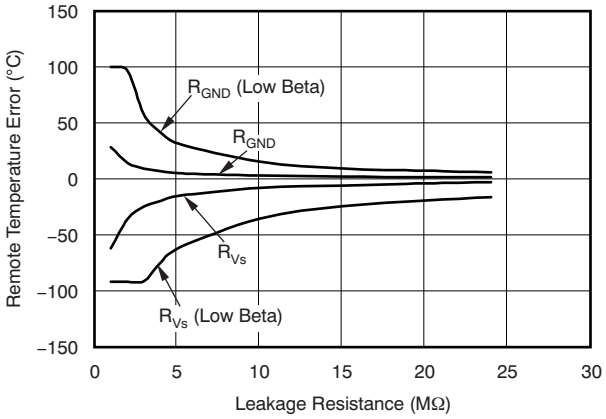


Figure 3.

QUIESCENT CURRENT vs CONVERSION RATE

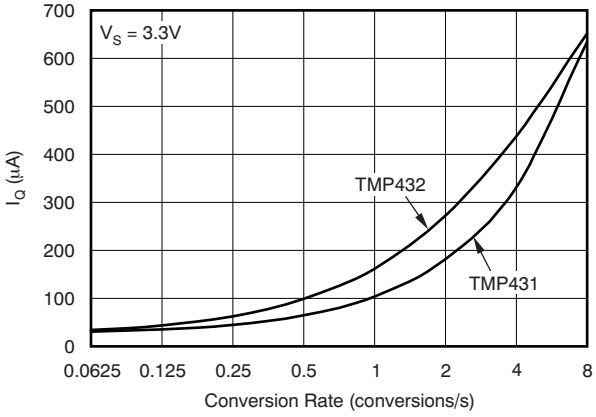


Figure 4.

SHUTDOWN QUIESCENT CURRENT vs SCL CLOCK FREQUENCY

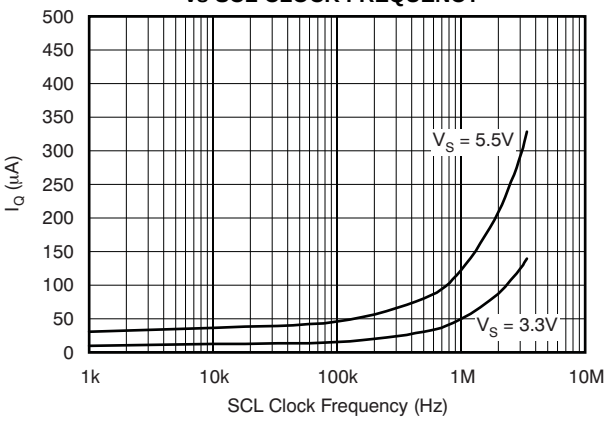


Figure 5.

SHUTDOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

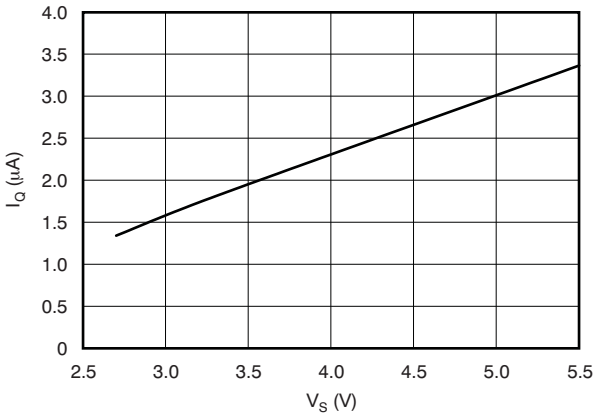


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_S = 3.3V, unless otherwise noted.

REMOTE TEMPERATURE ERROR vs SERIES RESISTANCE

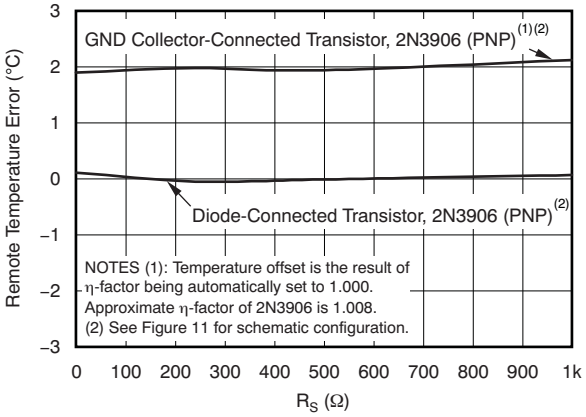


Figure 7.

REMOTE TEMPERATURE ERROR vs SERIES RESISTANCE (Low-Beta Transistor)

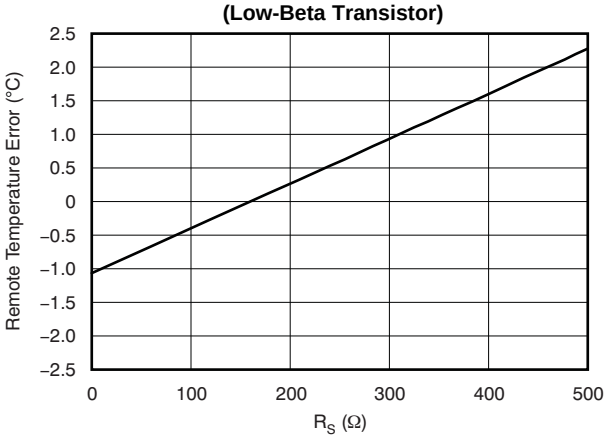


Figure 8.

REMOTE TEMPERATURE ERROR vs DIFFERENTIAL CAPACITANCE AT +25°C, V_{CC} = 3.3V, R_S = 0Ω

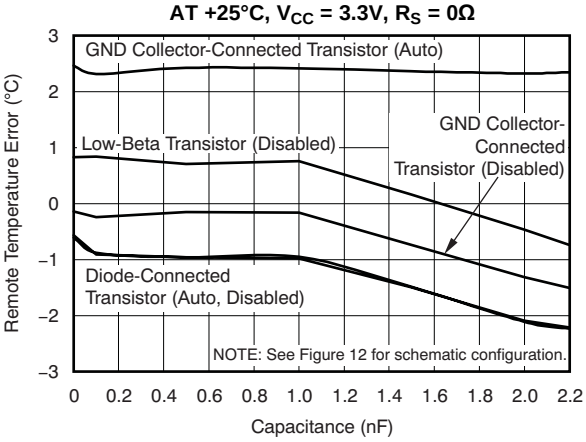


Figure 9.

REMOTE TEMPERATURE ERROR vs DIFFERENTIAL CAPACITANCE with 45nm CPU AT +25°C, V_{CC} = 3.3V, R_S = 0Ω, Beta = 011 (AUTO)

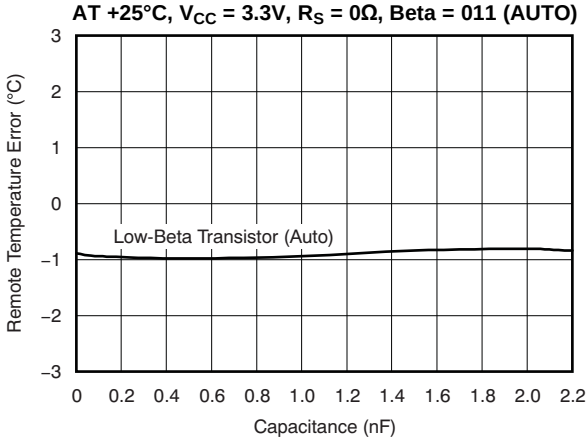
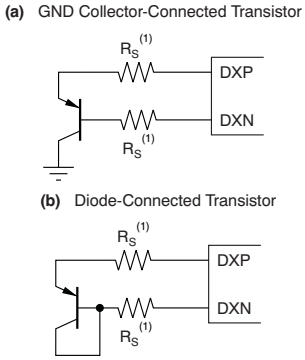


Figure 10.

PARAMETRIC MEASUREMENT INFORMATION

TYPICAL CONNECTIONS

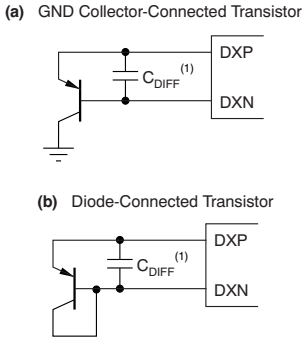
Figure 11. SERIES RESISTANCE CONFIGURATION



(1) R_S should be less than 1kΩ; see *Filtering* section.

Figure 12.

Figure 13. DIFFERENTIAL CAPACITANCE CONFIGURATION



(1) C_{DIFF} should be less than 2200pF; see *Filtering* section.

Figure 14.

APPLICATION INFORMATION

The TMP431 (two-channel) and TMP432 (three-channel) are digital temperature sensors that combine a local die temperature measurement channel and a remote junction temperature measurement channel in a single VSSOP-8 (TMP431) or VSSOP-10 (TMP432) package. They are Two-Wire- and SMBus interface-compatible and are specified over a temperature range of –40°C to +125°C. The TMP431/32 contain multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum/minimum limits, and status information. User-programmed high and low temperature limits stored in the TMP431/32 can be used to trigger an over/under temperature alarm ($\overline{\text{ALERT}}$) on local and remote temperatures. Additional thermal limits can be programmed into the TMP431/32 and used to trigger another flag ($\overline{\text{THERM}}$) that can be used to initiate a system response to rising temperatures.

For proper remote temperature sensing operation, the TMP431 requires only a transistor connected between DXP and DXN; the TMP432 requires transistors conncected between DXP1 and DXN1, and between DXP2 and DXN2.

The SCL and SDA interface pins require pull-up resistors as part of the communication bus, while $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ are open-drain outputs that also need pull-up resistors. $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ may be shared with other devices if desired for a wired-OR implementation. A 0.1µF power-supply bypass capacitor is recommended for good local bypassing. See Figure 15 for a typical configuration of the TMP431; see Figure 16 for a typical configuration of the TMP432.

BETA COMPENSATION

Previous generations of remote junction temperature sensors were operated by controlling the emitter current of the sensing transistor. However, examination of the physics of a transistor shows that V_{BE} is actually a function of the collector current. If beta is independent of the collector current, then V_{BE} may be calculated from the emitter current. In earlier generations of processors that contained PNP transistors connected to these temperature sensors, controlling the emitter current provided acceptable temperature measurement results. At 90nm process geometry and below, however, the beta factor continues to decrease and the premise that it is independent of collector current becomes less certain.

To manage this increasing temperature measurement error, the TMP431/32 control the collector current instead of the emitter current. The TMP431/32 automatically detect and choose the correct range depending on the beta factor of the external transistor. This auto-ranging is performed at the beginning of each temperature conversion in order to correct for any changes in the beta factor as a result of temperature variation. The device can operate a PNP transistor with a beta factor as low as 0.1. See the *Beta Compensation Configuration Register* section for further information.

SERIES RESISTANCE CANCELLATION

Series resistance in an application circuit that typically results from printed circuit board (PCB) trace resistance and remote line length is automatically cancelled by the TMP431/32, preventing what would otherwise result in a temperature offset. A total of up to 1kΩ of series line resistance is cancelled by the TMP431/32 if beta correction is disabled and up to 300Ω of series line resistance is cancelled if beta correction is enabled, eliminating the need for additional characterization and temperature offset correction. See the two *Remote Temperature Error vs Series Resistance* typical characteristic curves (Figure 7 and Figure 8) for details on the effects of series resistance on sensed remote temperature error.

DIFFERENTIAL INPUT CAPACITANCE

The TMP431/32 can tolerate differential input capacitance of up to 2200pF with minimal change in temperature error. The effect of capacitance on sensed remote temperature error is illustrated in Figure 9 and Figure 10, *Remote Temperature Error vs Differential Capacitance*. See the *Filtering* section for suggested component values where filtering unwanted coupled signals is needed.

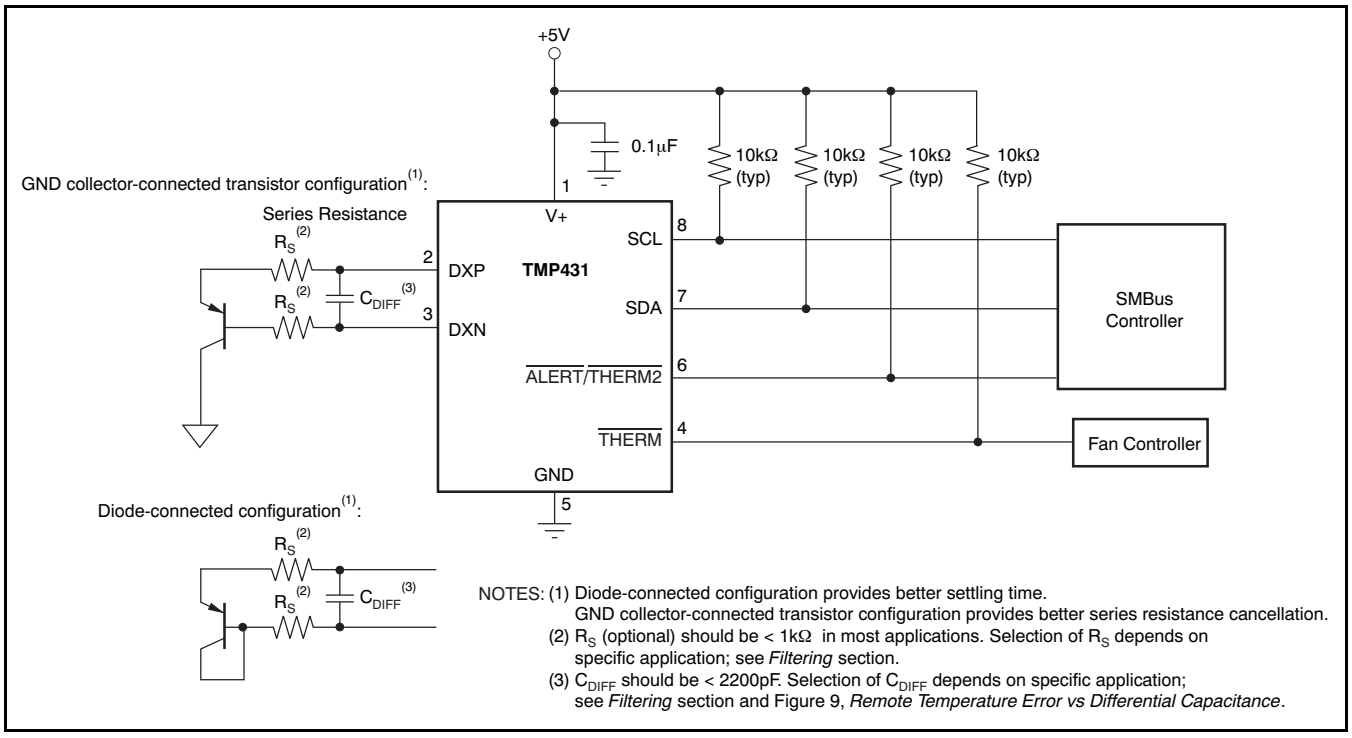


Figure 15. TMP431 Basic Connections

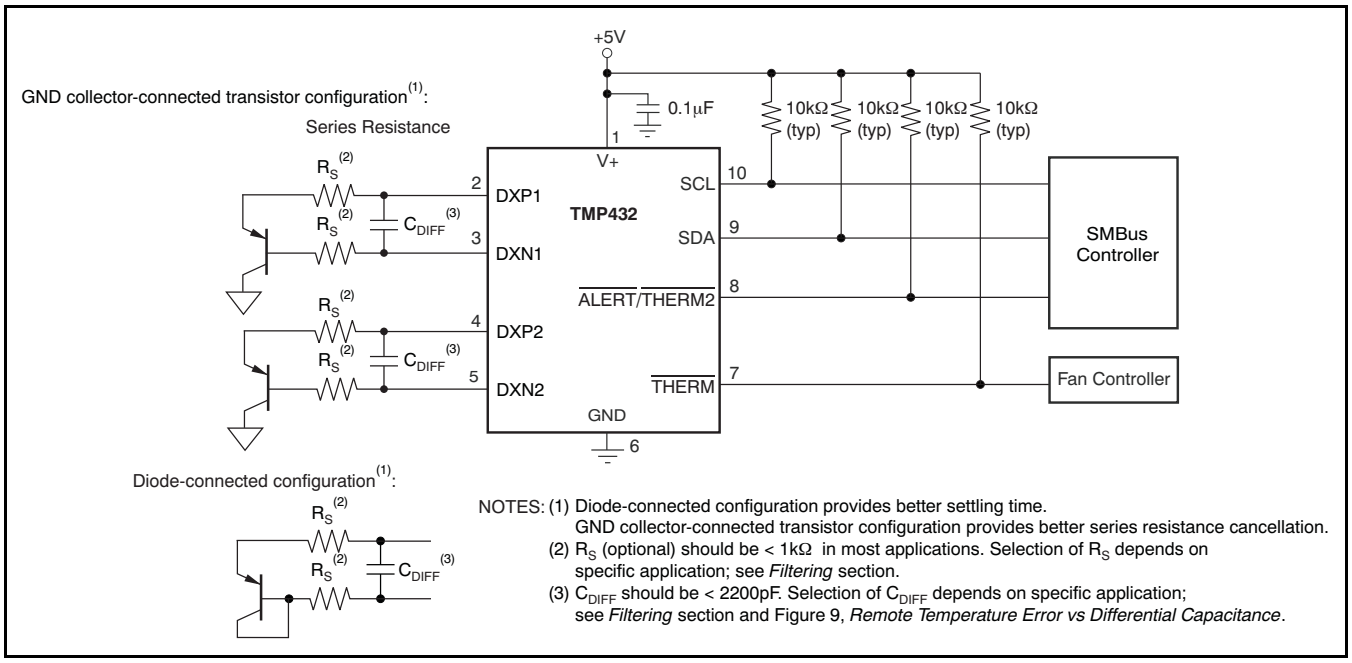


Figure 16. TMP432 Basic Connections

TEMPERATURE MEASUREMENT DATA

Temperature measurement data are taken over a default range of 0°C to +127°C for both local and remote locations. However, measurements from –55°C to +150°C can be made both locally and remotely by reconfiguring the TMP431/32 for the extended temperature range, as described in this section. Temperature data resulting from conversions within the default measurement range are represented in binary form, as shown in Table 1, *Standard Binary* column. Note that any temperature below 0°C results in a data value of zero (00h). Likewise, temperatures above +127°C result in a value of 127 (7Fh). The device can be set to measure over an extended temperature range by changing bit 2 of Configuration Register 1 from low to high. The change in measurement range and data format from standard binary to extended binary occurs at the next temperature conversion.

For data captured in the extended temperature range configuration, an offset of 64 (40h) is added to the standard binary value, as shown in Table 1, *Extended Binary* column. This configuration allows measurement of temperatures as low as –64°C, and as high as +191°C; however, most temperature-sensing diodes only measure with the range of –55°C to +150°C.

Additionally, the TMP431/32 are rated only for ambient local temperatures ranging from –40°C to +125°C. Parameters in the Absolute Maximum Ratings table must be observed.

Both local and remote temperature data use two bytes for data storage. The high byte stores the temperature with 1°C resolution. The second or low byte stores the decimal fraction value of the temperature and allows a higher measurement resolution, as shown in Table 2.

The measurement resolution for both the local and remote channels is 0.0625°C, and cannot be adjusted.

Table 1. Temperature Data Format (Local and Remote Temperature High Bytes)

	LOCAL/REMOTE TEMPERATURE REGISTER HIGH BYTE VALUE (+1°C RESOLUTION)			
	STANDARD BINARY(1)		EXTENDED BINARY(2)	
TEMP (°C)	BINARY	HEX	BINARY	HEX
−64	0000 0000	00	0000 0000	00
−50	0000 0000	00	0000 1110	0E
−25	0000 0000	00	0010 0111	27
0	0000 0000	00	0100 0000	40
1	0000 0001	01	0100 0001	41
5	0000 0101	05	0100 0101	45
10	0000 1010	0A	0100 1010	4A
25	0001 1001	19	0101 1001	59
50	0011 0010	32	0111 0010	72
75	0100 1011	4B	1000 1011	8B
100	0110 0100	64	1010 0100	A4
125	0111 1101	7D	1011 1101	BD
127	0111 1111	7F	1011 1111	BF
150	0111 1111	7F	1101 0110	D6
175	0111 1111	7F	1110 1111	EF
191	0111 1111	7F	1111 1111	FF

(1) Resolution is 1°C/count. Negative numbers are represented in twos complement format.
(2) Resolution is 1°C/count. All values are unsigned with a –64°C offset.

Table 2. Decimal Fraction Temperature Data Format (Local and Remote Temperature Low Bytes)

TEMP (°C)	TEMPERATURE REGISTER LOW BYTE VALUE (0.0625°C RESOLUTION)(1)	
	STANDARD AND EXTENDED BINARY	HEX
0	0000 0000	00
0.0625	0001 0000	10
0.1250	0010 0000	20
0.1875	0011 0000	30
0.2500	0100 0000	40
0.3125	0101 0000	50
0.3750	0110 0000	60
0.4375	0111 0000	70
0.5000	1000 0000	80
0.5625	1001 0000	90
0.6250	1010 0000	A0
0.6875	1011 0000	B0
0.7500	1100 0000	C0
0.8125	1101 0000	D0
0.8750	1110 0000	E0
0.9375	1111 0000	F0

(1) Resolution is 0.0625°C/count. All possible values are shown.

REGISTER INFORMATION

The TMP431/32 contain multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum/minimum, limits, and status information. These registers are described in Figure 17 and in Table 3 for the TMP431, and in Table 4 for the TMP432.

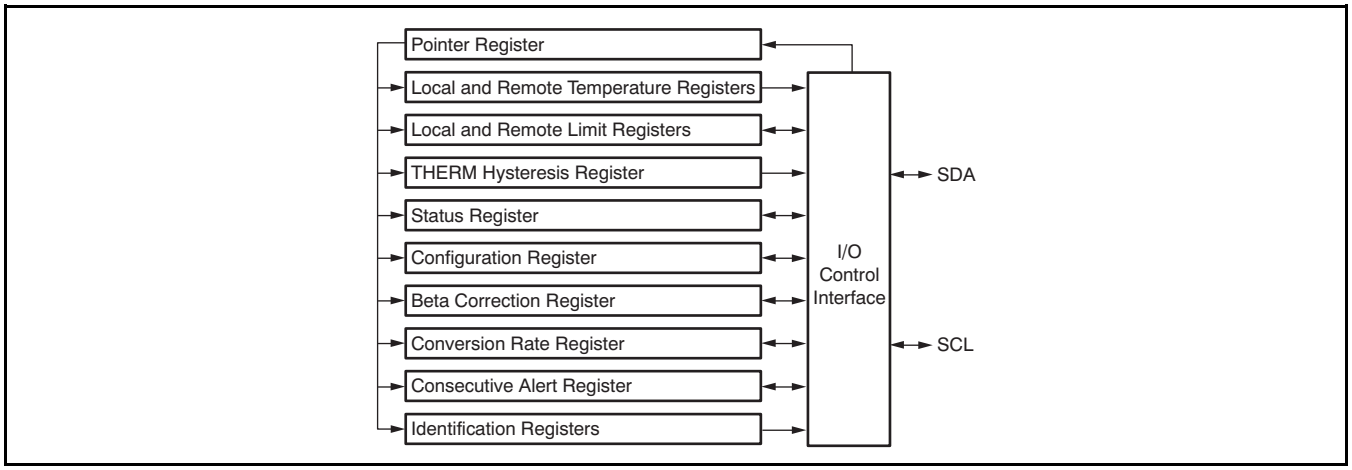


Figure 17. Internal Register Structure

Table 3. TMP431 Register Map

POINTER ADDRESS (HEX)		POWER-ON RESET (HEX)	BIT DESCRIPTIONS								REGISTER DESCRIPTIONS
READ	WRITE		D7	D6	D5	D4	D3	D2	D1	D0	
00	NA(1)	00	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	Local Temperature (High Byte)
01	NA	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature (High Byte)
02	NA	80	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM	Status Register
03	09	00	MASK	SD	$\overline{\text{AL/TH}}$	0	0	RANGE	0	0	Configuration Register 1
04	0A	07	0	0	0	0	R3	R2	R1	R0	Conversion Rate Register
05	0B	55	LTH11	LTH10	LTH9	LTH8	LTH7	LTH6	LTH5	LTH4	Local Temperature High Limit (High Byte)
06	0C	00	LTL11	LTL10	LTL9	LTL8	LTL7	LTL6	LTL5	LTL4	Local Temperature Low Limit (High Byte)
07	0D	55	RTH11	RTH10	RTH9	RTH8	RTH7	RTH6	RTH5	RTH4	Remote Temperature High Limit (High Byte)
08	0E	00	RTL11	RTL10	RTL9	RTL8	RTL7	RTL6	RTL5	RTL4	Remote Temperature Low Limit (High Byte)
NA	0F	XX	X(2)	X	X	X	X	X	X	X	One-Shot Start
10	NA	00	RT3	RT2	RT1	RT0	0	0	0	0	Remote Temperature (Low Byte)
13	13	00	RTH3	RTH2	RTH1	RTH0	0	0	0	0	Remote Temperature High Limit (Low Byte)
14	14	00	RTL3	RTL2	RTL1	RTL0	0	0	0	0	Remote Temperature Low Limit (Low Byte)
15	NA	00	LT3	LT2	LT1	LT0	0	0	0	0	Local Temperature (Low Byte)
16	16	00	LTH3	LTH2	LTH1	LTH0	0	0	0	0	Local Temperature High Limit (Low Byte)
17	17	00	LTL3	LTL2	LTL1	LTL0	0	0	0	0	Local Temperature Low Limit (Low Byte)
18	18	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N-factor Correction
19	19	55(3)	RTHL7	RTHL6	RTHL5	RTHL4	RTHL3	RTHL2	RTHL1	RTHL0	Remote THERM Limit
1A	1A	1C	0	0	0	REN	LEN	RC	0	0	Configuration Register 2
1F	1F	00	0	0	0	0	0	0	RIMASK	LMASK	Channel Mask
20	20	55(3)	LTHL7	LTHL6	LTHL5	LTHL4	LTHL3	LTHL2	LTHL1	LTHL0	Local THERM Limit
21	21	0A	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	THERM Hysteresis
22	22	70	0	CTH2	CTH1	CTH0	CALT2	CALT1	CALT0	0	Consecutive Alert Register
25	25	08	0	0	0	0	BC3	BC2	BC1	BC0	Beta Range Register
NA	FC	00	X(4)	X	X	X	X	X	X	X	Software Reset
FD	NA	31	0	0	1	1	0	0	0	1	TMP431 Device ID
FE	NA	55	0	1	0	1	0	1	0	1	Manufacturer ID

(1) NA = Not applicable; register is write- or read-only.
(2) X = Indeterminate state.
(3) TMP431C and TMP431D versions have a power-on reset value of 69h.
(4) X = Undefined. Writing any value to this register initiates a software reset; see the *Software Reset* section.

Table 4. TMP432 Register Map

POINTER ADDRESS		POWER-ON RESET (HEX)	BIT DESCRIPTIONS								REGISTER DESCRIPTIONS
READ	WRITE		D7	D6	D5	D4	D3	D2	D1	D0	
00	NA(1)	00	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	Local Temperature (High Byte)
01	NA	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature1 (High Byte)
02	NA	80	BUSY	0	0	HIGH	LOW	OPEN	THERM	0	Status Register
03	09	00	MASK	SD	$\overline{\text{AL/TH}}$	0	0	RANGE	0	0	Configuration Register1
04	0A	07	0	0	0	0	R3	R2	R1	R0	Conversion Rate Register
05	0B	55	LTH11	LTH10	LTH9	LTH8	LTH7	LTH6	LTH5	LTH4	Local Temperature High Limit (High Byte)
06	0C	00	LTL11	LTL10	LTL9	LTL8	LTL7	LTL6	LTL5	LTL4	Local Temperature Low Limit (High Byte)
07	0D	55	RTH11	RTH10	RTH9	RTH8	RTH7	RTH6	RTH5	RTH4	Remote Temperature1 High Limit (High Byte)
08	0E	00	RTL11	RTL10	RTL9	RTL8	RTL7	RTL6	RTL5	RTL4	Remote Temperature1 Low Limit (High Byte)
NA	0F	XX	X(2)	X	X	X	X	X	X	X	One-Shot Start
10	NA	00	RT3	RT2	RT1	RT0	0	0	0	0	Remote Temperature1 (Low Byte)
13	13	00	RTH3	RTH2	RTH1	RTH0	0	0	0	0	Remote Temperature1 High Limit (Low Byte)
14	14	00	RTL3	RTL2	RTL1	RTL0	0	0	0	0	Remote Temperature1 Low Limit (Low Byte)
15	15	55	RTH11	RTH10	RTH9	RTH8	RTH7	RTH6	RTH5	RTH4	Remote Temperature2 High Limit (High Byte)
16	16	00	RTL11	RTL10	RTL9	RTL8	RTL7	RTL6	RTL5	RTL4	Remote Temperature2 Low Limit (High Byte)
17	17	00	RTH3	RTH2	RTH1	RTH0	0	0	0	0	Remote Temperature2 High Limit (Low Byte)
18	18	00	RTL3	RTL2	RTL1	RTL0	0	0	0	0	Remote Temperature2 Low Limit (Low Byte)
19	19	55	RTHL7	RTHL6	RTHL5	RTHL4	RTHL3	RTHL2	RTHL1	RTHL0	Remote Therm Limit
1A	1A	55	RTHL7	RTHL6	RTHL5	RTHL4	RTHL3	RTHL2	RTHL1	RTHL0	Remote2 Therm Limit
1B	1B	00	0	0	0	0	0	R2FAULT	R1FAULT	0	Fault Status
1F	1F	00	0	0	0	0	0	R2MASK	R1MASK	LMASK	Channel Mask
20	20	55	LTHL7	LTHL6	LTHL5	LTHL4	LTHL3	LTHL2	LTHL1	LTHL0	Local Therm Limit
21	21	0A	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	Therm Limit Hysteresis
22	22	70	0	CTH2	CTH1	CTH0	CALT2	CALT1	CALT0	0	Consecutive Alert Register
23	NA	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature2 (High Byte)
24	NA	00	RT3	RT2	RT1	RT0	0	0	0	0	Remote Temperature2 (Low Byte)
25	25	08	0	0	0	0	BC3	BC2	BC1	BC0	Ch. 1 Beta Range Selection
26	26	08	0	0	0	0	BC3	BC2	BC1	BC0	Ch. 2 Beta Range Selection
27	27	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N-factor Correction Remote1

(1) NA = Not applicable; register is write- or read-only.
(2) Indeterminate state.

Table 4. TMP432 Register Map (continued)

POINTER ADDRESS		POWER-ON RESET (HEX)	BIT DESCRIPTIONS								REGISTER DESCRIPTIONS
READ	WRITE		D7	D6	D5	D4	D3	D2	D1	D0	
28	28	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N-factor Correction Remote2
29	NA	00	T3	T2	T1	T0	0	0	0	0	Local Temperature (Low Byte)
35	35	00	0	0	0	0	0	R2HIGH	R1HIGH	LHIGH	High Limit Status
36	36	00	0	0	0	0	0	R2LOW	R1LOW	LLOW	Low Limit Status
37	37	00	0	0	0	0	0	R2THERM	R1THERM	LTHERM	Therm Status
3D	3D	00	LTH3	LTH2	LTH1	LTH0	0	0	0	0	Local Temperature High Limit (Low Byte)
3E	3E	00	LTL3	LTL2	LTL1	LTL0	0	0	0	0	Local Temperature Low Limit (Low Byte)
3F	3F	3C	0	0	REN2	REN	LEN	RC	0	0	Configuration Register2
NA	FC	00	X(3)	X	X	X	X	X	X	X	Software Reset
FD	NA	32	0	0	1	1	0	0	1	0	TMP432 Device ID
FE	NA	55	0	1	0	1	0	1	0	1	Manufacturer ID

(3) X = Undefined. Writing any value to this register initiates a software reset; see the *Software Reset* section.

Pointer Register

Figure 17 shows the internal register structure of the TMP431/32. The 8-bit Pointer Register is used to address a given data register. The Pointer Register identifies which of the data registers should respond to a read or write command on the Two-Wire bus. This register is set with every write command. A write command must be issued to set the proper value in the Pointer Register before executing a read command. Table 3 describes the pointer address of the registers available in the TMP431. Table 4 describes the address of the registers available in the TMP432. The power-on reset (POR) value of the Pointer Register is 00h (0000 0000b).

Temperature Registers

The TMP431 has four 8-bit registers that hold temperature measurement results. The TMP432 has six 8-bit registers that hold temperature measurement results. Both the local channel and the remote channel have a high byte register that contains the most significant bits (MSBs) of the temperature analog-to-digital converter (ADC) result and a low byte register that contains the least significant bits (LSBs) of the temperature ADC result. The local channel high byte address for the TMP431/32 is 00h; the local channel low byte address is 15h for the TMP431 and 29h for the TMP432. The remote channel high byte is at address 01h; the remote channel low byte address is 10h. For the TMP432, the second remote channel high byte address is 23h; the second remote channel low byte is 24h. These registers are read-only and are updated by the ADC each time a temperature measurement is completed.

The TMP431/32 contain circuitry to assure that a low byte register read command returns data from the same ADC conversion as the immediately preceding high byte read command. This assurance remains valid only until another register is read. For proper operation, the high byte of a temperature register should be read first. The low byte register should be read in the next read command. The low byte register may be left unread if the LSBs are not needed. Alternatively, the temperature registers may be read as a 16-bit register by using a single two-byte read command from address 00h for the local channel result, or from address 01h for the remote channel result (23h for the second remote channel result). The high byte is output first, followed by the low byte. Both bytes of this read operation are from the same ADC conversion. The power-on reset value of both temperature registers is 00h.

Limit Registers

The TMP431/32 have registers for setting comparator limits for both the local and remote measurement channels. These registers have read and write capability. The High and Low Limit Registers for both channels span two registers, as do the temperature registers. The local temperature high limit is set by writing the high byte to pointer address 0Bh and writing the low byte to pointer address 16h for the TMP431 and 3Dh for the TMP432, or by using a single two-byte write command (high byte first) to pointer address 0Bh.

The local temperature high limit is obtained by reading the high byte from pointer address 05h and the low byte from pointer address 16h for the TMP4341 and 3Dh for the TMP432, or by using a two-byte read command from pointer address 05h. The power-on reset value of the local temperature high limit is 55h/00h (+85°C in standard temperature mode; +21°C in extended temperature mode).

Similarly, the local temperature low limit is set by writing the high byte to pointer address 0Ch and writing the low byte to pointer address 17h for the TMP431 and 3Eh for the TMP432, or by using a single two-byte write command to pointer address 0Ch. The local temperature low limit is read by reading the high byte from pointer address 06h and the low byte from pointer address 17h and 3Eh for the TMP432, or by using a two-byte read from pointer address 06h. The power-on reset value of the local temperature low limit register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The remote temperature high limit for the TMP431 (remote temperature1 high limit for the TMP432) is set by writing the high byte to pointer address 0Dh and writing the low byte to pointer address 13h, or by using a two-byte write command to pointer address 0Dh. The remote temperature high limit is obtained by reading the high byte from pointer address 07h and the low byte from pointer address 13h, or by using a two-byte read command from pointer address 07h. The power-on reset value of the Remote Temperature High Limit Register is 55h/00h (+85°C in standard temperature mode; +21°C in extended temperature mode).

The remote temperature low limit for the TMP431 (remote temperature1 low limit for the TMP432) is set by writing the high byte to pointer address 0Eh and writing the low byte to pointer address 14h, or by using a two-byte write to pointer address 0Eh. The remote temperature low limit is read by reading the high byte from pointer address 08h and the low byte from pointer address 14h, or by using a two-byte read from pointer address 08h. The power-on reset value of the Remote Temperature Low Limit Register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The remote temperature2 high limit for the TMP432 is set by writing the high byte to pointer address 15h and writing the low byte to pointer address 17h, or by using a two-byte write command to pointer address 15h. The remote temperature high limit is obtained by reading the high byte from pointer address 15h and the low byte from pointer address 17h, or by using a two-byte read command from pointer address 15h. The power-on reset value of the Remote Temperature High Limit Register is 55h/00h (+85°C in standard temperature mode; +21°C in extended temperature mode).

The remote temperature2 low limit for the TMP432 is set by writing the high byte to pointer address 16h and writing the low byte to pointer address 18h, or by using a two-byte write to pointer address 16h. The remote temperature low limit is read by reading the high byte from pointer address 16h and the low byte from pointer address 18h, or by using a two-byte read from pointer address 16h. The power-on reset value of the Remote Temperature Low Limit Register is 00h/00h (0°C in standard temperature mode; –64°C in extended mode).

The TMP431/32 also have a THERM limit register for both the local and the remote channels. These registers are eight bits and allow for THERM limits set to 1°C resolution. The local channel THERM limit is set by writing to pointer address 20h. The remote channel THERM limit is set by writing to pointer address 19h. The remote channel THERM2 limit for the TMP432 is set by writing to pointer address 1Ah.

The local channel THERM limit is obtained by reading from pointer address 20h; the remote channel THERM limit is read by reading from pointer address 19h. The remote channel THERM2 limit is read by reading from pointer address 1Ah. The power-on reset value of the THERM limit registers is 55h for the TMP431A, TMP431B, TMP432A, and TMP432B (+85°C in standard temperature mode; +21°C in extended temperature mode). The power-on reset value of the THERM limit registers is 69h for the TMP431C and TMP431D (+105°C in standard temperature mode; +41°C in extended temperature mode). The THERM limit comparators also have hysteresis. The hysteresis of both comparators is set by writing to pointer address 21h. The hysteresis value is obtained by reading from pointer address 21h. The value in the Hysteresis Register is an unsigned number (always positive). The power-on reset value of this register is 0Ah (+10°C).

Whenever changing between standard and extended temperature ranges, be aware that the temperatures stored in the temperature limit registers are **NOT** automatically reformatted to correspond to the new temperature range format. These values must be reprogrammed in the appropriate binary or extended binary format.

Status Registers

TMP431 Status Register

Table 5. TMP431 Status Register Format

TMP431 STATUS REGISTER (Read = 02h, Write = NA)								
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM
POR VALUE	0(1)	0	0	0	0	0	0	0

(1) The BUSY bit changes to '1' almost immediately (<< 100µs) following power-up, as the TMP431 begins the first temperature conversion. It is high whenever the TMP431 is converting a temperature reading.

The TMP431 has a Status Register to report the state of the temperature comparators. Table 5 shows the Status Register bits. The Status Register is read-only and is read by reading from pointer address 02h.

The BUSY bit reads as '1' if the ADC is making a conversion. It reads as '0' if the ADC is not converting.

The OPEN bit reads as '1' if the remote transistor was detected as open since the last read of the Status Register. The OPEN status is only detected when the ADC is attempting to convert a remote temperature.

The RTHRM bit reads as '1' if the remote temperature exceeds the remote THERM limit and remains greater than the remote THERM limit less the value in the shared Hysteresis Register; see Figure 23.

The LTHRM bit reads as '1' if the local temperature exceeds the local THERM limit and remains greater than the local THERM limit less the value in the shared Hysteresis Register; see Figure 23.

The LHIGH and RHIGH bit values depend on the state of the AL/TH bit in the Configuration Register 1. If the AL/TH bit is '0', the LHIGH bit reads as '1' if the local high limit was exceeded since the last clearing of the Status Register. The RHIGH bit reads as '1' if the remote high limit was exceeded since the last clearing of the Status Register. If the AL/TH bit is '1', the remote high limit and the local high limit are used to implement a THERM2 function. LHIGH reads as '1' if the local temperature exceeds the local high limit and remains greater than the local high limit less the value in the Hysteresis Register.

The RHIGH bit reads as '1' if the remote temperature has exceeded the remote high limit and remains greater than the remote high limit less the value in the Hysteresis Register.

The LLOW and RLOW bits are not affected by the AL/TH bit. The LLOW bit reads as '1' if the local low limit was exceeded since the last clearing of the Status Register. The RLOW bit reads as '1' if the remote low limit was exceeded since the last clearing of the Status Register.

The values of the LLOW, RLOW, and OPEN (as well as LHIGH and RHIGH when AL/TH is '0') are latched and read as '1' until the Status Register is read or a device reset occurs. These bits are cleared by reading the Status Register, provided that the condition causing the flag to be set no longer exists. The values of BUSY, LTHRM, and RTHRM (as well as LHIGH and RHIGH when ALERT/THERM2 is '1') are not latched and are not cleared by reading the Status Register. They always indicate the current state, and are updated appropriately at the end of the corresponding ADC conversion. Clearing the Status Register bits does not clear the state of the ALERT pin; an SMBus alert response address command must be used to clear the ALERT pin.

The TMP431 NORs LHIGH, LLOW, RHIGH, RLOW, and OPEN, so a status change for any of these flags from '0' to '1' automatically causes the ALERT pin to go low (only applies when the ALERT/THERM2 pin is configured for ALERT mode).

Status Registers (continued)

TMP432 Status Register

Table 6. TMP432 Status Register Format

TMP432 STATUS REGISTER (Read = 02h, Write = NA)								
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	BUSY	0	0	HIGH	LOW	OPEN	THERM	0
POR VALUE	0(1)	0	0	0	0	0	0	0

(1) The BUSY bit changes to '1' almost immediately (<< 100µs) following power-up, as the TMP432 begins the first temperature conversion. It is high whenever the TMP432 is converting a temperature reading.

The TMP432 has a Status Register to report the state of the temperature comparators. Table 6 shows the Status Register bits. The Status Register is read-only and is read by reading from pointer address 02h.

The BUSY bit reads as '1' if the ADC is making a conversion. It reads as '0' if the ADC is not converting.

The OPEN bit reads as '1' if the remote transistor was detected as open since the last read of the Status Register. The OPEN status is only detected when the ADC is attempting to convert a remote temperature.

The THERM bit reads as '1' if the temperature from any channel (remote or local) has exceeded the THERM limit and remains greater than the THERM limit less the value in the shared Hysteresis Register; see Figure 23.

The HIGH bit value depends on the state of the $\overline{\text{AL/TH}}$ bit in the Configuration Register 1. If the $\overline{\text{AL/TH}}$ bit is '0', the HIGH bit reads '1' if any of the temperature channels go beyond the programmed high limit since the last clearing of the Status Register. If the $\overline{\text{AL/TH}}$ bit is '1', the HIGH limit is used to implement THERM2 function. The HIGH bit reads as '1' if the temperature exceeds the high limit less the value in the Hysteresis Register.

The $\overline{\text{AL/TH}}$ bit does not affect the Status Register LOW bit. The LOW bit reads as '1' if any of the temperature channels go beyond the programmed low limit since the last clearing of the Status Register.

The values of the LOW and OPEN bits (as well as HIGH when $\overline{\text{AL/TH}}$ is '0') are latched and read as '1' until the Status Register is read or a device reset occurs. These bits are cleared by reading the Status Register, if the condition causing the flag to be set no longer exists.

The values of BUSY and THERM (as well as HIGH when $\overline{\text{AL/TH}}$ is '1') are not latched and are not cleared by reading the Status Register. They always indicate the current state, and are updated appropriately at the end of the corresponding ADC conversion. Clearing the Status Register bits does not clear the state of the $\overline{\text{ALERT}}$ pin; an SMBus alert response address command must be used to clear the $\overline{\text{ALERT}}$ pin.

The TMP432 NORs HIGH, LOW, and OPEN, so a status change for any of these flags from '0' to '1' automatically causes the $\overline{\text{ALERT}}$ pin to go low (only applies when the $\overline{\text{ALERT}}$/THERM2 pin is configured for ALERT mode).

Configuration Register 1

The Configuration Register 1 sets the temperature range, controls shutdown mode, and determines how the ALERT/THERM2 pin functions. The Configuration Register is set by writing to pointer address 09h and read by reading from pointer address 03h.

The MASK bit (bit 7) enables or disables the ALERT pin output if ALERT/THERM = 0. If ALERT/THERM = 1 then the MASK bit has no effect. If MASK is set to '0', the ALERT pin goes low when one of the temperature measurement channels exceeds its high or low limits for the chosen number of consecutive conversions. If the MASK bit is set to '1', the TMP431/32 retain the ALERT pin status, but the ALERT pin does not go low.

The shutdown (SD) bit (bit 6) enables or disables the temperature measurement circuitry. If SD = 0, the TMP431/32 convert continuously at the rate set in the conversion rate register. When SD is set to '1', the TMP431/32 immediately stop converting and enter a shutdown mode. When SD is set to '0' again, the TMP431/32 resume continuous conversions. A single conversion can be started when SD = 1 by writing to the One-Shot Register.

The AL/TH bit (bit 5) controls whether the ALERT pin functions in ALERT mode or THERM2 mode. If AL/TH = 0, the ALERT pin operates as an interrupt pin. In this mode, the ALERT pin goes low after the set number of consecutive out-of-limit temperature measurements occur.

If AL/TH = 1, the ALERT/THERM2 pin implements a THERM function (THERM2). In this mode, THERM2 functions similar to the THERM pin except that the local high limit and remote high limit registers are used for the thresholds. THERM2 goes low when either RHIGH or LHIGH is set.

The temperature range is set by configuring bit 2 of the Configuration Register 1. Setting this bit low configures the TMP431/32 for the standard measurement range (0°C to +127°C); temperature conversions will be stored in the standard binary format. Setting bit 2 high configures the TMP431/32 for the extended measurement range (–55°C to +150°C); temperature conversions are stored in the extended binary format (see Table 1).

The remaining bits of the Configuration Register 1 are reserved and must always be set to '0'. The power-on reset value for this register is 00h. Table 7 summarizes the bits of the Configuration Register 1.

Table 7. Configuration Register 1 Bit Descriptions

CONFIGURATION REGISTER 1 (Read = 03h, Write = 09h, POR = 00h)			
BIT	**NAME**	**FUNCTION**	**POWER-ON RESET VALUE**
7	MASK	0 = ALERT Enabled 1 = ALERT Masked	0
6	SD	0 = Run 1 = Shut Down	0
5	AL/TH	0 = ALERT Mode 1 = THERM Mode	0
4, 3	Reserved	—	0
2	Temperature Range	0 = 0°C to +127°C 1 = −55°C to +150°C	0
1, 0	Reserved	—	0

Configuration Register 2

Configuration Register 2 (pointer address 1Ah for the TMP431 and 3Fh for the TMP432) controls which temperature measurement channels are enabled and whether the external channels have the resistance correction feature enabled or not.

The RC bit enables the resistance correction feature for the external temperature channels. If RC = '1', series resistance correction is enabled; if RC = '0', resistance correction is disabled. Resistance correction should be enabled for most applications. However, disabling the resistance correction may yield slightly improved temperature measurement noise performance, and reduce conversion time by about 50%, which could lower power consumption when conversion rates of two per second or less are selected.

The LEN bit enables the local temperature measurement channel. If LEN = '1', the local channel is enabled; if LEN = '0', the local channel is disabled.

The REN bit enables external temperature measurement channel 1 (connected to pins 2 and 3.) If REN = '1', the external channel is enabled; if REN = '0', the external channel is disabled.

For the TMP432 only, the REN2 bit enables the second external measurement channel (connected to pins 4 and 5). If REN2 = '1', the second external channel is enabled; if REN2 = '0', the second external channel is disabled.

The temperature measurement sequence is local channel, external channel 1, external channel 2, shutdown, and delay (to set conversion rate, if necessary). The sequence starts over with the local channel. If any of the channels are disabled, they are skipped in the sequence. Table 8 summarizes the bits of Configuration Register 2.

Table 8. Configuration Register 2 Bit Descriptions

CONFIGURATION REGISTER 2 (Read/Write = 1A for TMP431 3F for TMP432; POR = 1Ch for TMP431; 3Ch for TMP432)			
BIT	**NAME**	**FUNCTION**	**POWER-ON RESET VALUE**
7, 6	Reserved	—	0
5	REN2	0 = External channel 2 disabled 1 = External channel 2 enabled	1 (TMP432) 0 (TMP431)
4	REN	0 = External channel 1 disabled 1 = External channel 1 enabled	1
3	LEN	0 = Local channel disabled 1 = Local channel enabled	1
2	RC	0 = Resistance correction disabled 1 = Resistance correction enabled	1
1, 0	Reserved	—	0

Conversion Rate Register

The Conversion Rate Register (pointer address 0Ah) controls the rate at which temperature conversions are performed. This register adjusts the idle time between conversions but not the conversion timing itself, thereby allowing the TMP431/32 power dissipation to be balanced with the temperature register update rate. Table 9 shows the conversion rate options and corresponding current consumption.

One-Shot Conversions

When the TMP431/32 are in shutdown mode (SD = 1 in the Configuration Register 1), a single conversion on both channels is started by writing any value to the One-Shot Start Register, pointer address 0Fh. This write operation starts one conversion; the TMP431/32 return to shutdown mode when that conversion completes. The value of the data sent in the write command is irrelevant and is not stored by the TMP431/32. When the TMP431/32 are in shutdown mode, an initial 200ps is required before a one-shot command can be given. (Note: When a shutdown command is issued, the TMP431/32 shut down immediately, aborting the current conversion.) This wait time only applies to the 200ps immediately following shutdown. One-shot commands can be issued without delay thereafter.

Table 9. Conversion Rate Register

CONVERSION RATE REGISTER (Read = 04h, Write = 0Ah, POR = 07h)										
									AVERAGE I_Q (TYP) (µA)	
R7	R6	R5	R4	R3	R2	R1	R0	CONVERSION/SEC	V_S = 2.7V	V_S = 5.5V
0	0	0	0	0	0	0	0	0.0625	11	32
0	0	0	0	0	0	0	1	0.125	17	38
0	0	0	0	0	0	1	0	0.25	28	49
0	0	0	0	0	0	1	1	0.5	47	69
0	0	0	0	0	1	0	0	1	80	103
0	0	0	0	0	1	0	1	2	128	155
0	0	0	0	0	1	1	0	4	190	220
07h to 0Fh								8	373	413

Beta Compensation Configuration Register

If the Beta Compensation Configuration Register is set to '1xxx' (beta correction enabled) for a given remote channel at the beginning of each temperature conversion, the TMP431/32 automatically detect if the sensor is diode-connected or GND collector-connected, select the proper beta range, and measure the sensor temperature appropriately.

If the Beta Compensation Configuration Register is set to '0111' (beta correction disabled) for a given channel, the automatic detection is bypassed and the temperature is measured assuming a diode-connected sensor. A PNP transistor may continue to be GND collector-connected in this mode, but no beta compensation factor is applied. When the beta correction is set to '0111' or the sensor is diode-connected (base shorted to collector), the η-factor used by the TMP431/32 is 1.008. When the beta correction configuration is set to '1xxx' (beta correction enabled) and the sensor is GND collector-connected (PNP collector to ground), the η-factor used by the TMP431/32 is 1.000. Table 10 shows the read value for the selected beta ranges and the appropriate η-factor used for each conversion.

Table 10. Beta Compensation Configuration Register

BCx3-BCx0	BETA RANGE DESCRIPTION	η-FACTOR	TIME
1000	Automatically selected range 0 (0.10 < beta < 0.18)	1.000	126ms
1001	Automatically selected range 1 (0.16 < beta < 0.26)	1.000	126ms
1010	Automatically selected range 2 (0.24 < beta < 0.43)	1.000	126ms
1011	Automatically selected range 3 (0.35 < beta < 0.78)	1.000	126ms
1100	Automatically selected range 4 (0.64 < beta < 1.8)	1.000	126ms
1101	Automatically selected range 5 (1.4 < beta < 9.0)	1.000	126ms
1110	Automatically selected range 6 (6.7 < beta < 40.0)	1.000	126ms
1111	Automatically selected range 7 (beta > 27.0)	1.000	126ms
1111	Automatically detected diode connected sensor	1.008	93ms
0000	Manually selected range 0 (0.10 < beta < 0.5)	1.000	93ms
0001	Manually selected range 1 (0.13 < beta < 1.0)	1.000	93ms
0010	Manually selected range 2 (0.18 < beta < 2.0)	1.000	93ms
0011	Manually selected range 3 (0.3 < beta < 25)	1.000	93ms
0100	Manually selected range 4 (0.5 < beta < 50)	1.000	93ms
0101	Manually selected range 5 (1.1 < beta < 100)	1.000	93ms
0110	Manually selected range 6 (2.4 < beta < 150)	1.000	93ms
0111	Manually disabled beta correction	1.008	93ms

η-Factor Correction Register

The TMP431/32 allow for a different η-factor value to be used for converting remote channel measurements to temperature. The remote channel uses sequential current excitation to extract a differential V_{BE} voltage measurement to determine the temperature of the remote transistor. Equation 1 relates this voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{\eta kT}{q} \ln\left(\frac{I_2}{I_1}\right) \quad (1)$$

The value η in Equation 1 is a characteristic of the particular transistor used for the remote channel. When the beta compensation configuration is set to '0111' (beta compensation disabled) or the sensor is diode-connected (base shorted to collector), the η-factor used by the TMP431/32 is 1.008. When the beta compensation configuration is set to '1000' (beta compensation enabled) and the sensor is GND collector-connected (PNP collector to ground), the η-factor used by the TMP431/32 is 1.000. If the η-factor used for the temperature conversion does not match the characteristic of the sensor, then temperature offset is observed. The value in the η-Factor Correction Register may be used to adjust the effective η-factor according to Equation 2 and Equation 3 for disabled beta compensation or a diode-connected sensor. Equation 4 and Equation 5 may be used for enabled beta compensation and a GND collector-connected sensor.

$$\eta_{eff} = \frac{1.008 \times 300}{300 - N_{ADJUST}} \quad (2)$$

$$N_{ADJUST} = 300 - \frac{300 \times 1.008}{\eta_{eff}} \quad (3)$$

$$\eta_{eff} = \frac{1.000 \times 300}{300 - N_{ADJUST}} \quad (4)$$

$$N_{ADJUST} = 300 - \frac{300 \times 1.000}{\eta_{eff}} \quad (5)$$

The η-correction value must be stored in twos-complement format, yielding an effective data range from –128 to +127. Table 11 shows the η-factor range for both 1.008 and 1.000. For the TMP431, the η-correction value may be written to and read from pointer address 18h. For the TMP432, the η-correction value may be written to and read from pointer address 27h. The η-correction value for the second remote channel is read to and written from pointer address 28h. The register power-on reset value is 00h, thus having no effect unless written to.

Table 11. η-Factor Range

N_{ADJUST}			η
BINARY	HEX	DECIMAL	
01111111	7F	127	1.747977
00001010	0A	10	1.042759
00001000	08	8	1.035616
00000110	06	6	1.028571
00000100	04	4	1.021622
00000010	02	2	1.014765
00000001	01	1	1.011371
00000000	00	0	1.008
11111111	FF	–1	1.004651
11111110	FE	–2	1.001325
11111100	FC	–4	0.994737
11111010	FA	–6	0.988235
11111000	F8	–8	0.981818
11110110	F6	–10	0.975484
10000000	80	–128	0.706542

Software Reset

The TMP431/32 may be reset by writing any value to Pointer Register FCh. This action restores the power-on reset state to all of the TMP431/32 registers as well as abort any conversion in process and clear the ALERT and THERM pins.

The TMP431/32 also support reset via the two-wire general call address (00000000). The TMP431/32 acknowledge the general call address and respond to the second byte. If the second byte is 00000110, the TMP431/32 execute a software reset. The TMP431/32 do not respond to other values in the second byte.

Consecutive Alert Register

The value in the Consecutive Alert Register (address 22h) determines how many consecutive out-of-limit measurements must occur on a measurement channel before the ALERT or the THERM signal is activated. The value in this register does not affect bits in the Status Register. Values of one, two, three, or four consecutive conversions can be selected; one conversion is the default. This function allows additional filtering for the ALERT or the THERM pin. Table 14 shows the consecutive alert bits. For bit descriptions, refer to Table 12.

Table 12. Consecutive Alert Register Bit Descriptions

BIT NAME			NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS (ALERT/THERM)
CALT2/CTH2	CALT1/CTH1	CALT0/CTH0	
0	0	0	1
0	0	1	2
0	1	1	3
1	1	1	4

.

Therm Hysteresis Register

The THERM Hysteresis Register, shown in Table 15, stores the hysteresis value used for the THERM pin alarm function. This register must be programmed with a value that is less than the Local Temperature High Limit Register value, Remote Temperature High Limit Register value, Local THERM Limit Register value, or Remote THERM Limit Register value; otherwise, the respective temperature comparator does not trip on the measured temperature falling edges. Allowable hysteresis values are shown in Table 13. The default hysteresis value is 10°C, whether the device is operating in the standard or extended mode setting.

Identification Registers

The TMP431/32 allow for the Two-Wire bus controller to query the device for manufacturer and device IDs to enable the device for software identification of the device at the particular Two-Wire bus address. The manufacturer ID is obtained by reading from pointer address FEh. The TMP431/32 both return 55h for the manufacturer code. The device ID is obtained by reading from pointer address FDh. The TMP431 returns 31h for the device ID and the TMP432 returns 32h for the device ID (see Table 3 and Table 4). These registers are read-only.

Table 13. Allowable THERM Hysteresis Values

TEMPERATURE (°C)	THERM HYSTERESIS VALUE	
	TH[7:0] (STANDARD BINARY)	(HEX)
0	0000 0000	00
1	0000 0001	01
5	0000 0101	05
10	0000 1010	0A
25	0001 1001	19
50	0011 0010	32
75	0100 1011	4B
100	0110 0100	64
125	0111 1101	7D
127	0111 1111	7F
150	1001 0110	96
175	1010 1111	AF
200	1100 1000	C8
225	1110 0001	E1
255	1111 1111	FF

Table 14. Consecutive Alert Register Format

CONSECUTIVE ALERT REGISTER (READ = 22h, WRITE = 22h, POR = 70h)								
BIT #	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	0	CTH2	CTH1	CTH0	CALT2	CALT1	CALT0	0
POR VALUE	0	1	1	1	0	0	0	0

Table 15. THERM Hysteresis Register Format

THERM HYSTERESIS REGISTER (Read = 21h, Write = 21h, POR = 0Ah)								
BIT #	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
POR VALUE	0	0	0	0	1	0	1	0

Fault Status Register

The Fault Status Register indicates if there is a fault on the remote channel diode. Bit 2 is set if remote channel 2 is open or faultily connected. Similarly, bit 1 corresponds to remote channel 1.

Channel Mask Register

The Channel Mask Register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin is asserted when the masked channel reads a diode fault or out-of-limit error.

High Limit Status Register

The High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, then the HIGH status bit in the Status Register is set.

Low Limit Status Register

The Low Limit Status Register contains the status bits that are set when a temperature channel low limit is exceeded. If any of these bits are set, then the LOW status bit in the Status Register is set.

THERM Limit Status Register

The THERM Limit Status Register contains the status bits that are set when a temperature channel THERM limit is exceeded. If any of these bits are set, then the THERM status bit in the Status Register is set.

BUS OVERVIEW

The TMP431/32 are SMBus interface-compatible. In SMBus protocol, the device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. START is indicated by pulling the data line (SDA) from a high to low logic level while SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer SDA must remain stable while SCL is high, because any change in SDA while SCL is high is interpreted as a control signal.

Once all data have been transferred, the master generates a STOP condition. STOP is indicated by pulling SDA from low to high, while SCL is high.

SERIAL INTERFACE

The TMP431/32 operate only as slave devices on either the Two-Wire bus or the SMBus. Connections to either bus are made via the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP431/32 support the transmission protocol for fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the TMP431/32, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit that indicates the intent of executing a read or write operation.

The address of the TMP431A/32A/31C is 4Ch (1001100b). The address of the TMP431B/32B/31D is 4Dh (1001101b).

READ/WRITE OPERATIONS

Accessing a particular register on the TMP431/32 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{\text{W}}$ bit low. Every write operation to the TMP431/32 require a value for the Pointer Register (see Figure 19).

When reading from the TMP431/32, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This transaction is accomplished by issuing a slave address byte with the R/$\overline{\text{W}}$ bit low, followed by the Pointer Register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{\text{W}}$ bit high to initiate the read command. See Figure 20 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes, because the TMP431/32 retain the Pointer Register value until it is changed by the next write operation. Note that register bytes are sent MSB first, followed by the LSB.

TIMING DIAGRAMS

The TMP431/32 are Two-Wire and SMBus-compatible. Figure 18 to Figure 22 describe the various operations on the TMP431/32. Bus definitions are given below. Parameters for Figure 18 are defined in Table 16.

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a STOP or a repeated START condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high

period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, data transfer termination can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

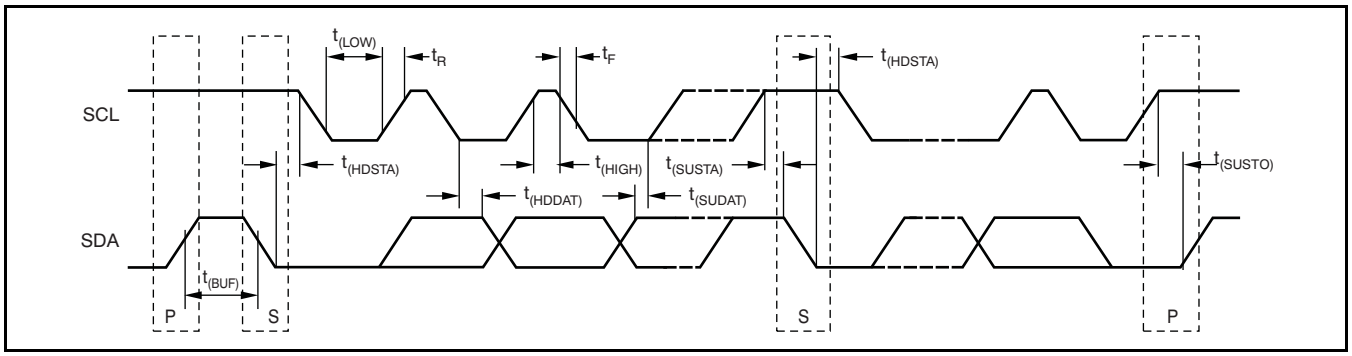
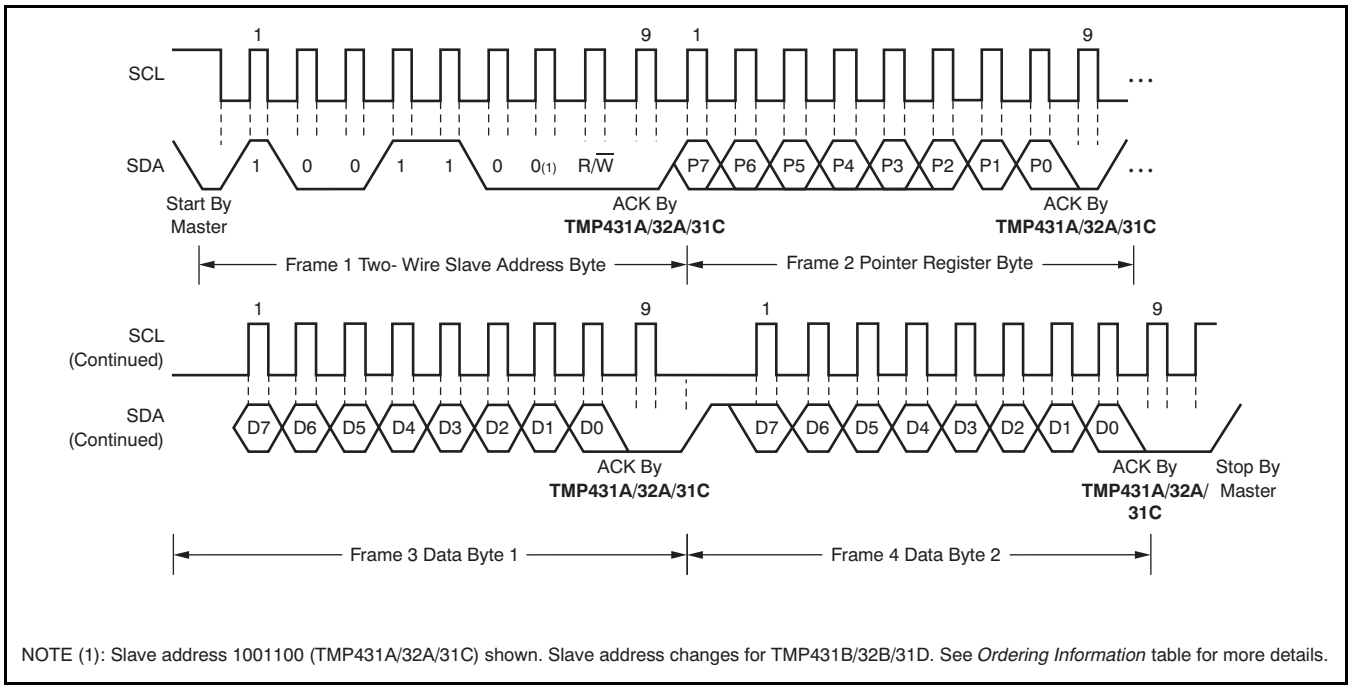


Figure 18. Two-Wire Timing Diagram

Table 16. Timing Diagram Definitions for Figure 18

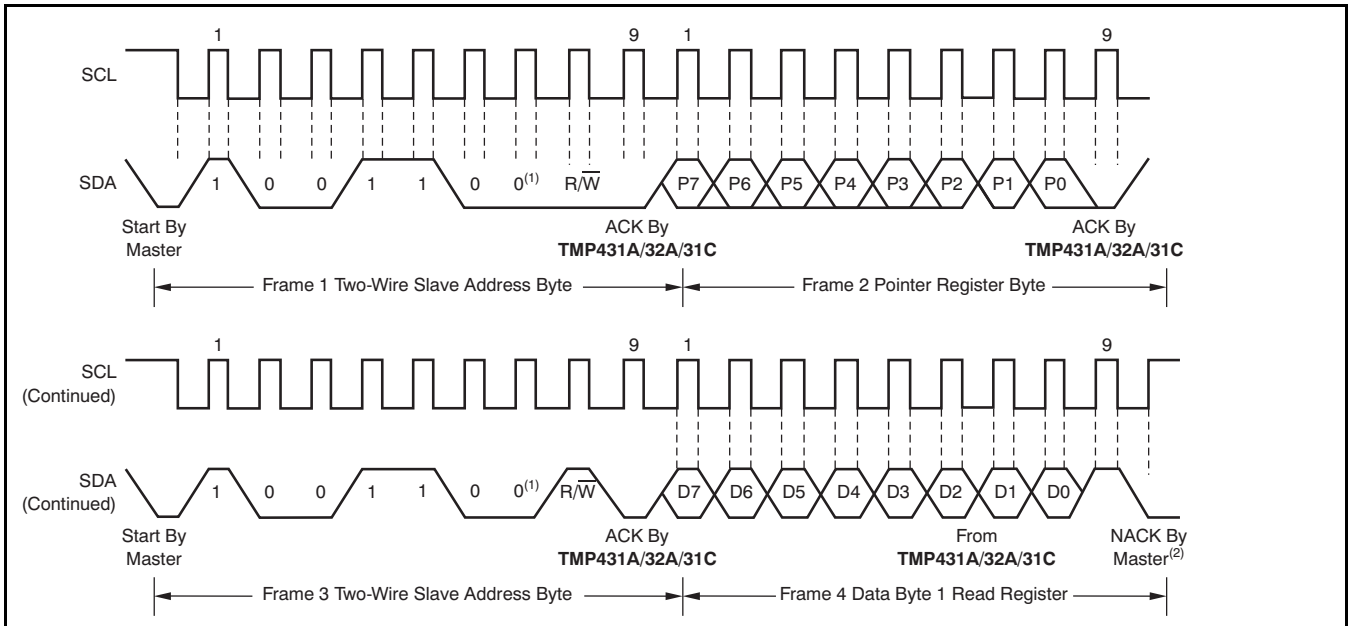
PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	$f_{(SCL)}$	0.001	0.4	0.001	3.4	MHZ
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	100		100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		100		ns
Data Hold Time	$t_{(HDDAT)}$	0(1)		0(2)		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCL Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCL Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns
for SCLK ≤ 100kHz			1000			ns

(1) For cases with fall time of SCL less than 20ns and/or the rise time or fall time of SDA less than 20ns, the hold time should be greater than 20ns.
(2) For cases with fall time of SCL less than 10ns and/or the rise or fall time of SDA less than 10ns, the hold time should be greater than 10ns.



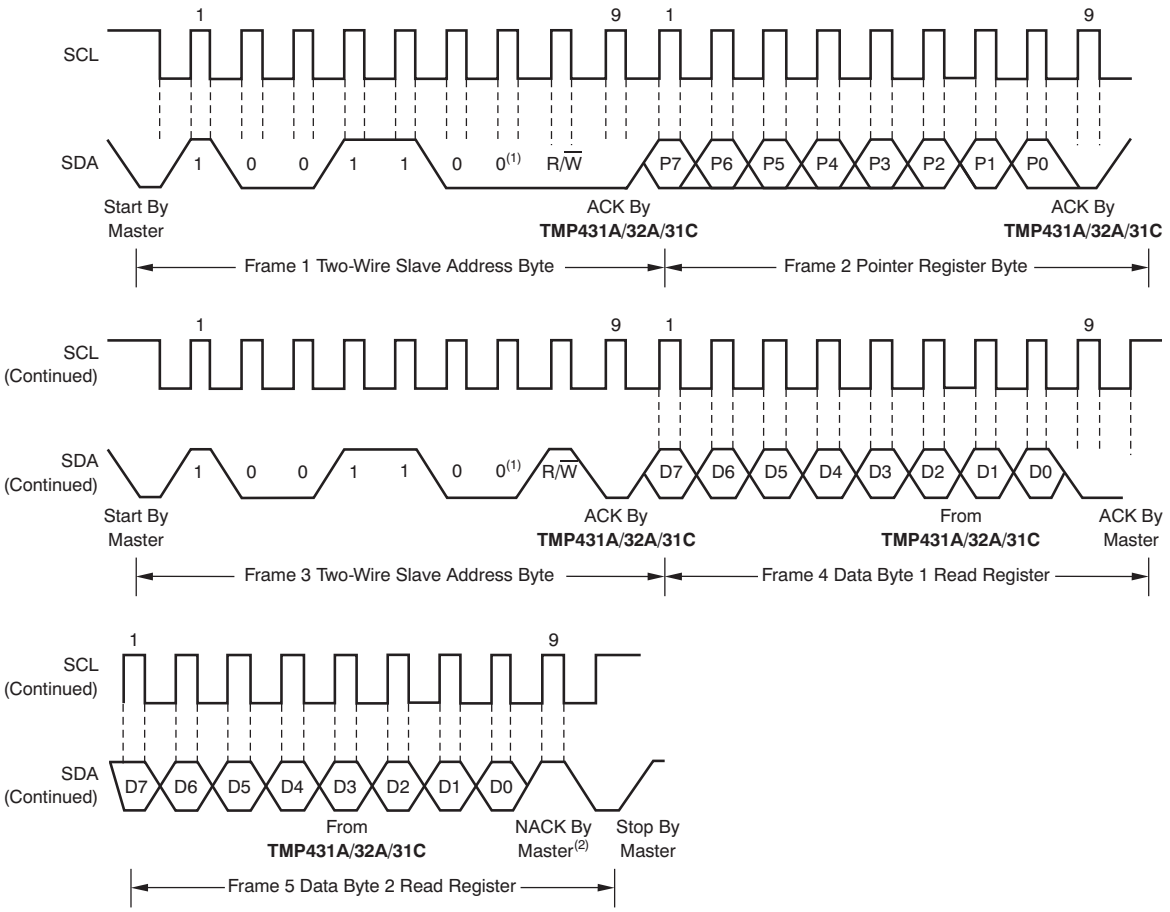
NOTE (1): Slave address 1001100 (TMP431A/32A/31C) shown. Slave address changes for TMP431B/32B/31D. See *Ordering Information* table for more details.

Figure 19. Two-Wire Timing Diagram for Write Word Format



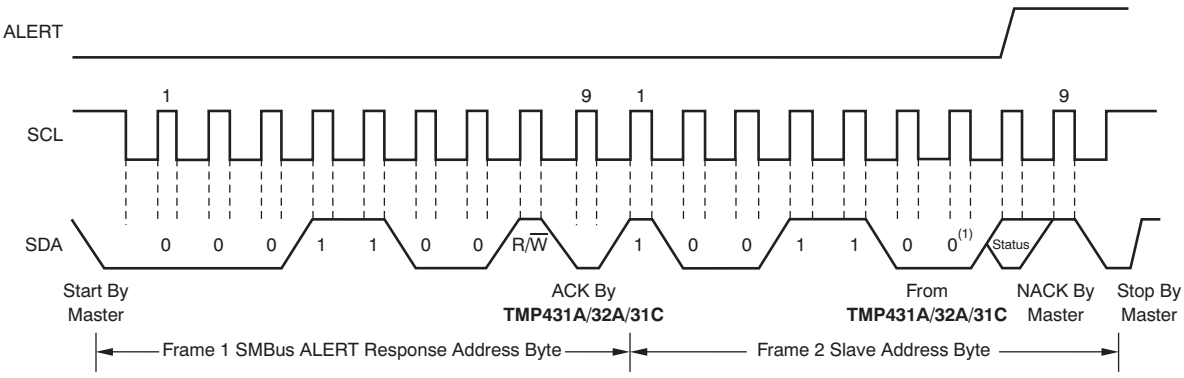
NOTES: (1) Slave address 1001100 (TMP431A/32A/31C) shown. Slave address changes for TMP431B/32B/31D. See *Ordering Information* table for more details.
(2) Master should leave SDA high to terminate a single-byte read operation.

Figure 20. Two-Wire Timing Diagram for Single-Byte Read Format



NOTES: (1) Slave address 1001100 (TMP431A/32A/31C) shown. Slave address changes for TMP431B/32B/31D. See *Ordering Information* table for more details.
(2) Master should leave SDA high to terminate a two-byte read operation.

Figure 21. Two-Wire Timing Diagram for Two-Byte Read Format



NOTE (1): Slave address 1001100 (TMP431A/32A/31C) shown. Slave address changes for TMP431B/32B/31D. See *Ordering Information* table for more details.

Figure 22. Timing Diagram for SMBus ALERT

HIGH-SPEED MODE

In order for the Two-Wire bus to operate at frequencies above 400kHz, the master device must issue a High-speed mode (Hs-mode) master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP431/32 do not acknowledge this byte, but switch the input filters on SDA and SCL and the output filter on SDA to operate in Hs-mode, allowing transfers at up to 3.4MHz. After the Hs-mode master code has been issued, the master transmits a Two-Wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP431/32 switch the input and output filter back to fast-mode operation.

TIMEOUT FUNCTION

The serial interface of the TMP431/32 resets if either SCL or SDA are held low for 32ms (typical) between a START and STOP condition. If the TMP431/32 are holding the bus low, it releases the bus and waits for a START condition.

$\overline{\text{THERM}}$ and ALERT/THERM2

The TMP431/32 have two pins dedicated to alarm functions, the $\overline{\text{THERM}}$ and ALERT/THERM2 pins. Both pins are open-drain outputs that each require a pull-up resistor to V+. These pins can be wire-ORed together with other alarm pins for system monitoring of multiple sensors. The $\overline{\text{THERM}}$ pin provides a thermal interrupt that cannot be software disabled. The $\overline{\text{ALERT}}$ pin is intended for use as an earlier warning interrupt, and can be software disabled, or masked. The ALERT/THERM2 pin can also be configured for use as $\overline{\text{THERM2}}$, a second $\overline{\text{THERM}}$ pin (Configuration Register 1: $\overline{\text{AL/TH}}$ bit = 1). The default setting configures pin 6 for the TMP431 and pin 8 for the TMP432 to function as $\overline{\text{ALERT}}$ ($\overline{\text{AL/TH}}$ = 0).

The $\overline{\text{THERM}}$ pin asserts low when either the measured local or remote temperature is outside of the temperature range programmed in the corresponding Local/Remote THERM Limit Register. The THERM temperature limit range can be programmed with a wider range than that of the limit registers, which allows $\overline{\text{ALERT}}$ to provide an earlier warning than $\overline{\text{THERM}}$. The $\overline{\text{THERM}}$ alarm resets automatically when the measured temperature returns to within the THERM temperature limit range minus the hysteresis value stored in the THERM Hysteresis Register. The allowable values of hysteresis are shown in Table 13. The default hysteresis is 10°C. When the ALERT/THERM2 pin is configured as a second thermal alarm (Configuration Register: bit 7 = x, bit 5 = 1), it functions the same as $\overline{\text{THERM}}$, but uses the temperatures stored in the Local/Remote Temperature High Limit Registers to set its comparison range.

When ALERT/THERM2 is configured as $\overline{\text{ALERT}}$ (Configuration Register 1: bit 7 = 0, bit 5 = 0), the pin asserts low when either the measured local or remote temperature violates the range limit set by the corresponding Local/Remote Temperature High/Low Limit Registers. This alert function can be configured to assert only if the range is violated a specified number of consecutive times (1, 2, 3, or 4). The consecutive violation limit is set in the Consecutive Alert Register. False alerts that occur as a result of environmental noise can be prevented by requiring consecutive faults. $\overline{\text{ALERT}}$ also asserts low if the remote temperature sensor is open-circuit. When the MASK function is enabled (Configuration Register 1: bit 7 = 1), $\overline{\text{ALERT}}$ is disabled (that is, masked). $\overline{\text{ALERT}}$ resets when the master reads the device address, as long as the condition that caused the alert no longer persists, and the Status Register has been reset.

SMBus ALERT FUNCTION

The TMP431/32 support the SMBus Alert function. When pin 6 (for the TMP431) or pin 8 (for the TMP432) is configured as an alert output, the $\overline{\text{ALERT}}$ pin of the TMP431/32 may be connected as an SMBus Alert signal. When a master detects an alert condition on the $\overline{\text{ALERT}}$ line, the master sends an SMBus Alert command (00011001) on the bus. If the $\overline{\text{ALERT}}$ pin of the TMP431/32 is active, the devices acknowledge the SMBus Alert command and respond by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether the temperature exceeding one of the temperature high limit settings or falling below one of the temperature low limit settings caused the alert condition. This bit is high if the temperature is greater than or equal to one of the temperature high limit settings; this bit is low if the temperature is less than one of the temperature low limit settings. See Figure 23 for details of this sequence.

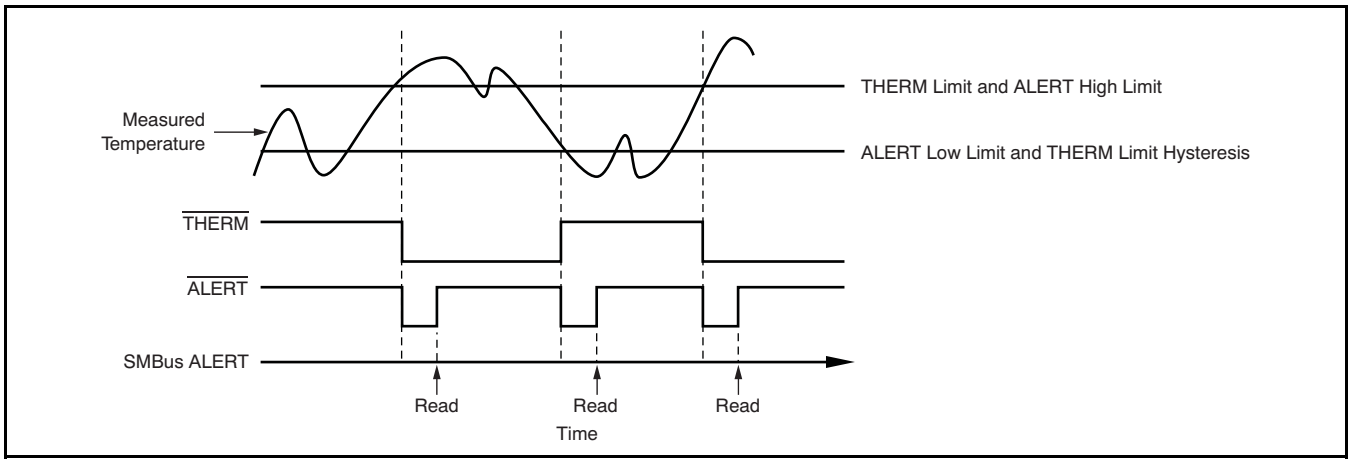


Figure 23. SMBus Alert Timing Diagram

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determines which device clears its alert status. If the TMP431/32 win the arbitration, the ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP431/32 lose the arbitration, the ALERT pin remains active.

SHUTDOWN MODE (SD)

The TMP431/32 shutdown mode allows the user to save maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 3µA; see typical characteristic curve *Shutdown Quiescent Current vs Supply Voltage* (Figure 6). Shutdown mode is enabled when the SD bit of the Configuration Register 1 is high; the device shuts down immediately, aborting the current conversion. When SD is low, the device maintains a continuous conversion state.

SENSOR FAULT

The TMP431/32 can sense a fault at the DXP input that results from an incorrect diode connection or an open circuit. The detection circuitry consists of a voltage comparator that trips when the voltage at DXP exceeds (V+) – 0.6V (typical). The comparator output is continuously checked during a conversion. If a fault is detected, the last valid measured temperature is used for the temperature measurement result, the OPEN bit (Status Register, bit 2) is set high, and, if the alert function is enabled, ALERT asserts low.

When not using the remote sensor with the TMP431/32, the DXP and DXN inputs must be connected together to prevent meaningless fault warnings.

UNDERVOLTAGE LOCKOUT

The TMP431/32 sense when the power-supply voltage has reached a minimum voltage level for the ADC to function. The detection circuitry consists of a voltage comparator that enables the ADC after the power supply (V+) exceeds 2.45V (typical). The comparator output is continuously checked during a conversion. The TMP431/32 do not perform a temperature conversion if the power supply is not valid. The last valid measured temperature is used for the temperature measurement result.

GENERAL CALL RESET

The TMP431/32 support reset via the Two-Wire General Call address 00h (0000 0000b). The TMP431/32 acknowledge the General Call address and respond to the second byte. If the second byte is 06h (0000 0110b), the TMP431/32 execute a software reset. This software reset restores the power-on reset state to all TMP431/32 registers, aborts any conversion in progress, and clears the ALERT and THERM pins. The TMP431/32 take no action in response to other values in the second byte.

FILTERING

Remote junction temperature sensors are usually implemented in noisy environments. Noise is frequently generated by fast digital signals and if not filtered properly can induce errors that corrupt temperature measurements. The TMP431/32 have a built-in 65kHz filter on the inputs of DXP and DXN to minimize the effects of noise. However, a differential low-pass filter can help attenuate unwanted coupled signals. Exact component values are application-specific. It is also recommended that the capacitor value remains between 0pF to 2200pF with a series resistance less than 1kΩ.

REMOTE SENSING

The TMP431/32 are designed to be used with either discrete transistors or substrate transistors built into processor chips and ASICs. Either NPN- or PNP-type transistors can be used, as long as the base-emitter junction is used as the remote temperature sense. NPN transistors must be diode-connected. PNP transistors can either be transistor- or diode-connected (see Figure 15).

Errors in remote temperature sensor readings are typically the consequence of the ideality factor and current excitation used by the TMP431/32 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a high-level and low-level current for the temperature-sensing substrate transistors. The TMP431/32 use 6μA for I_{LOW} and 120μA for I_{HIGH}. The TMP431/32 allow for different η-factor values; see the η- *Factor Correction Register* section.

The ideality factor (η) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The ideality factor for the TMP431/32 is trimmed to be 1.008. For transistors whose ideality factor does not match the TMP431/32, Equation 6 can be used to calculate the temperature error. Note that for the equation to be used correctly, actual temperature (°C) must be converted to Kelvin (K).

$$T_{ERR} = \left(\frac{\eta - 1.008}{1.008}\right) \times [273.15 + T(°C)]$$

Where:

- η = Ideality factor of remote temperature sensor
- T(°C) = actual temperature
- T_{ERR} = Error in TMP431/32 reading due to η ≠ 1.008
- Degree delta is the same for °C and K (6)

For *n* = 1.004 and T(°C) = 100°C:

$$T_{ERR} = \left(\frac{1.004 - 1.008}{1.008}\right) \times (273.15 + 100°C)$$

$$T_{ERR} = 1.48°C \quad (7)$$

If a discrete transistor is used as the remote temperature sensor with the TMP431/32, the best accuracy can be achieved by selecting the transistor according to the following criteria:

1. Base-emitter voltage > 0.25V at 6μA, at the highest sensed temperature.
2. Base-emitter voltage < 0.95V at 120μA, at the lowest sensed temperature.
3. Base resistance < 100Ω.
4. Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (that is, 50 to 150).

Based on these criteria, two recommended small-signal transistors are the 2N3904 (NPN) or 2N3906 (PNP).

MEASUREMENT ACCURACY AND THERMAL CONSIDERATIONS

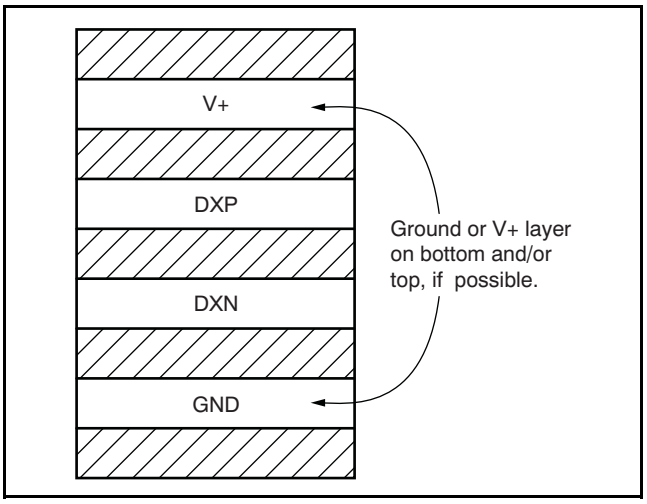
The temperature measurement accuracy of the TMP431/32 depends on the remote and/or local temperature sensor being at the same temperature as the system point being monitored. Clearly, if the temperature sensor is not in good thermal contact with the part of the system being monitored, then there will be a delay in the response of the sensor to a temperature change in the system. For remote temperature sensing applications that use a substrate transistor (or a small, SOT23 transistor) placed close to the device being monitored, this delay is usually not a concern.

The local temperature sensor inside the TMP431/32 monitors the ambient air around the device. The thermal time constant for the TMP431/32 is approximately 2 seconds. This constant implies that if the ambient air changes quickly by 100°C, it would take the TMP431/32 about 10 seconds (that is, five thermal time constants) to settle to within 1°C of the final value. In most applications, the TMP431/32 package is in thermal contact with the printed circuit board (PCB), as well as subjected to forced airflow. The accuracy of the measured temperature directly depends on how accurately the PCB and forced airflow temperatures represent the temperature that the TMP431/32 is measuring. Additionally, the internal power dissipation of the TMP431/32 can cause the temperature to rise above the ambient or PCB temperature. The internal power dissipated as a result of exciting the remote temperature sensor is negligible because of the small currents used. For a 5.5V supply and maximum conversion rate of eight conversions per second, the TMP431/32 dissipate 1.82mW (PD_{IQ} = 5.5V × 330μA). If both the $\overline{\text{ALERT}}$/THERM2 and $\overline{\text{THERM}}$ pins are each sinking 1mA, an additional 0.8mW is dissipated (PD_{OUT} = 1mA × 0.4V + 1mA × 0.4V = 0.8mW). Total power dissipation is then 2.62mW (PD_{IQ} + PD_{OUT}) and, with an θ_{JA} of 150°C/W, causes the junction temperature to rise approximately 0.393°C above the ambient.

LAYOUT CONSIDERATIONS

Remote temperature sensing on the TMP431/32 measures very small voltages using very low currents; therefore, noise at the IC inputs must be minimized. Most applications using the TMP431/32 have high digital content, with several clocks and logic level transitions creating a noisy environment. Layout should conform to the following guidelines:

1. Place the TMP431/32 as close to the remote junction sensor as possible.
2. Route the DXP and DXN traces next to each other and shield them from adjacent signals through the use of ground guard traces, as shown in Figure 24. If a multilayer PCB is used, bury these traces between ground or V_{DD} planes to shield them from extrinsic noise sources. 5 mil (0,127 mm) PCB traces are recommended.
3. Minimize additional thermocouple junctions caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the DXP and DXN connections to cancel any thermocouple effects.
4. Use a 0.1µF local bypass capacitor directly between the V+ and GND of the TMP431/32. Figure 25 shows the suggested bypass capacitor placement for the TMP431/32. This capacitance includes any cable capacitance between the remote temperature sensor and TMP431/32.
5. If the connection between the remote temperature sensor and the TMP431/32 is less than 8 inches (20,32 cm), use a twisted-wire pair connection. Beyond 8 inches, use a twisted, shielded pair with the shield grounded as close to the TMP431/32 as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60Hz pickup.
6. Thoroughly clean and remove all flux residue in and around the pins of the TMP431/32 to avoid temperature offset readings as a result of leakage paths between DXP or DXN and GND, or between DXP or DXN and V+.



Note: Use 5 mil (.005 in, or 0,127 mm) traces with 5 mil (.005 in, or 0,127 mm) spacing.

Figure 24. Example Signal Traces

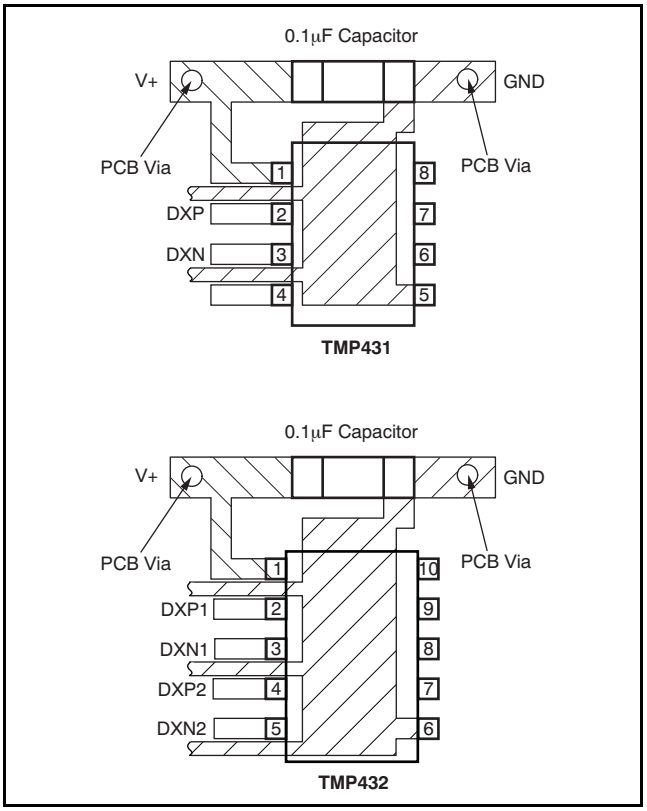


Figure 25. Suggested Bypass Capacitor Placement

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2012) to Revision F — **Page**

- Changed Ordering Information table 2
- Added five new register descriptions 25

Changes from Revision D (November 2012) to Revision E — **Page**

- Changed all MSOP-10 to VSSOP-10 throughout document 1

Changes from Revision C (February 2011) to Revision D — **Page**

- Changed all MSOP-8 to VSSOP-8 throughout document 1

Changes from Revision B (April 2010) to Revision C — **Page**

- Added *Therm high limit* column to *Package Information* table 2
- Added TMP431C, TMP431D device information 2
- Added footnote (4) to TMP431 Register Map 13
- Revised information about power-on reset value of THERM limit registers in *Limit Registers* section 16
- Updated *Serial Bus Address* section for TMP431C/TMP431D device versions 25
- Revised Figure 19 27
- Updated Figure 20 27
- Changed Figure 21 28
- Revised Figure 22 28

Changes from Revision A (November 2009) to Revision B — **Page**

- Corrected Equation 7 31

Changes from Original (September 2009) to Revision A — **Page**

- Changed device status for TMP432 throughout document 1
- Changed orderable device status for TMP432A and TMP432B devices 2
- Corrected bit D6 value in Configuration Register 1 in TMP431 Register Map 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP431ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DRTI	Samples
TMP431ADGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DRTI	Samples
TMP431BDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DRUI	Samples
TMP431BDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DRUI	Samples
TMP431CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DUEC	Samples
TMP431CDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DUEC	Samples
TMP431DDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DUFC	Samples
TMP431DDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DUFC	Samples
TMP432ADGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DSCI	Samples
TMP432ADGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DSCI	Samples
TMP432BDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DSDI	Samples
TMP432BDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DSDI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

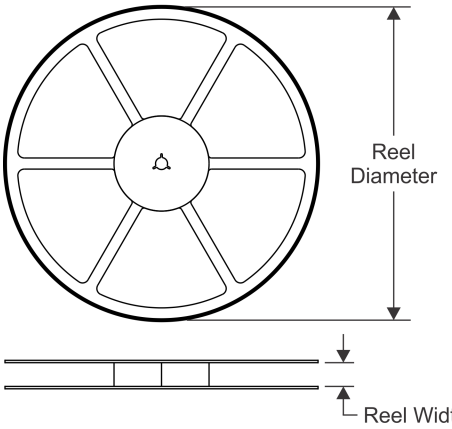
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

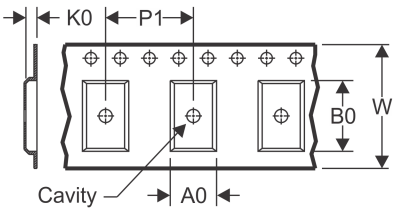
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

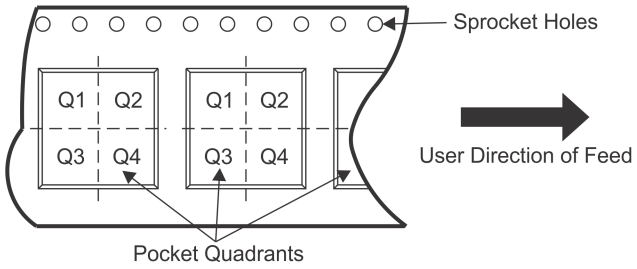


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

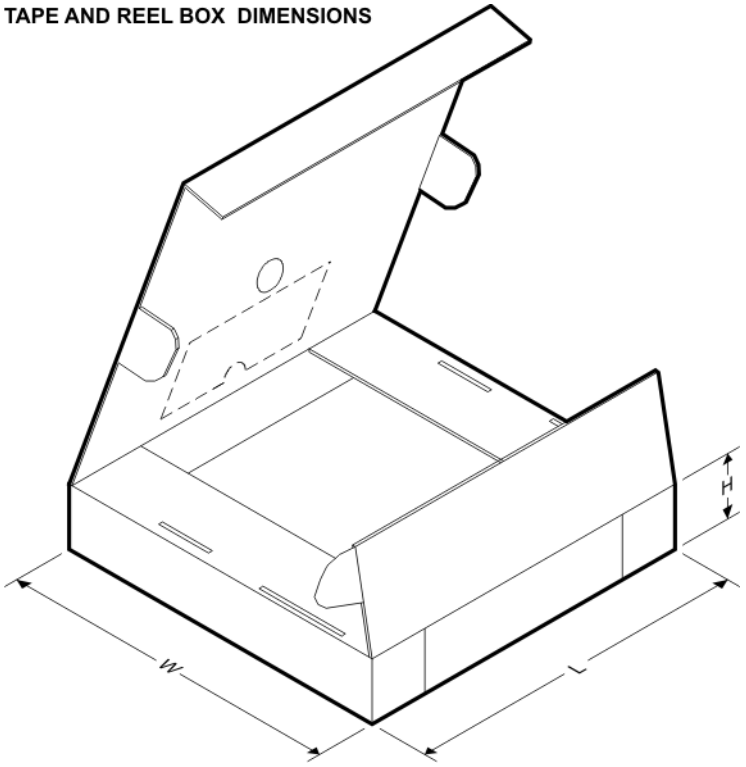
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP431ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431ADGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431BDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431BDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431CDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431CDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431DDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP431DDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432ADGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432ADGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432ADGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432ADGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432BDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432BDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432BDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP432BDGST	VSSOP	DGS	10	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

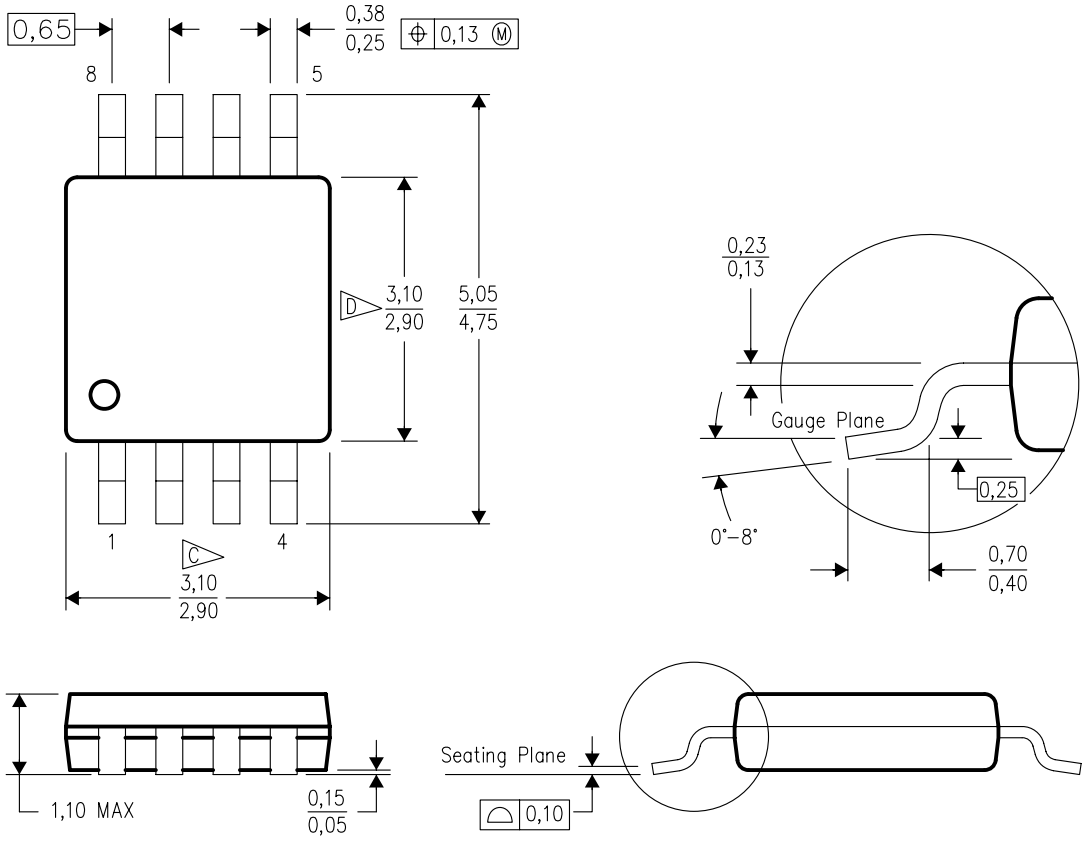
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP431ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP431ADGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP431BDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP431BDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP431CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TMP431CDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP431CDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP431CDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
TMP431DDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TMP431DDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
TMP432ADGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TMP432ADGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMP432ADGST	VSSOP	DGS	10	250	366.0	364.0	50.0
TMP432ADGST	VSSOP	DGS	10	250	358.0	335.0	35.0
TMP432BDGSR	VSSOP	DGS	10	2500	406.0	348.0	63.0
TMP432BDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMP432BDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
TMP432BDGST	VSSOP	DGS	10	250	223.0	270.0	35.0

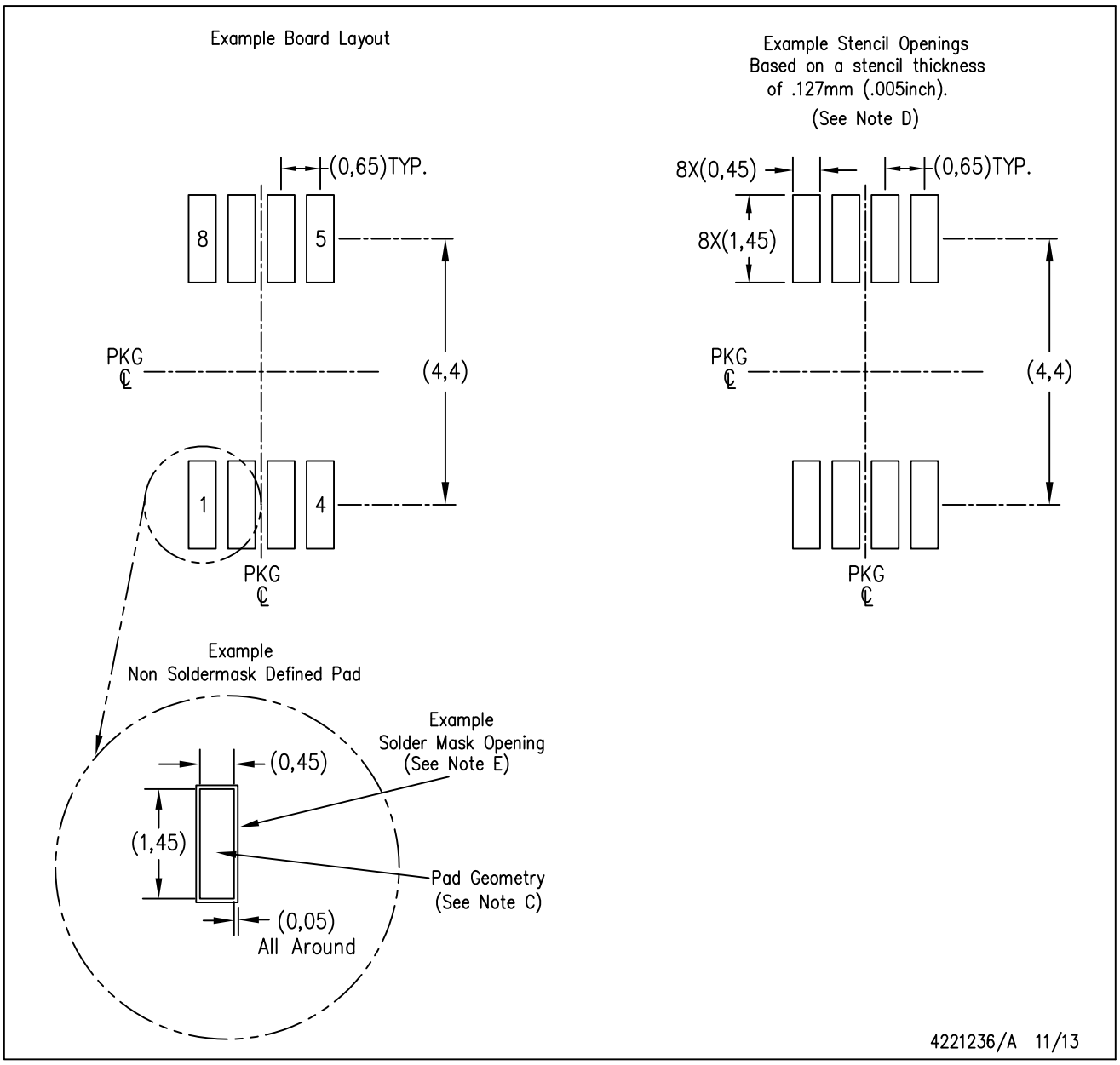
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

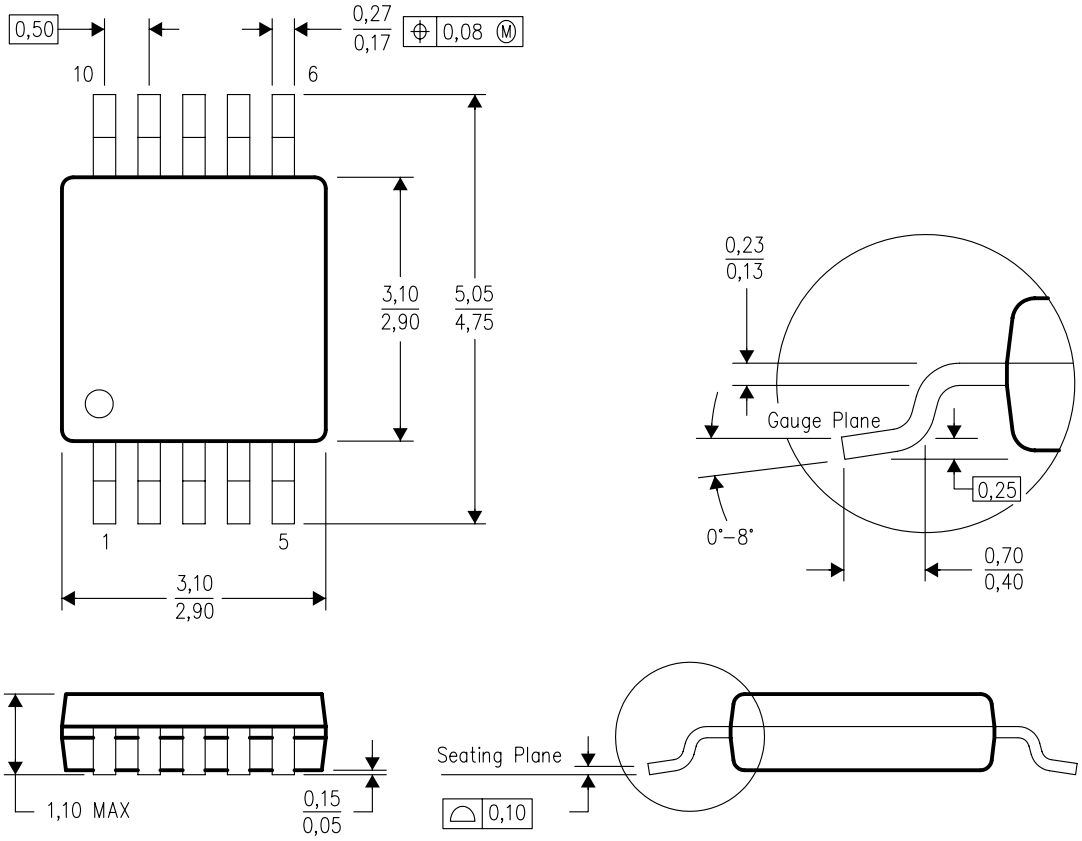
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

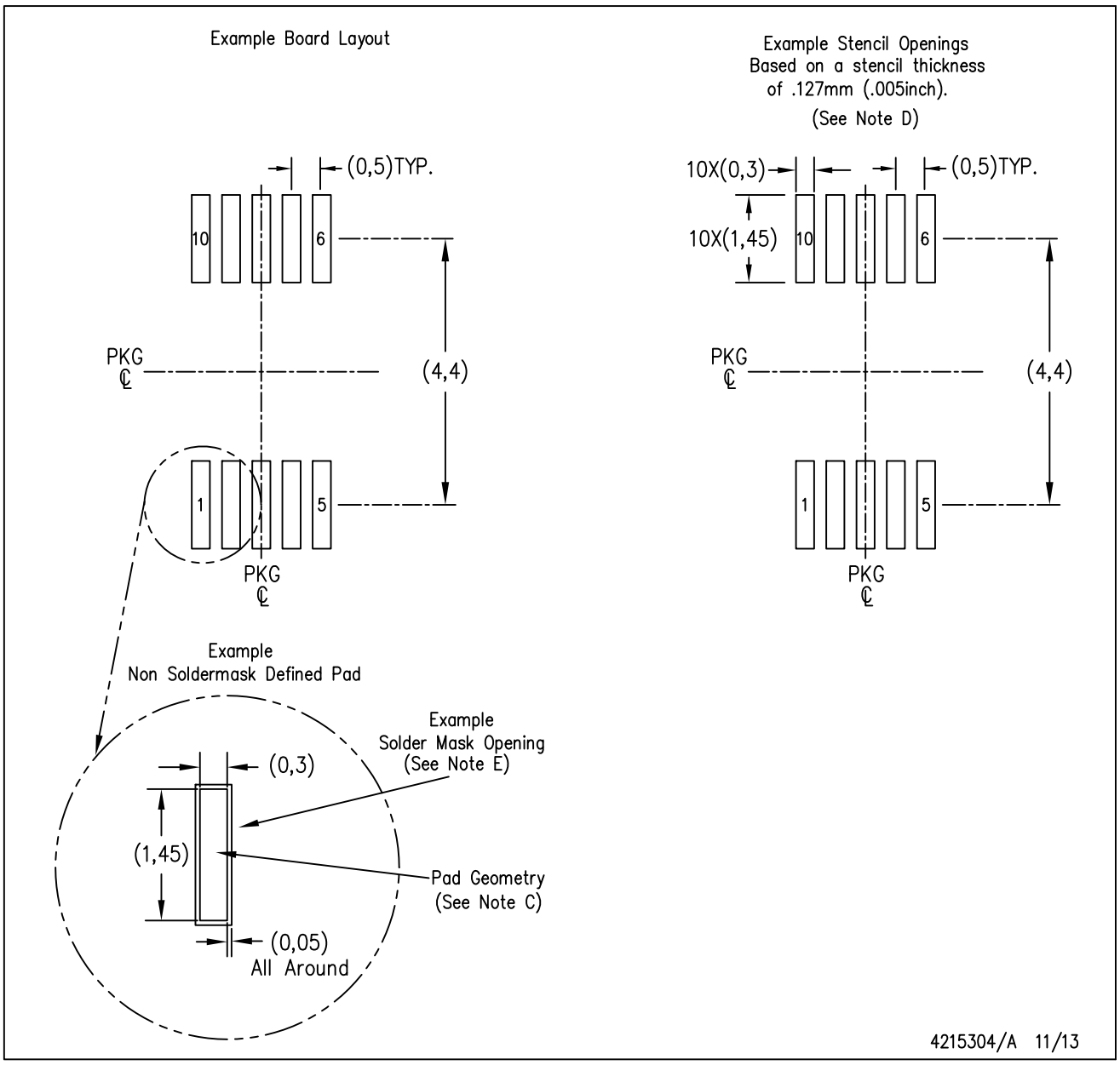
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
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E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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