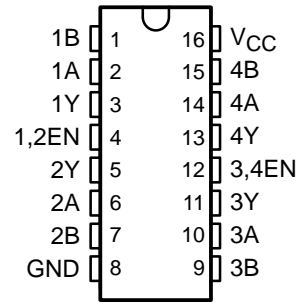


# MC3486 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

SLLS097C – JUNE 1980 – REVISED FEBRUARY 2002

- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11
- 3-State, TTL-Compatible Outputs
- Fast Transition Times
- Operates From Single 5-V Supply
- Designed to Be Interchangeable With Motorola™ MC3486

D, N, OR NS PACKAGE  
(TOP VIEW)



## description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B and ITU Recommendations V.10 and V.11. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

The MC3486 is characterized for operation from 0°C to 70°C.

### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES	
	PLASTIC SMALL OUTLINE (D, NS)	PLASTIC DIP (N)
0°C to 70°C	MC3486D MC3486NS	MC3486N

The D package is available taped and reeled. Add the suffix R to the device type (e.g., MC3486DR). The NS package is only available taped and reeled.



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# MC3486 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

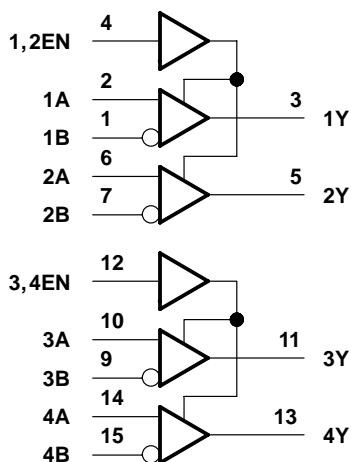
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**FUNCTION TABLE**  
(each receiver)

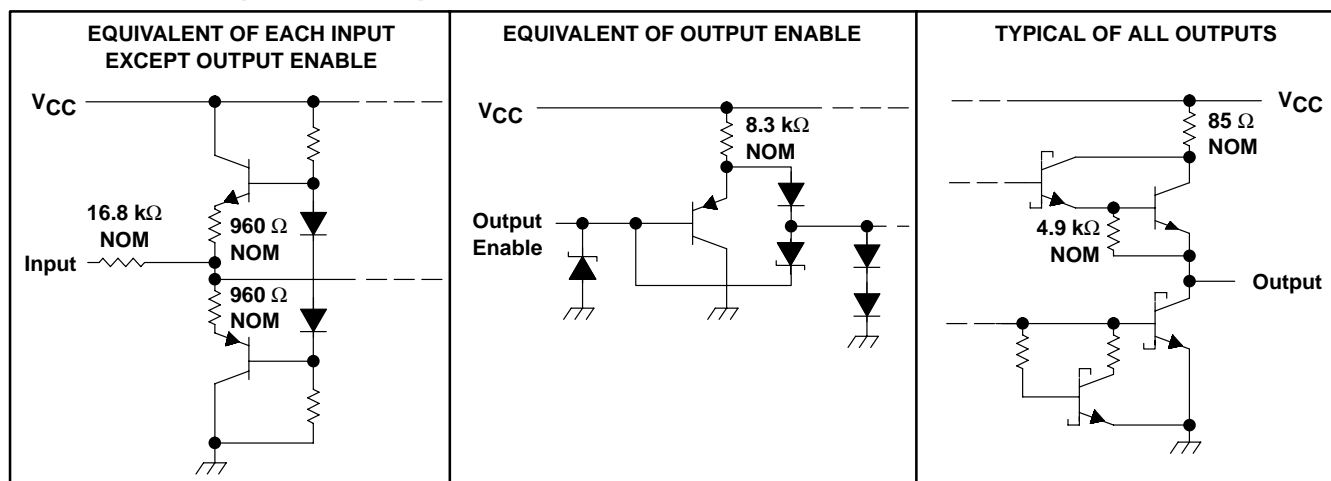
DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y
$V_{ID} \leq 0.2\text{ V}$	H	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	H	?
$V_{ID} \leq -0.2\text{ V}$	H	L
Irrelevant	L	Z
Open	H	?

H = high level, L = low level, Z = high impedance (off),  
? = indeterminate

## logic diagram (positive logic)



## schematics of inputs and outputs



# MC3486 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	8 V
Input voltage, $V_I$ (A or B inputs)	$\pm 15$ V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 25$ V
Enable input voltage	8 V
Low-level output current, $I_{OL}$	50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	73°C/W
N package	67°C/W
NS package	67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.  
 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IC}$ Common-mode input voltage			$\pm 7$	V
$V_{ID}$ Differential input voltage			$\pm 6$	V
$V_{IH}$ High-level enable input voltage	2			V
$V_{IL}$ Low-level enable input voltage			0.8	V
$T_A$ Operating free-air temperature	0		70	°C

# MC3486

## QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+}$	Differential input high-threshold voltage	$V_O = 2.7\text{ V}$ , $I_O = -0.4\text{ mA}$		0.2	V
$V_{IT-}$	Differential input low-threshold voltage	$V_O = 0.5\text{ V}$ , $I_O = -8\text{ mA}$	$-0.2^\dagger$		V
$V_{IK}$	Enable-input clamp voltage	$I_I = -10\text{ mA}$		-1.5	V
$V_{OH}$	High-level output voltage	$V_{ID} = 0.4\text{ V}$ , $I_O = -0.4\text{ mA}$ , See Note 4 and Figure 1	2.7		V
$V_{OL}$	Low-level output voltage	$V_{ID} = -0.4\text{ V}$ , $I_O = 8\text{ mA}$ , See Note 4 and Figure 1		0.5	V
$I_{OZ}$	High-impedance-state output current	$V_{IL} = 0.8\text{ V}$ , $V_{ID} = -3\text{ V}$ , $V_O = 2.7\text{ V}$		40	$\mu\text{A}$
		$V_{IL} = 0.8\text{ V}$ , $V_{ID} = 3\text{ V}$ , $V_O = 0.5\text{ V}$		-40	
$I_{IB}$	Differential-input bias current	$V_{CC} = 0\text{ V}$ or $5.25\text{ V}$ , Other inputs at $0\text{ V}$	$V_I = -10\text{ V}$	-3.25	mA
			$V_I = -3\text{ V}$	-1.5	
			$V_I = 3\text{ V}$	1.5	
			$V_I = 10\text{ V}$	3.25	
$I_{IH}$	High-level enable input current	$V_I = 5.25\text{ V}$		100	$\mu\text{A}$
		$V_I = 2.7\text{ V}$		20	
$I_{IL}$	Low-level enable input current	$V_I = -0.5\text{ V}$		-100	$\mu\text{A}$
$I_{OS}$	Short-circuit output current	$V_{ID} = 3\text{ V}$ , $V_O = 0$ , See Note 5	-15	-100	mA
$I_{CC}$	Supply current	$V_{IL} = 0$		85	mA

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 4. Refer to ANSI Standards TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.

5. Only one output should be shorted at a time.

### switching characteristics, $V_{CC} = 5\text{ V}$ , $C_L = 15\text{ pF}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$	Propagation delay time, high- to low-level output	See Figure 2		28	35	ns
$t_{PLH}$	Propagation delay time, low- to high-level output			27	30	ns
$t_{pZH}$	Output enable time to high level	See Figure 3		13	30	ns
$t_{pZL}$	Output enable time to low level			20	30	ns
$t_{PHZ}$	Output disable time from high level			26	35	ns
$t_{PLZ}$	Output disable time from low level			27	35	ns



# MC3486 QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION

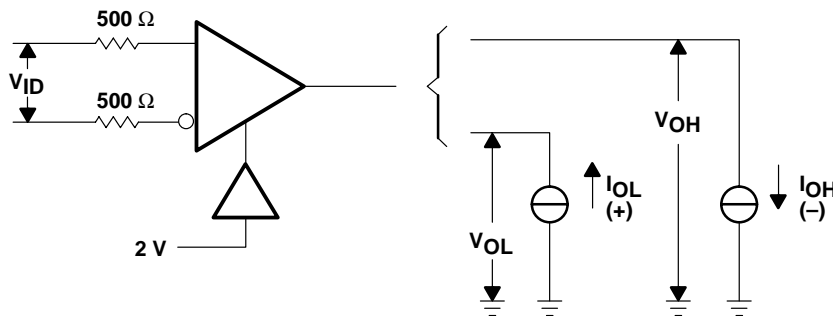
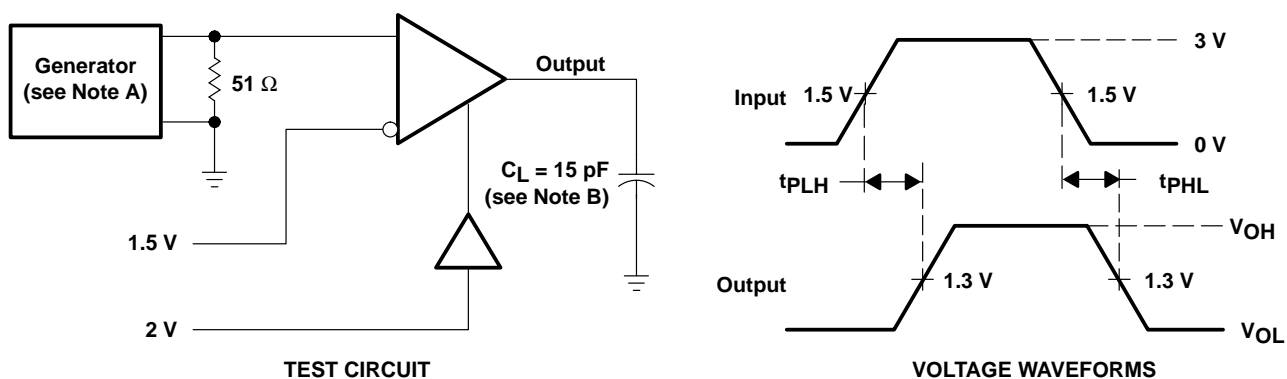


Figure 1.  $V_{OH}$ ,  $V_{OL}$



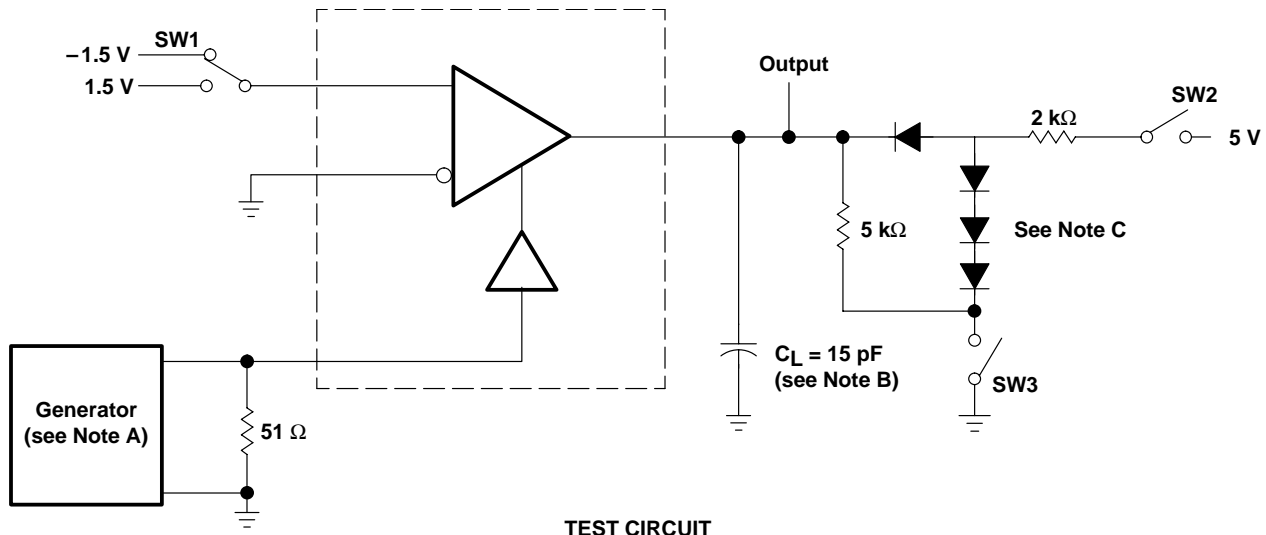
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ .  
 B.  $C_L$  includes probe and stray capacitance.

Figure 2. Test Circuit and Voltage Waveforms

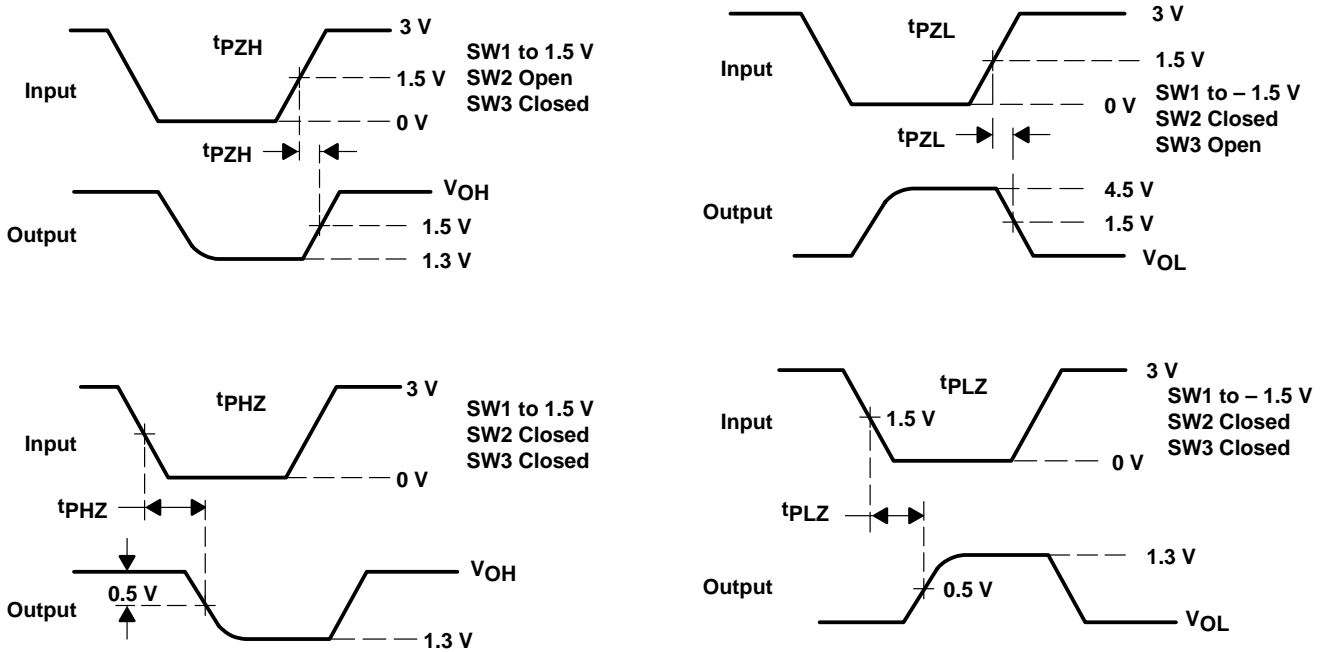
**MC3486**  
**QUADRUPLE DIFFERENTIAL LINE RECEIVER**  
**WITH 3-STATE OUTPUTS**

SLLS097C – JUNE 1980 – REVISED FEBRUARY 2002

**PARAMETER MEASUREMENT INFORMATION**



**TEST CIRCUIT**



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t<sub>r</sub> ≤ 6 ns, t<sub>f</sub> ≤ 6 ns.  
 B. C<sub>L</sub> includes probe and stray capacitance.  
 C. All diodes are 1N916 or equivalent.

**Figure 3. Test Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC3486D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	<a href="#">Samples</a>
MC3486DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	<a href="#">Samples</a>
MC3486DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	<a href="#">Samples</a>
MC3486DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	<a href="#">Samples</a>
MC3486DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	<a href="#">Samples</a>
MC3486J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
MC3486N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC3486N	<a href="#">Samples</a>
MC3486NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC3486N	<a href="#">Samples</a>
MC3486NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3486	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3486DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3486NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3486DR	SOIC	D	16	2500	333.2	345.9	28.6
MC3486NSR	SO	NS	16	2000	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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