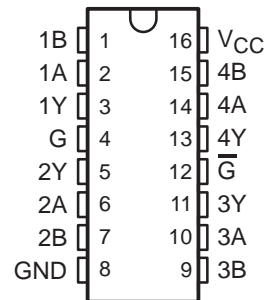


SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS008D – JUNE 1986 – REVISED MAY 1995

- Meets or Exceeds ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range –7 V to 7 V
- Input Sensitivity . . . ± 200 mV
- Input Hysteresis . . . 120 mV Typ
- High Input Impedance . . . 12 k Ω Min
- Operates from Single 5-V Supply
- Low Supply Current Requirement 35 mA Max
- Improved Speed and Power Version of the AM26LS32A

SN75ALS193 . . . D, J OR N PACKAGE
(TOP VIEW)



description

The SN75ALS193 is a monolithic quadruple line receiver with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. This device meets the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of –7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the 'ALS192 quadruple differential line driver.

The SN75ALS193 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES		OUTPUT Y
	G	Ḡ	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate,
Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

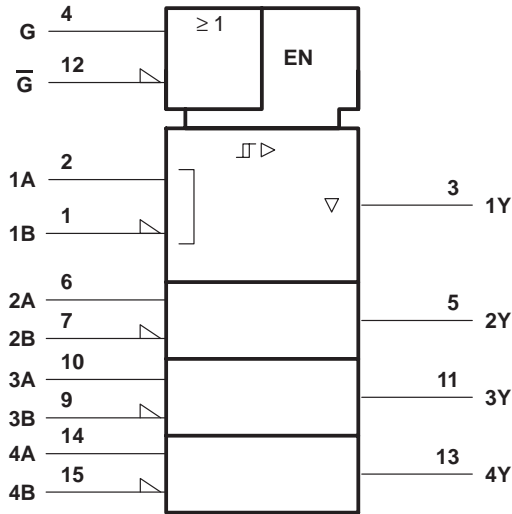
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SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER

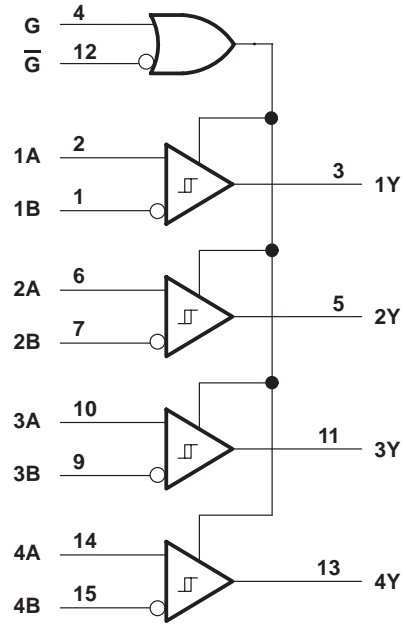
SLLS008D – JUNE 1986 – REVISED MAY 1995

logic symbol†

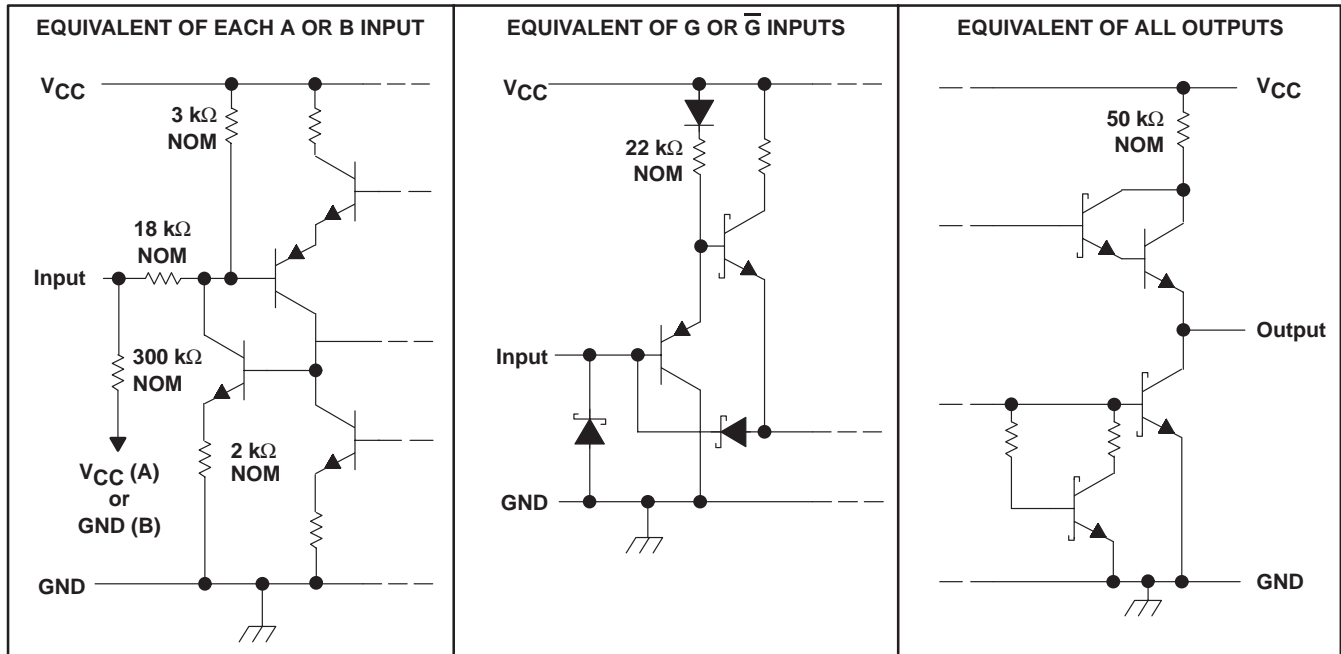


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (A or B)	± 15 V
Differential input voltage, V_{ID} (see Note 2)	± 15 V
Enable input voltage, V_I	7 V
Low-level output current, I_{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
J	1025 mW	8.2 mW/ $^\circ\text{C}$	656 mW
N	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			± 7	V
Differential input voltage, V_{ID}			± 12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	$^\circ\text{C}$

SN75ALS193

QUADRUPLE DIFFERENTIAL LINE RECEIVER

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electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage					200	mV
V _{IT-}	Negative-going input threshold voltage			-200§			mV
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})				120		mV
V _{IK}	Enable-input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, I _{OH} = -400 μA,	V _{ID} = 200 mV, See Figure 1	2.5	3.6		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{ID} = -200 mV, See Figure 1	I _{OL} = 8 mA			0.45	V
			I _{OL} = 16 mA			0.5	
I _{OZ}	High-impedance-state output current	V _{CC} = MAX	V _O = 2.4 V			20	μA
			V _O = 0.4 V			-20	
I _I	Line input current	Other input at 0, See Note 3	V _{CC} = MIN, V _I = 15 V		0.7	1.2	mA
			V _{CC} = MIN, V _I = -15 V		-1.0	-1.7	
I _{IH}	High-level enable-input current	V _{CC} = MAX	V _{IH} = 2.7 V			20	μA
			V _{IH} = MAX			100	
I _{IL}	Low-level enable-input current	V _{CC} = MAX,	V _{IL} = 0.4 V			-100	μA
	Input resistance			12	18		kΩ
I _{OS}	Short-circuit output current	V _{CC} = MAX, V _O = 0,	V _{ID} = 3 V, See Note 4	-15	-78	-130	mA
I _{CC}	Supply current	V _{CC} = MAX,	Outputs disabled		22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.

4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	V _{ID} = -2.5 V to 2.5 V, C _L = 15 pF, See Figure 2			15	22	ns
t _{PHL}	Propagation delay time, high-to-low-level output				15	22	
t _{PZH}	Output enable time to high level	C _L = 15 pF, See Figure 3			13	25	
t _{PZL}	Output enable time to low level				11	25	
t _{PHZ}	Output disable time from high level	C _L = 5 pF, See Figure 3			13	25	
t _{PLZ}	Output disable time from low level				15	22	



PARAMETER MEASUREMENT INFORMATION

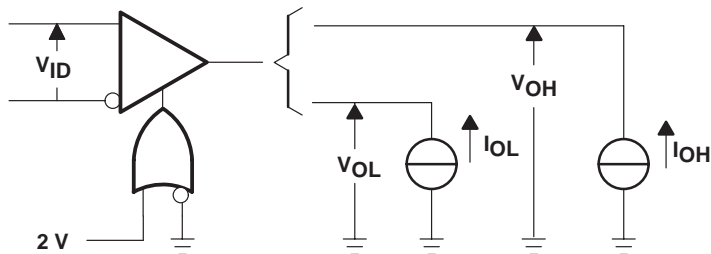
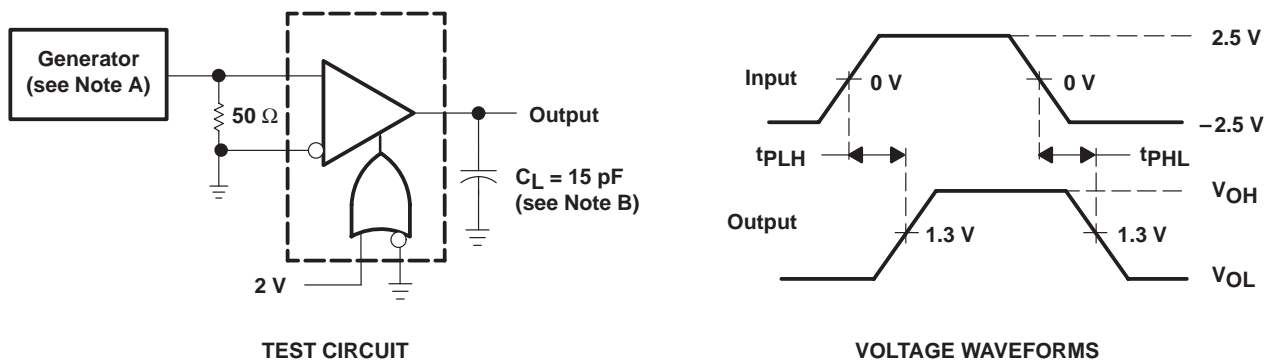


Figure 1. V_{OH} , V_{OL}



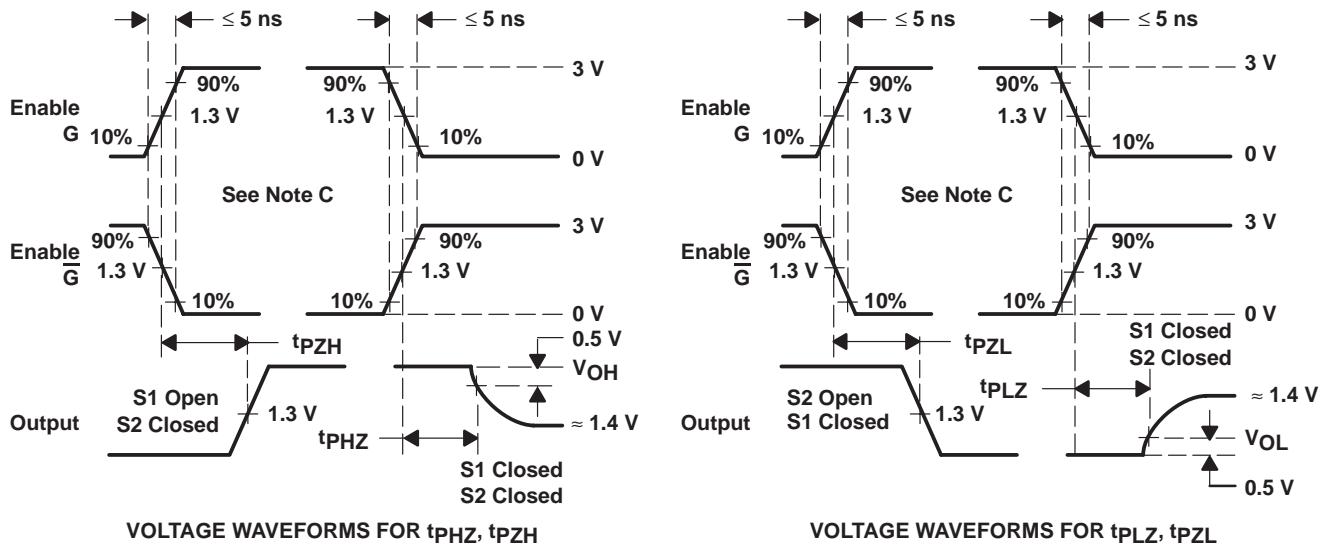
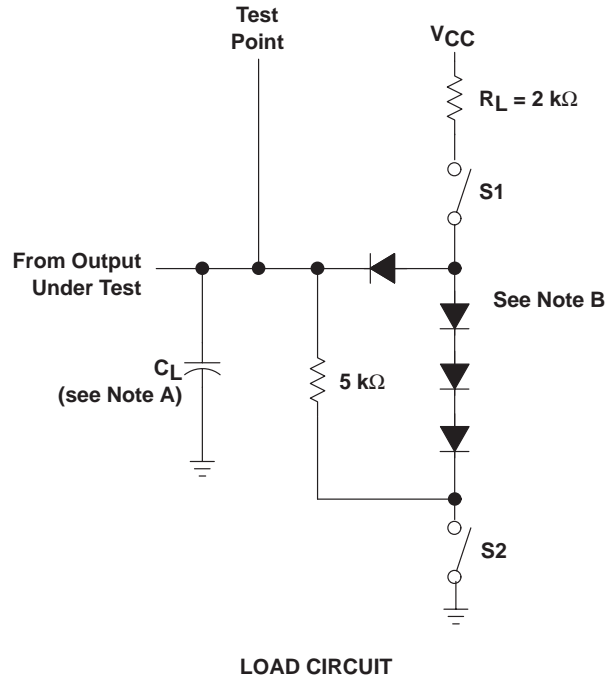
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns.
 B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Enable \overline{G} is tested with \overline{G} high; \overline{G} is tested with \overline{G} low.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

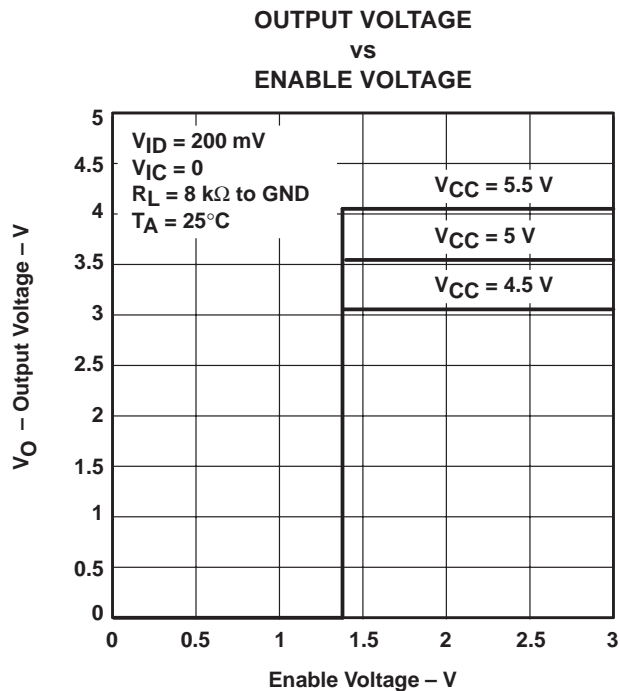


Figure 4

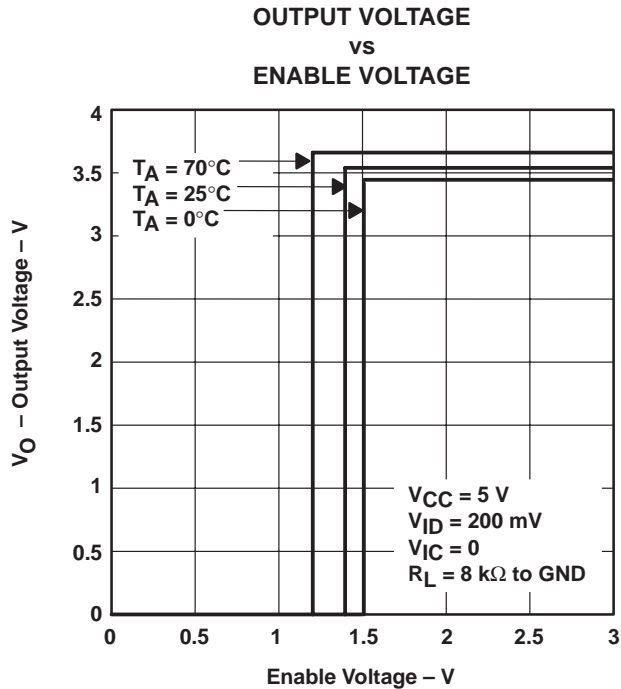


Figure 5

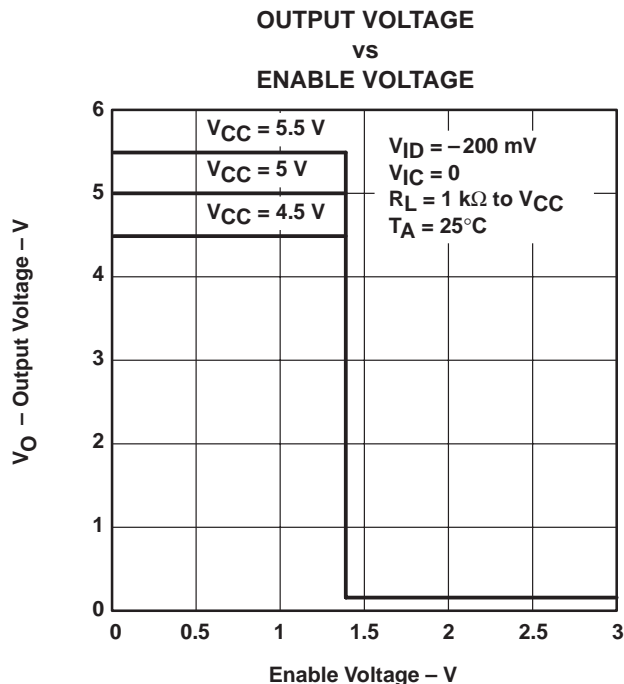


Figure 6

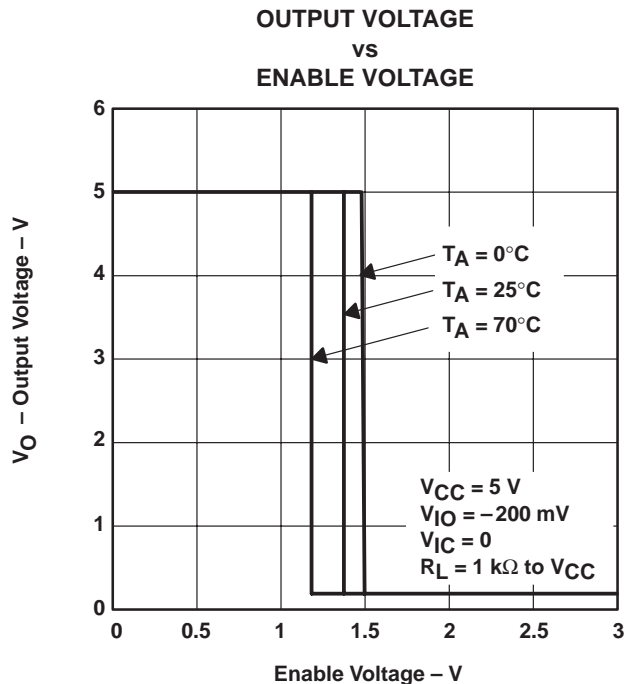


Figure 7

SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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TYPICAL CHARACTERISTICS

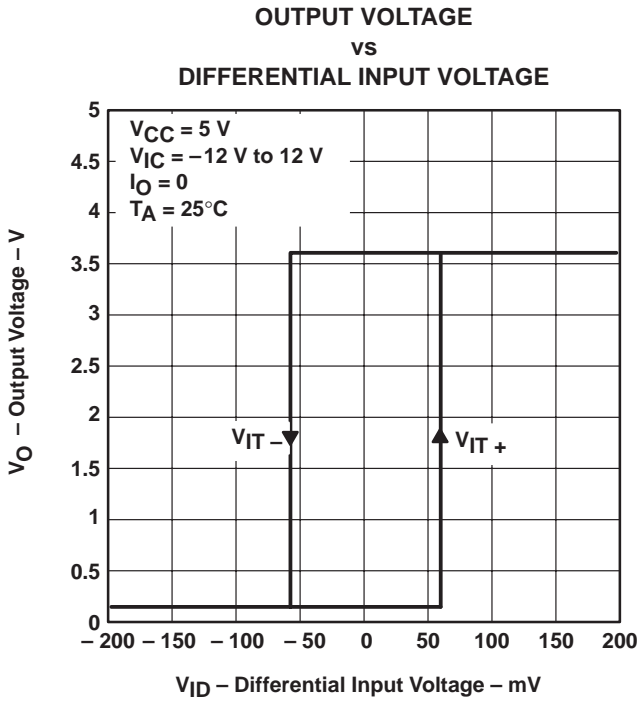


Figure 8

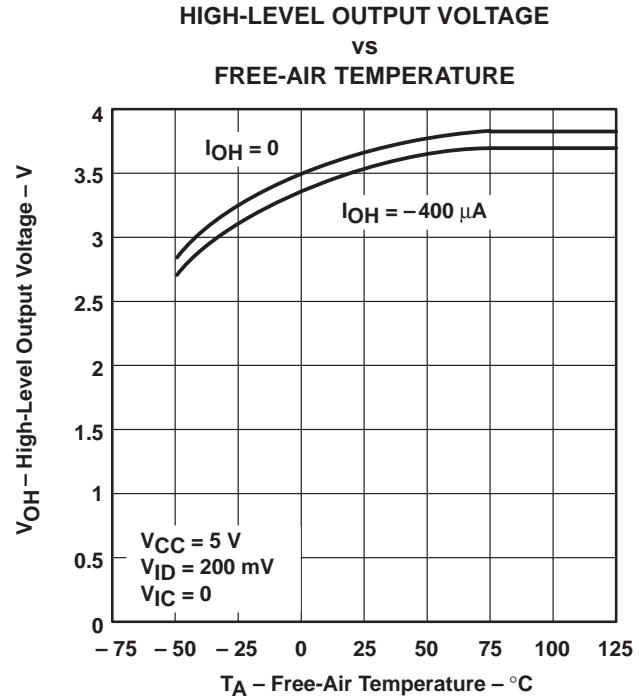


Figure 9

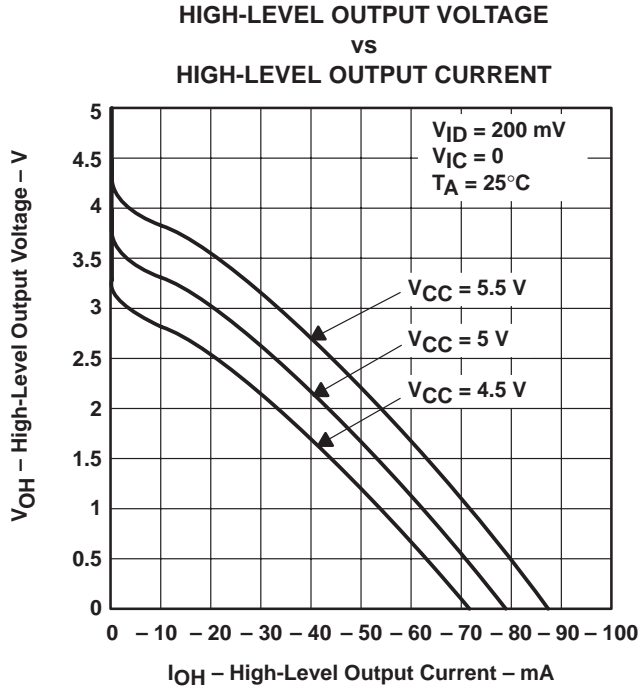


Figure 10

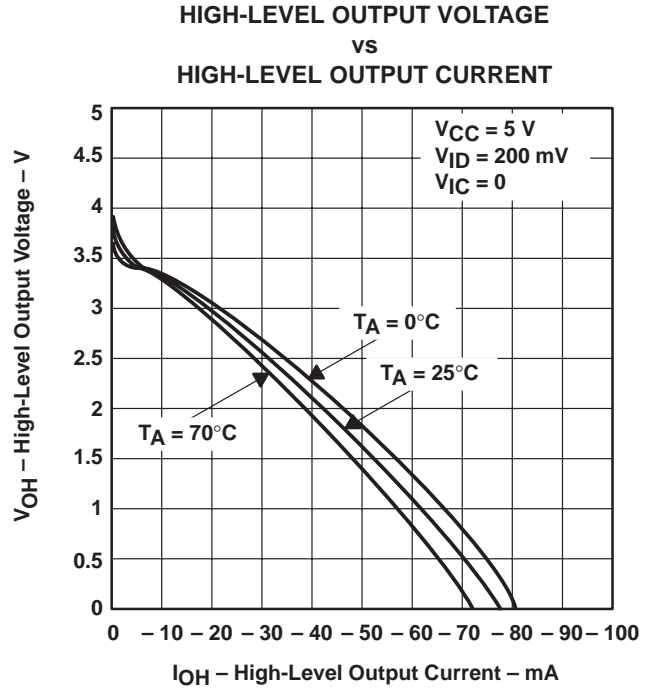


Figure 11

TYPICAL CHARACTERISTICS

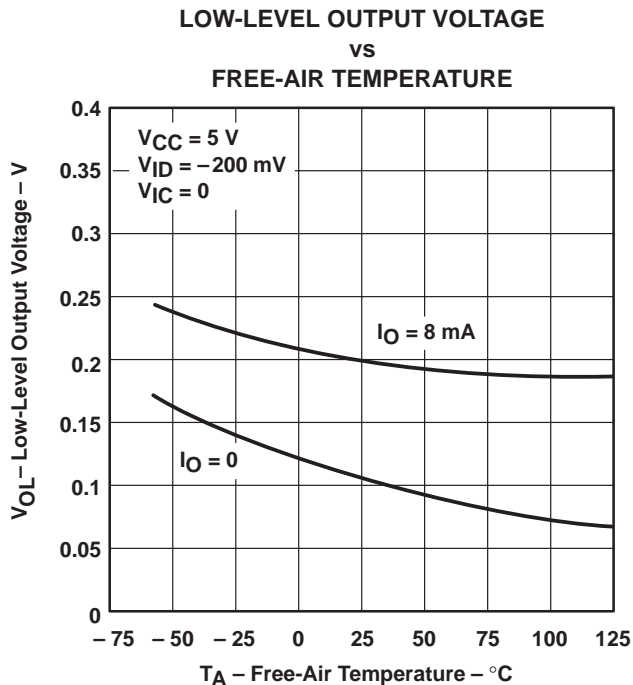


Figure 12

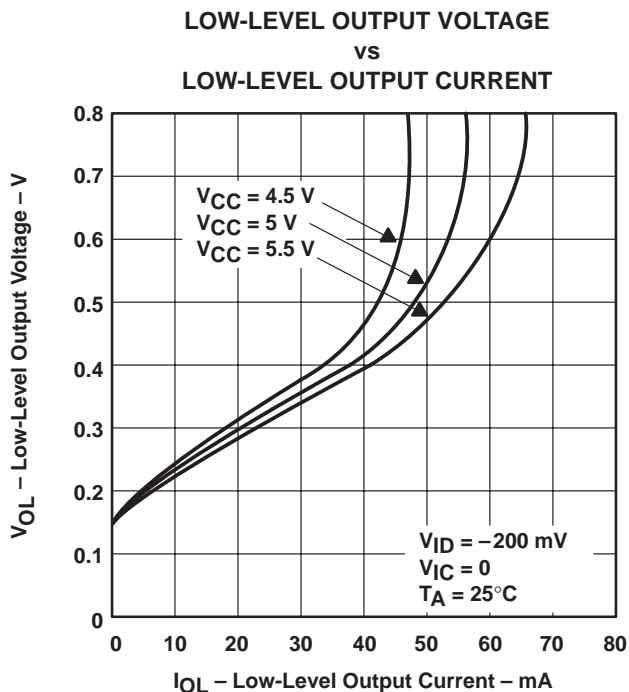


Figure 13

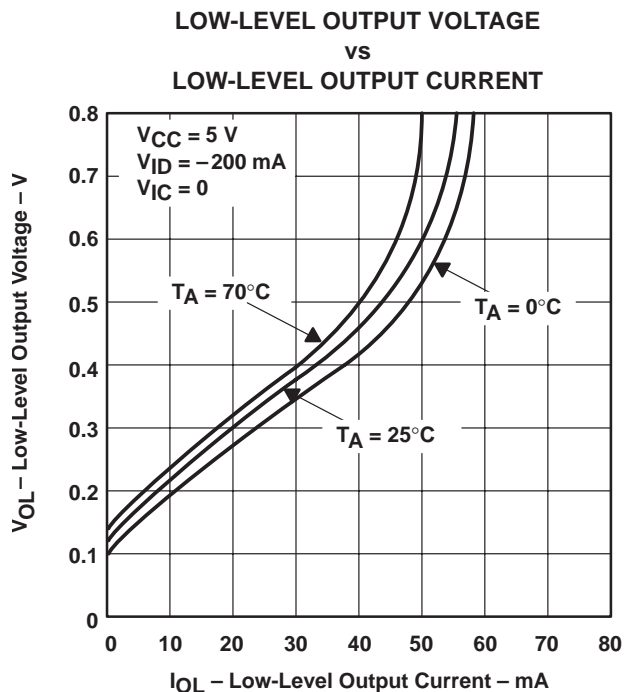


Figure 14

SN75ALS193 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

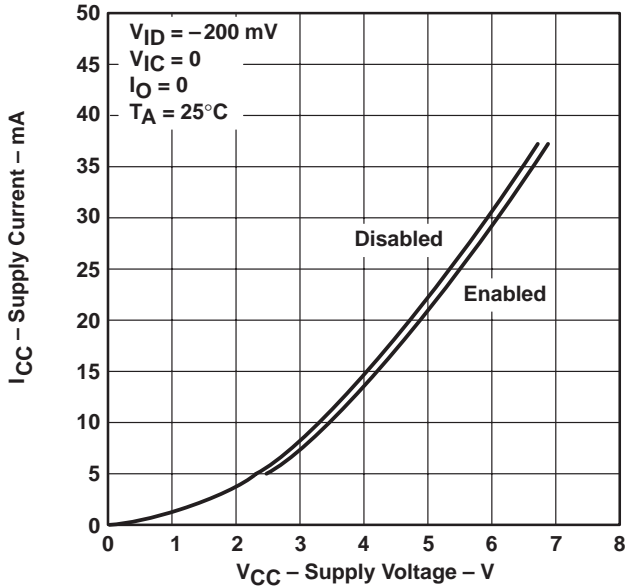


Figure 15

**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

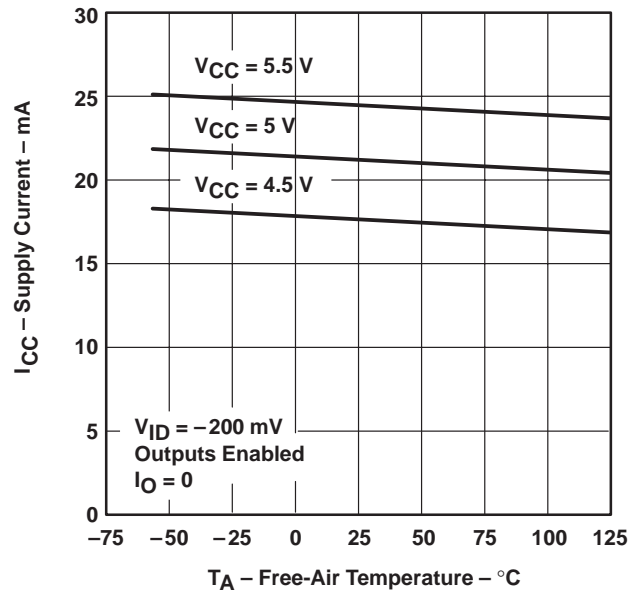


Figure 16

**SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE**

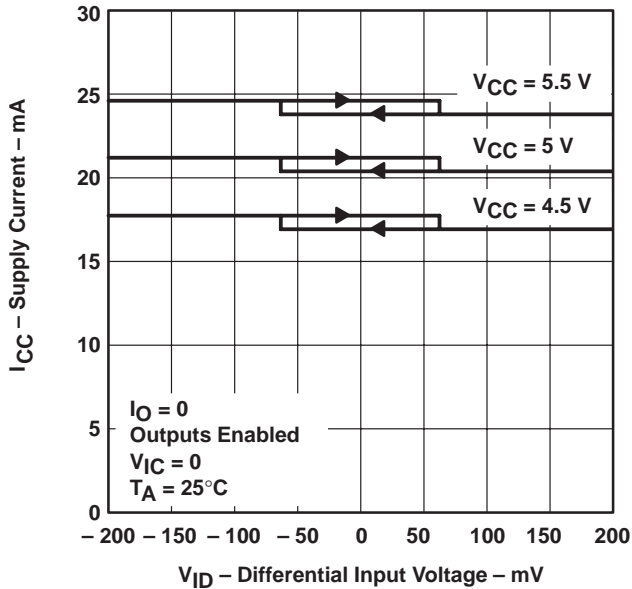


Figure 17

**SUPPLY CURRENT
vs
FREQUENCY**

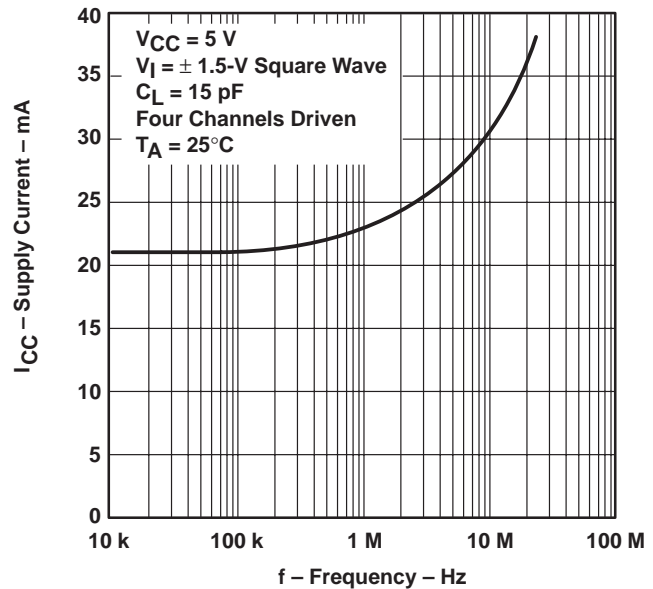


Figure 18

TYPICAL CHARACTERISTICS

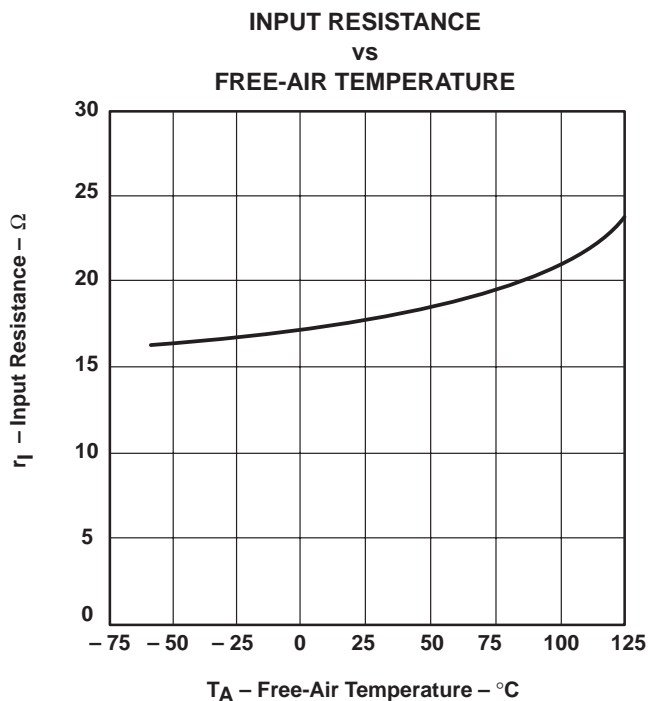


Figure 19

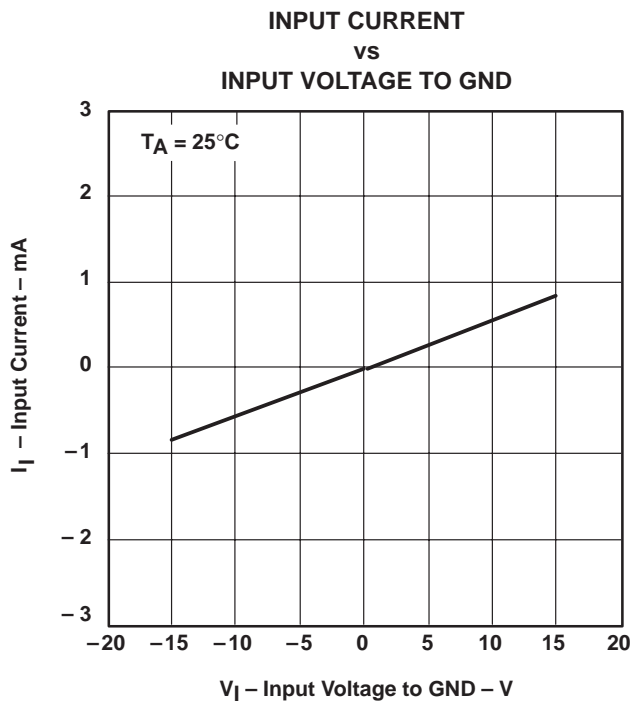


Figure 20

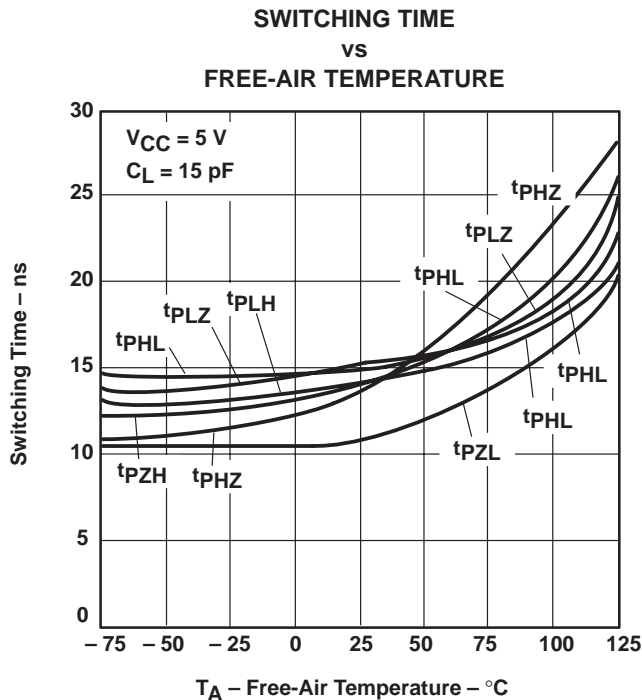


Figure 21

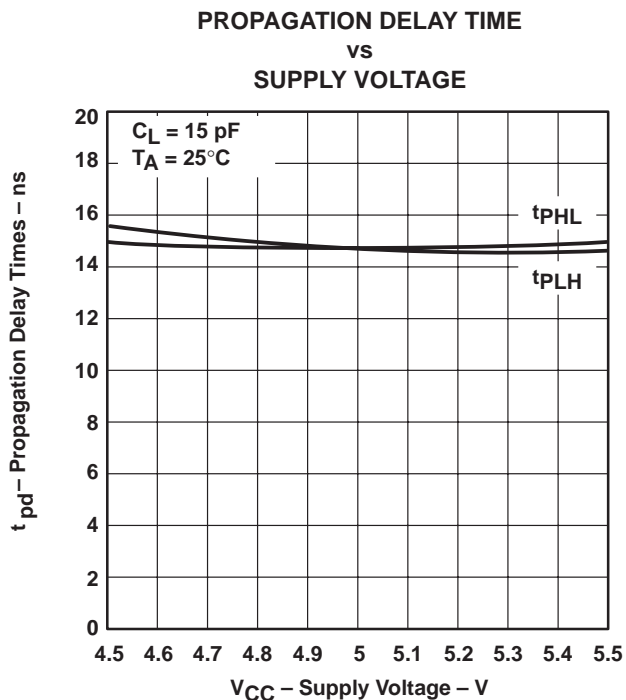


Figure 22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75ALS193D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	Samples
SN75ALS193DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	Samples
SN75ALS193DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	Samples
SN75ALS193DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	Samples
SN75ALS193DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	Samples
SN75ALS193DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS193	Samples
SN75ALS193J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN75ALS193N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS193N	Samples
SN75ALS193NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS193N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS193DR	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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