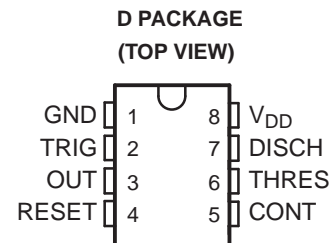


LinCMOS™ TIMER

 Check for Samples: [TLC555-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Very Low Power Consumption
 - 1 mW Typ at $V_{DD} = 5\text{ V}$
- Capable of Operation in Astable Mode
- CMOS Output Capable of Swinging Rail to Rail
- High Output-Current Capability
 - Sink 100 mA Typ
 - Source 10 mA Typ
- Output Fully Compatible With CMOS, TTL, and MOS
- Low Supply Current Reduces Spikes During Output Transitions
- Single-Supply Operation From 2 V to 15 V
- Functionally Interchangeable With the NE555; Has Same Pinout



DESCRIPTION AND ORDERING INFORMATION

The TLC555 is a monolithic timing circuit fabricated using the TI LinCMOS™ process. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Because of its high input impedance, this device uses smaller timing capacitors than those used by the NE555. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage.

Like the NE555, the TLC555 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT). When the trigger input (TRIG) falling below the trigger level sets the flip-flop, and the output goes high. Having TRIG above the trigger level and the threshold input (THRES) above the threshold level resets the flip-flop, and the output is low. The reset input (RESET) can override all other inputs, and a possible use is to initiate a new timing cycle. RESET going low resets the flip-flop, and the output is low. Whenever the output is low, a low-impedance path exists between the discharge terminal (DISCH) and GND. Tie all unused inputs to an appropriate logic level to prevent false triggering.

The advantage of the TLC555-Q1 is that it exhibits greatly reduced supply-current spikes during output transitions. Although the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the main reason the TLC555-Q1 is able to have low current spikes is due to its edge rates. This minimizes the need for the large decoupling capacitors required by the NE555.

The TLC555 is characterized for operation over the full automotive temperature range of -40°C to 125°C .

ORDERING INFORMATION⁽¹⁾

| T_A | V_{DD} | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|--|-------------|------------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | 5 V to 15 V | SOIC – D | Reel of 2500 | TLC555QDRQ1 | TL555Q |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

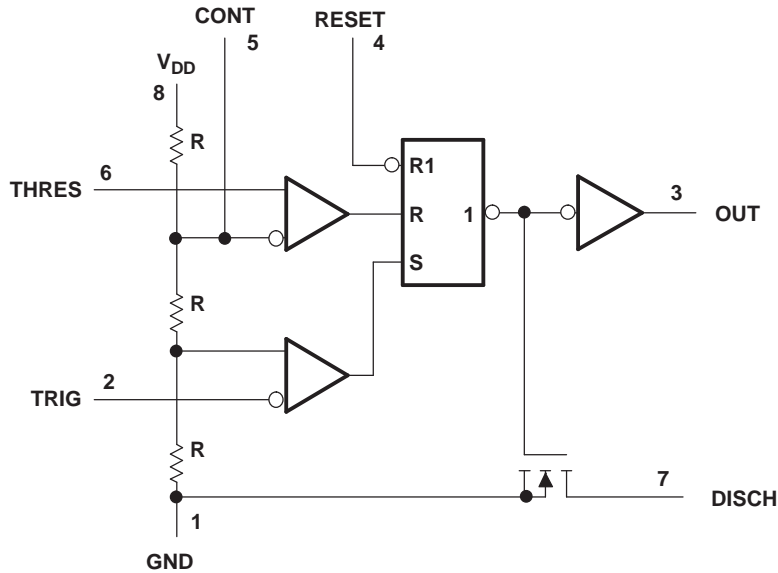
LinCMOS is a trademark of Texas Instruments.

Table 1. FUNCTION TABLE

| RESET VOLTAGE ⁽¹⁾ | TRIGGER VOLTAGE ⁽¹⁾ | THRESHOLD VOLTAGE ⁽¹⁾ | OUTPUT | DISCHARGE SWITCH |
|------------------------------|--------------------------------|----------------------------------|---------------------------|------------------|
| <MIN | Irrelevant | Irrelevant | L | On |
| >MAX | <MIN | Irrelevant | H | Off |
| >MAX | >MAX | >MAX | L | On |
| >MAX | >MAX | <MIN | As previously established | |

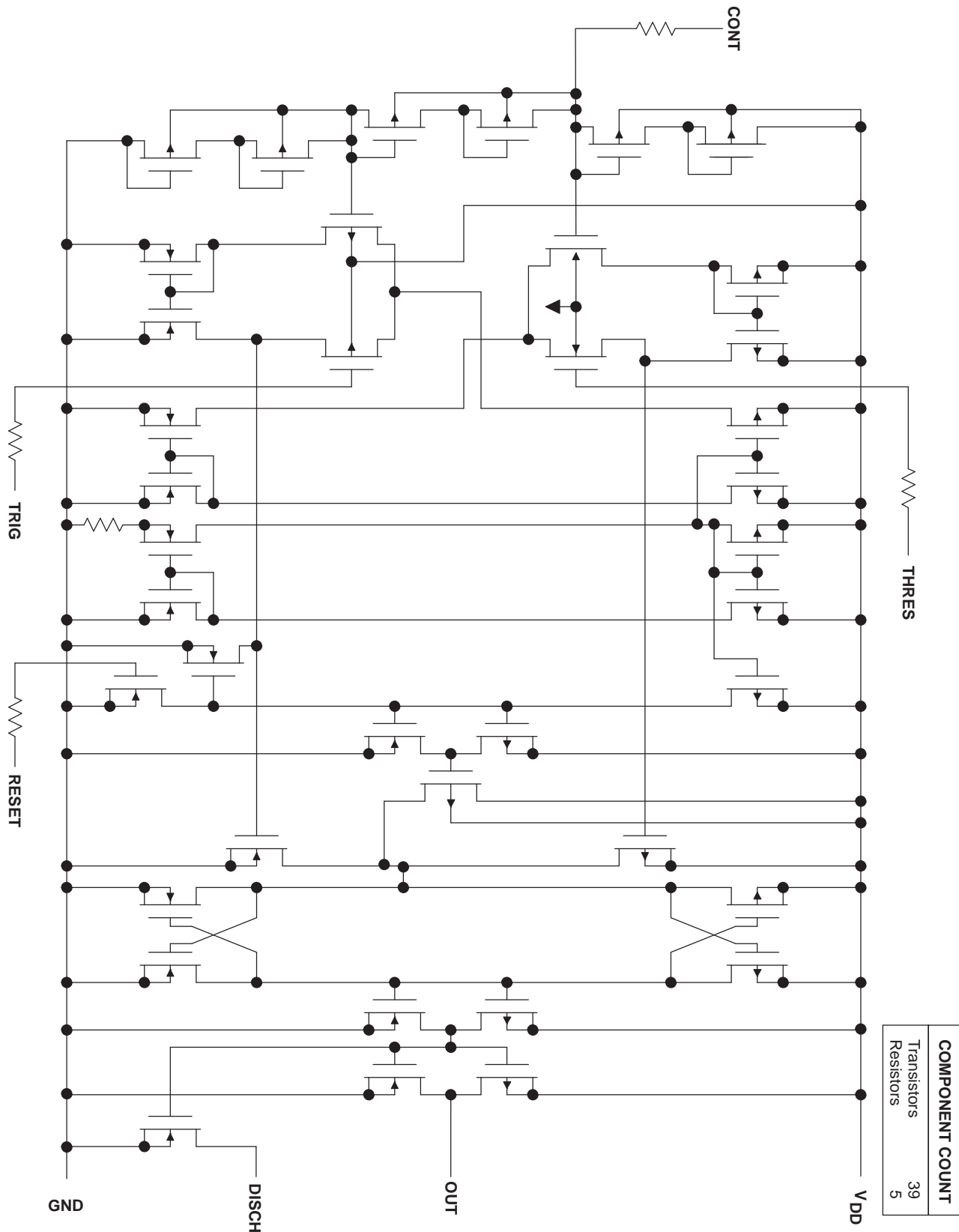
(1) For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

FUNCTIONAL BLOCK DIAGRAM



A. RESET can override TRIG, which can override THRES.

Figure 1. EQUIVALENT SCHEMATIC



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|--------------------------------------|------------------------------|-----------------|------|
| V _{DD} | Supply voltage ⁽²⁾ | | 18 | V |
| V _I | Input voltage range | -0.3 | V _{DD} | V |
| | Sink current, discharge or output | | 150 | mA |
| I _O | Source current, output | | 15 | mA |
| | Continuous total power dissipation | See Dissipation Rating Table | | |
| T _A | Operating free-air temperature range | -40 | 125 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |
| | HBM (human-body model) ESD | | 1000 | V |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network GND.

Dissipation Ratings

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 125°C POWER RATING |
|---------|---------------------------------------|--|--|
| D | 725 mW | 5.8 mW/°C | 145 mW |

Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|------|
| V _{DD} | Supply voltage | 2 | 15 | V |
| T _A | Operating free-air temperature | -40 | 125 | °C |

Electrical Characteristics

$V_{DD} = 5\text{ V}$, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T_A ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|--|------------------------------------|--------------------------|----------------------|------|-------|------|------|
| V_{IT} | Threshold voltage | | 25°C | 2.8 | 3.3 | 3.8 | V |
| | | | Full range | 2.7 | | 3.9 | |
| I_{IT} | Threshold current | | 25°C | | 10 | | pA |
| | | | Full range | | 5000 | | |
| $V_{I(TRIG)}$ | Trigger voltage | | 25°C | 1.36 | 1.66 | 1.96 | V |
| | | | Full range | 1.26 | | 2.06 | |
| $I_{I(TRIG)}$ | Trigger current | | 25°C | | 10 | | pA |
| | | | Full range | | 5000 | | |
| $V_{I(RESET)}$ | Reset voltage | | 25°C | 0.4 | 1.1 | 1.5 | V |
| | | | Full range | 0.3 | | 1.8 | |
| $I_{I(RESET)}$ | Reset current | | 25°C | | 10 | | pA |
| | | | Full range | | 5000 | | |
| Control voltage (open-circuit) as a percentage of supply voltage | | | Full range | | 66.7% | | |
| | Discharge-switch on-state voltage | $I_{OL} = 10\text{ mA}$ | 25°C | | 0.14 | 0.5 | V |
| | | | Full range | | | 0.6 | |
| | Discharge-switch off-state current | | 25°C | | 0.1 | | nA |
| | | | Full range | | 120 | | |
| V_{OH} | High-level output voltage | $I_{OH} = -1\text{ mA}$ | 25°C | 4.1 | 4.8 | | V |
| | | | Full range | 4.1 | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 8\text{ mA}$ | 25°C | | 0.21 | 0.4 | V |
| | | | Full range | | | 0.6 | |
| | | $I_{OL} = 5\text{ mA}$ | 25°C | | 0.13 | 0.3 | |
| | | | Full range | | | 0.45 | |
| | | $I_{OL} = 3.2\text{ mA}$ | 25°C | | 0.08 | 0.3 | |
| | | | Full range | | | 0.4 | |
| I_{DD} | Supply current ⁽²⁾ | | 25°C | | 170 | 350 | μA |
| | | | Full range | | | 700 | |

(1) Full-range T_A is -40°C to 125°C .

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

Electrical Characteristics

$V_{DD} = 15\text{ V}$, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T_A ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|----------------|--|--------------------------|----------------------|------|-------|-------|------|
| V_{IT} | Threshold voltage | | 25°C | 9.45 | 10 | 10.55 | V |
| | | | Full range | 9.35 | | 10.65 | |
| I_{IT} | Threshold current | | 25°C | | 10 | | pA |
| | | | Full range | | 5000 | | |
| $V_{I(TRIG)}$ | Trigger voltage | | 25°C | 4.65 | 5 | 5.35 | V |
| | | | Full range | 4.55 | | 5.45 | |
| $I_{I(TRIG)}$ | Trigger current | | 25°C | | 10 | | pA |
| | | | Full range | | 5000 | | |
| $V_{I(RESET)}$ | Reset voltage | | 25°C | 0.4 | 1.1 | 1.5 | V |
| | | | Full range | 0.3 | | 1.8 | |
| $I_{I(RESET)}$ | Reset current | | 25°C | | 10 | | pA |
| | | | Full range | | 5000 | | |
| | Control voltage (open-circuit) as a percentage of supply voltage | | Full range | | 66.7% | | |
| | Discharge-switch on-state voltage | $I_{OL} = 100\text{ mA}$ | 25°C | | 0.77 | 1.7 | V |
| | | | Full range | | | 1.8 | |
| | Discharge switch off-state current | | 25°C | | 0.1 | | nA |
| | | | Full range | | 120 | | |
| V_{OH} | High-level output voltage | $I_{OH} = -10\text{ mA}$ | 25°C | 12.5 | 14.2 | | V |
| | | | Full range | 12.5 | | | |
| | | $I_{OH} = -5\text{ mA}$ | 25°C | 13.5 | 14.6 | | |
| | | | Full range | 13.5 | | | |
| | | $I_{OH} = -1\text{ mA}$ | 25°C | 14.2 | 14.9 | | |
| | | | Full range | 14.2 | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 100\text{ mA}$ | 25°C | | 1.28 | 3.2 | V |
| | | | Full range | | | 3.8 | |
| | | $I_{OL} = 50\text{ mA}$ | 25°C | | 0.63 | 1 | |
| | | | Full range | | | 1.5 | |
| | | $I_{OL} = 10\text{ mA}$ | 25°C | | 0.12 | 0.3 | |
| | | | Full range | | | 0.45 | |
| I_{DD} | Supply current ⁽²⁾ | | 25°C | | 360 | 600 | μA |
| | | | Full range | | | 1000 | |

(1) Full-range T_A is -40°C to 125°C .

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

Operating Characteristics

 $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|--|-----|-----|-----|------|
| | Initial error of timing interval ⁽¹⁾ | $V_{DD} = 5\text{ V to }15\text{ V}$, $C_T = 0.1\ \mu\text{F}$, $R_A = R_B = 1\ \text{k}\Omega\text{ to }100\ \text{k}\Omega^{(2)}$ | | 1 | 3 | % |
| | Supply voltage sensitivity of timing interval | $V_{DD} = 5\text{ V to }15\text{ V}$, $C_T = 0.1\ \mu\text{F}$, $R_A = R_B = 1\ \text{k}\Omega\text{ to }100\ \text{k}\Omega^{(2)}$ | | 0.1 | 0.5 | %/V |
| t_r | Output pulse rise time | $R_L = 10\ \text{M}\Omega$, $C_L = 10\ \text{pF}$ | | 20 | 75 | ns |
| t_f | Output pulse fall time | $R_L = 10\ \text{M}\Omega$, $C_L = 10\ \text{pF}$ | | 15 | 60 | ns |
| f_{max} | Maximum frequency in astable mode | $R_A = 470\ \Omega$, $C_T = 200\ \text{pF}$, $R_B = 200\ \Omega^{(2)}$ | 1.2 | 2.1 | | MHz |

- (1) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
- (2) R_A , R_B , and C_T are as defined in [Figure 2](#).

TYPICAL CHARACTERISTICS

**DISCHARGE SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE**

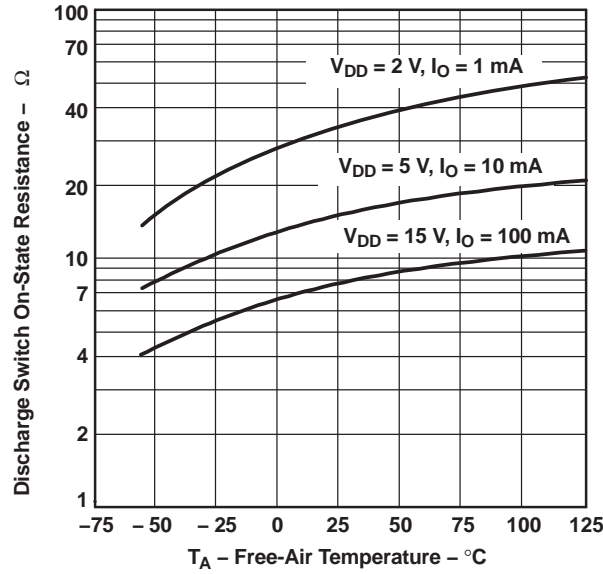
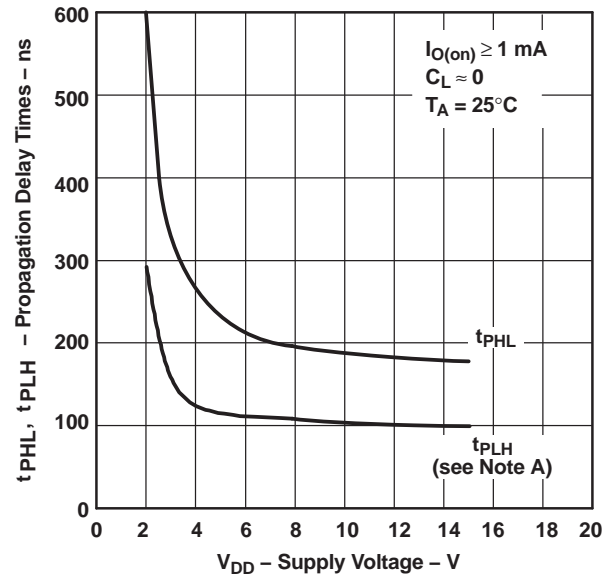


Figure 2.

**PROPAGATION DELAY TIMES TO DISCHARGE
OUTPUT FROM TRIGGER AND THRESHOLD
SHORTED TOGETHER
vs
SUPPLY VOLTAGE**



A. The effects of the load resistance on these values must be taken into account separately.

Figure 3.

APPLICATION INFORMATION

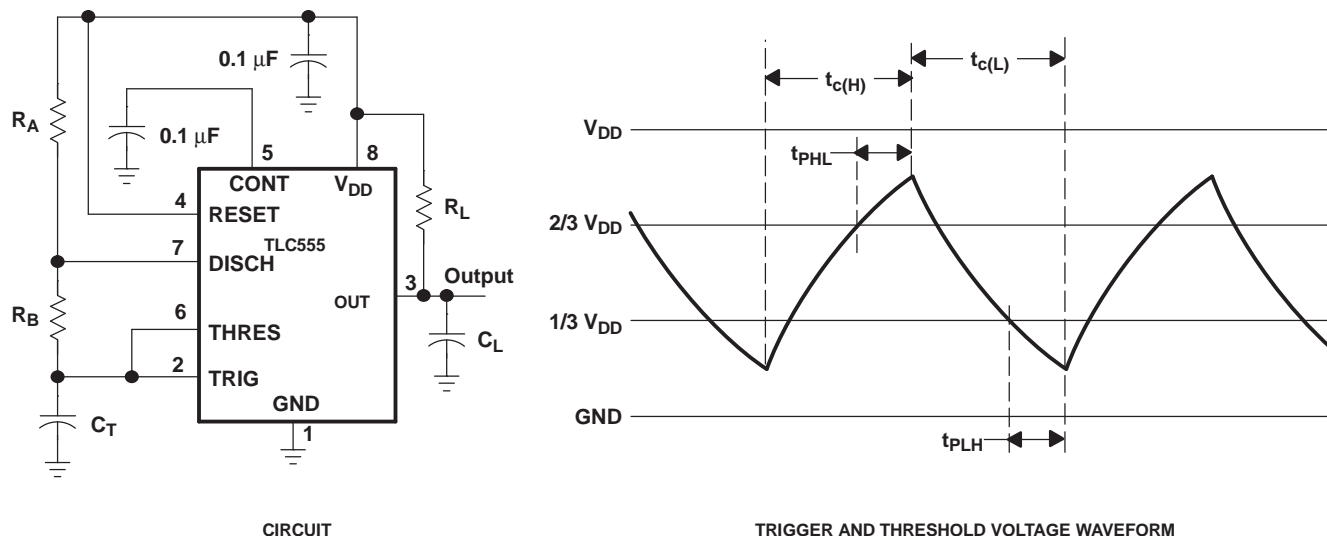


Figure 4. Astable Operation

Connecting TRIG to THRES, as shown in Figure 4, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the threshold voltage level (approximately $0.67 V_{DD}$) and then discharges through R_B only to the value of the trigger voltage level (approximately $0.33 V_{DD}$). The output is high during the charging cycle ($t_{c(H)}$) and low during the discharge cycle ($t_{c(L)}$). The values of R_A , R_B , and C_T control the duty cycle as shown in the following equations.

$$t_{c(H)} \approx C_T (R_A + R_B) \ln 2 \quad (\ln 2 = 0.693)$$

$$t_{c(L)} \approx C_T R_B \ln 2$$

$$\text{Period} = t_{c(H)} + t_{c(L)} \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_{c(L)}}{t_{c(H)} + t_{c(L)}} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1- μF capacitor at CONT in Figure 4 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay times from the TRIG and THRES inputs to DISCH. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance (r_{on}) during discharge adds to R_B to provide another source of timing error in the calculation when R_B is very low or r_{on} is very high.

The following equations provide better agreement with measured values.

$$t_{c(H)} = C_T (R_A + R_B) \ln \left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})}\right) \right] + t_{PHL}$$

$$t_{c(L)} = C_T (R_B + r_{on}) \ln \left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)}\right) \right] + t_{PLH}$$

These equations and those given previously are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln 2 at low frequencies and ln 3 at extremely high frequencies. For a duty cycle close to 50%, one can substitute an appropriate constant for the

logarithmic terms with good results. Duty cycles less than 50% $\frac{t_{c(H)}}{t_{c(H)} + t_{c(L)}}$ require that $\frac{t_{c(H)}}{t_{c(L)}} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, a voltage applied to CONT can set the trip point on TRIG. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500-µA bias provides good results.

REVISION HISTORY

| Changes from Revision Original (October 2006) to Revision A | Page |
|---|------|
| • Changed next-to-last paragraph in Description and Ordering Information section | 1 |
| • Changed top-side marking | 1 |
| • In the 5-V and 15-V Electrical Characteristics tables, changed all "MAX" entries in the T _A column to "Full range" | 5 |
| • Deleted the last Electrical Characteristics table, which contained only redundant data | 7 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| TLC555QDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU Call TI | Level-1-260C-UNLIM | -40 to 125 | TL555Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC555-Q1 :

- Catalog: [TLC555](#)
- Military: [TLC555M](#)



NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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