# Symphony™ DSP56371

#### Target Applications

- Audio effects
- DVD receivers
- Audio/video receivers
- Car radios/amplifiers
- Mini systems
- Virtual headphones
- · Virtual speaker systems
- TVs

#### Overview

The Symphony™ DSP56371 is designed to support a multitude of digital signal processing applications requiring a lot of horsepower in a small package. In order to serve the specific needs of consumer and automotive applications, the DSP56371 includes a powerful set of built-in audio peripherals and embedded software modules, plus a wealth of audio processing functions, including an operating system, various equalization algorithms, compression, signal generator, tone control, fade/balance, level meter/spectrum analyzer and many more. It also supports various matrix decoders and sound-field processing algorithms.

The DSP56371 uses the high-performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs), combined with the audio signal processing capability of the Symphony DSP Family. This design retains code compatibility with Freescale's popular DSP56000 core family of DSPs, but provides twice the level of performance.

Symphony DSP56371			
PLL	Synthesized	SHI	
OnCE/JTAG	Onyx™ DSP Core	ESAI 0	
EFCOP	ROM 128K x 24	ESAI 1	
Timer		DAX	
RAM 88K x 24			

#### **Benefits Features**

• High-performance 150 or 180 million instructions per second (MIPS) using an internal 150 or 180 MHz clock at 1.25V

High-Performance 24-bit DSP56300 Core

- Object code compatibility with the DSP56000 core
- · Highly parallel instruction set
- Data arithmetic logic unit (ALU) with a 24 x 24-bit multiplier accumulator and a 56-bit barrel shifter
- Six-channel DMA controller
- Program controller with position independent code support and instruction cache support
- Very low-power, fully static CMOS design with operating frequencies down to DC
- STOP and WAIT low-power standby modes

- · Designed to provide the high performance necessary for many audio applications
- Allows easy migration from DSP56000 Family devices
- Enhances performance by allowing multiple instructions to be executed in a single cycle
- Allows implementation of double-precision (48-bit) arithmetic operations
- Allows for data movement independent from core
- Supports flexibility in code development

#### **On-Chip Debug Interface**

- Internal address tracing support and On-Chip Emulation (OnCE)
- JTAG port

Allows for real-time software development, software download to on-chip or on-board RAM, software running and debug with full speed operation and breakpoint capability and the ability to modify all user-accessible registers, memory and peripherals

# **On-Chip Memory Configuration**

- 16K-48K x 24-bit Y-data RAM and 32K x 24-bit Y-data ROM
- 28K-36K x 24-bit X-data RAM and 32K x 24-bit X-data ROM
- 4K-44K x 24-bit program RAM
- 64K x 24-bit program and bootstrap ROM including a PROM patching mechanism
- · User configurable memory partitions
- · Provides user flexibility in memory partitioning

#### Phase-Locked Loop (PLL)

- PLL allows the processor to operate at a higher internal clock frequency derived from a low-frequency clock input
- Clock generator performs low-power division and internal clock generation
- Ability to oscillate at different frequencies reduces costs by eliminating the need to add additional oscillators to a system
- · Lower frequency clock input can reduce the overall electromagnetic interference (EMI) generated by a system

# **Enhanced Serial Audio Interface (ESAI)**

- Two dedicated Tx and 4 selectable Tx/Rx
- TDM network compatible with up to 32 words per frame
- Can be configured as a master or a slave
- · Supports many programmable protocols such as I2S, Sony, AC97, network
- Glueless connection to industry standard CODECS (I2S, Left Justified, Right Justified and AC97)
- Full-duplex serial port for serial communications with DSPs, MPUs and MCUs



## **Development Tools**

**DSPAUDIOEVMM1:** Generic motherboard that is used (along with a specific daughterboard) to demonstrate the abilities of the DSP5636x Family and provides a hardware tool to allow development of applications that use these devices. \$750\*

**DSPB56371DB1**: Daughterboard for DSPB56371 used with the DSPAUDIOEVMM1 \$250\*

**DSPD56371DB1**: Daughterboard for DSPD56371 used with the DSPAUDIOEVMM1 \$250\*

**SUITE56**: Robust tool suite for DSP56300 family of digital signal processors (DSPs) that includes an assembler, linker, simulator, debugger and several utilities.

Free\*\*

**SDI Debugger**: Symphony Debugger Interface Free\*\*

\*Prices listed are Manufacturer's Suggested Resale Price (MSRP)
\*\* Subject to license agreement and registration.

Package Options		
DSPB56371AF150	80 LQFP	-40°C to 85°C
DSPC56371AF150	80 LQFP	-40°C to 85°C
DSPD56371AF150	80 LQFP	-40°C to 85°C
DSPB56371AF180	80 LQFP	0°C to 70°C
DSPC56371AF180	80 LQFP	0°C to 70°C
DSPD56371AF180	80 LQFP	0°C to 70°C

Features	Benefits

#### Serial Host Interface (SHI)

- Serial peripheral interface protocol
- Inter-IC (I2C) protocol
- Multimaster capability in I2C mode
- 10-word receive FIFO
- Support for 8-, 16- and 24-bit word
- High-speed synchronous communication between multiple DSPs or between DSP and MCU or between DSP and serial peripherals
- Designed to provide a simple, efficient method of data exchange between devices

#### **Digital Audio Transmitter (DAX)**

- Digital audio interface that transmits data in SPDIF, AES/EBU, CP-340 and IEC958 formats
- Supports both master and slave mode
- Allows data transmission in commonly used digital audio formats to speed development time and reduce complexity

## **Enhanced Filter Co-Processor (EFCOP)**

- Fully programmable real/complex filter machine with 24-bit resolution
- · FIR filter options
- IIR filter options

 Allows simple implementation of filters without burdening the main CPU

#### **Triple Timer Module**

- Programmable mode of operation
- Timer mode, measurement mode, pulse with modulation mode, watchdog mode
- Common prescaler
- · Software polled or interrupt driven
- Three timers

• Flexible, programmable timer system

#### Watchdog Timer Module (WDT)

- Based on a 16-bit free-running down counter
- · Timeout period is user specified
- Used to recover from runaway code

#### **General Purpose Input Output (GPIO)**

- Most unused peripheral pins may be programmed as GPIO
- Up to 47 GPIO

Can be used for an array of functions in customers' systems

Learn More: For more information about Freescale audio processors,

please visit www.freescale.com/digitalaudio.

