FAIRCHILD
SEMICONDUCTOR™

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74VHC4051 • 74VHC4052 • 74VHC4053
8-Channel Analog Multiplexer • Dual 4-Channel Analog Multiplexer • Triple 2-Channel Analog Multiplexer

General Description

These multiplexers are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low “on” resistance and low “off” leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the “on” resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, ground, and V_{EE}. This enables the connection of 0–5V logic signals when V_{CC} = 5V and an analog input range of ±5V when V_{EE} = 5V. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

VHC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is “on”, and connects one of the eight inputs to the common output.

VHC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4-channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is “on”, connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.

VHC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be “on”.

Features

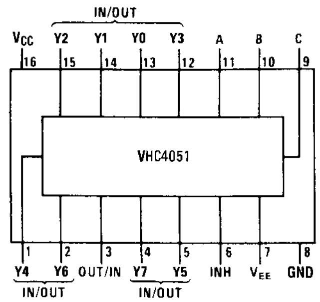
- Wide analog input voltage range: ±6V
- Low “on” resistance: 50 typ. (V_{CC}–V_{EE} = 4.5V)
  30 typ. (V_{CC}–V_{EE} = 9V)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum
- Matched switch characteristic
- Pin and function compatible with the 74HC4051/ 4052/ 4053

Ordering Code:

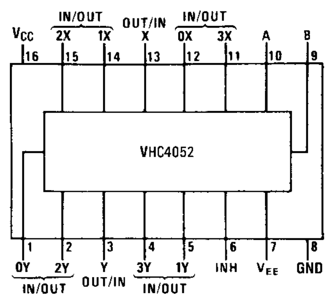
Order Number	Package Number	Package Description
74VHC4051M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
74VHC4051WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide
74VHC4051MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC4051N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
74VHC4052M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
74VHC4052WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide
74VHC4052MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC4052N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
74VHC4053M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
74VHC4053WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide
74VHC4053MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC4053N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

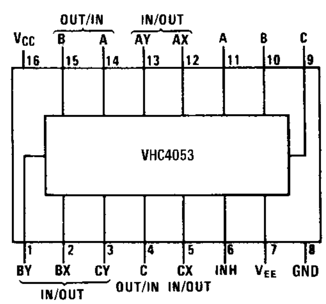
Connection Diagrams



Top View



Top View



Top View

Truth Tables

4051

Input				"ON"
INH	**C**	**B**	**A**	**Channel**
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

4052

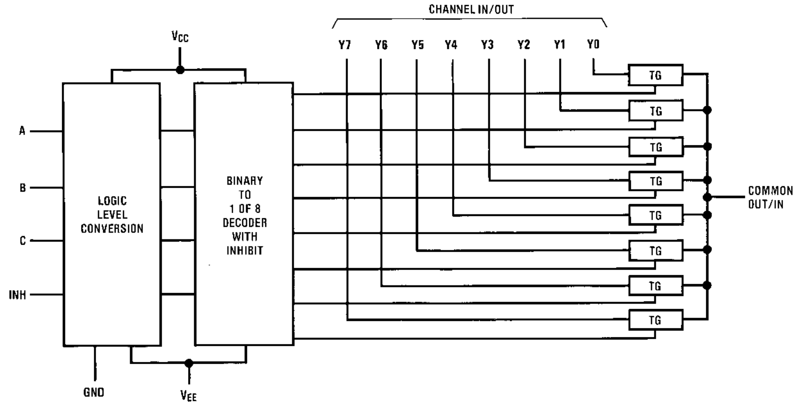
Inputs			"ON" Channels	
INH	**B**	**A**	**X**	**Y**
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

4053

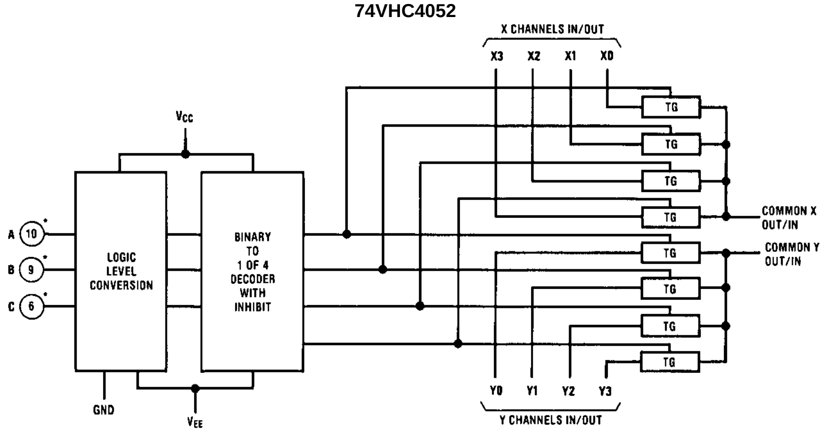
Input				"ON" Channels		
INH	**C**	**B**	**A**	**C**	**B**	**A**
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AX
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AX
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AX
L	H	H	H	CY	BY	AY

Logic Diagrams

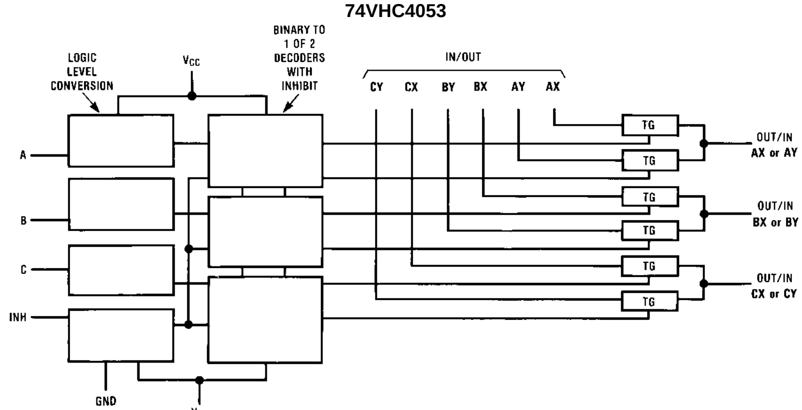
74VHC4051



74VHC4052



74VHC4053



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	–0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to –7.5V
Control Input Voltage (V_{IN})	–1.5 to V_{CC}+1.5V
Switch I/O Voltage (V_{IO})	V_{EE}–0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	–6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	–40	+85	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic “N” package: –12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}		$T_A = 25°C$	$T_A = -40$ to $85°C$	Units
						Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage				2.0V		1.5	1.5	V
					4.5V		3.15	3.15	V
					6.0V		4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage				2.0V		0.5	0.5	V
					4.5V		1.35	1.35	V
					6.0V		1.8	1.8	V
R_{ON}	Maximum “ON” Resistance (Note 5)		$V_{INH} = V_{IL}$, $I_S = 2.0$ mA	GND	4.5V	40	160	200	Ω
			$V_{IS} = V_{CC}$ to V_{EE}	–4.5V	4.5V	30	120	150	Ω
			(Figure 1)	–6.0V	6.0V	20	100	125	Ω
			$V_{INH} = V_{IL}$, $I_S = 2.0$ mA	GND	2.0V	100	230	280	Ω
			$V_{IS} = V_{CC}$ or V_{EE}	GND	4.5V	40	110	140	Ω
			(Figure 1)	–4.5V	4.5V	20	90	120	Ω
				–6.0V	6.0V	15	80	100	Ω
R_{ON}	Maximum “ON” Resistance Matching		$V_{INH} = V_{IL}$	GND	4.5V	10	20	25	Ω
			$V_{IS} = V_{CC}$ to GND	–4.5V	4.5V	5	10	15	Ω
				–6.0V	6.0V	5	10	12	Ω
I_N	Maximum Control Input Current		$V_{IN} = V_{CC}$ or GND $V_{CC} = 2 - 6V$				±.05	±0.5	μA
I_{CC}	Maximum Quiescent Supply Current		$V_{IN} = V_{CC}$ or GND	GND	6.0V		4	40	μA
			$I_{OUT} = 0$ μA	–6.0V	6.0V		8	80	μA
I_{IZ}	Maximum Switch “OFF” Leakage Current (Switch Input)		$V_{OS} = V_{CC}$ or V_{EE}	GND	6.0V		±60	±300	nA
			$V_{IS} = V_{EE}$ or V_{CC}	–6.0V	6.0V		±100	±500	nA
			$V_{INH} = V_{IH}$ (Figure 2)						
I_{IZ}	Maximum Switch “ON” Leakage Current	VHC4051	$V_{IS} = V_{CC}$ to V_{EE}	GND	6.0V		±0.1	±1.0	μA
			$V_{INH} = V_{IL}$	–6.0V	6.0V		±0.2	±2.0	μA
			(Figure 3)						
		VHC4052	$V_{IS} = V_{CC}$ to V_{EE}	GND	6.0V		±0.050	±0.5	μA
			$V_{INH} = V_{IL}$	–6.0V	6.0V		±0.1	±1.0	μA
			(Figure 3)						
		VHC4053	$V_{IS} = V_{CC}$ to V_{EE}	GND	6.0V		±0.05	±0.5	μA
			$V_{INH} = V_{IL}$	–6.0V	6.0V		±0.5	±0.5	μA
			(Figure 3)						
I_{IZ}	Maximum Switch “OFF” Leakage Current (Common Pin)	VHC4051	$V_{OS} = V_{CC}$ or V_{EE}	GND	6.0V		±0.1	±1.0	μA
			$V_{IS} = V_{EE}$ or V_{CC}	–6.0V	6.0V		±0.2	±2.0	μA
			$V_{INH} = V_{IH}$						
		VHC4052	$V_{OS} = V_{CC}$ or V_{EE}	GND	6.0V		±0.05	±0.5	μA
			$V_{IS} = V_{EE}$ or V_{CC}	–6.0V	6.0V		±0.1	±1.0	μA
			$V_{INH} = V_{IH}$						
		VHC4053	$V_{OS} = V_{CC}$ or V_{EE}	GND	6.0V		±0.05	±0.5	μA
			$V_{IS} = V_{EE}$ or V_{CC}	–6.0V	6.0V		±0.05	±0.5	μA
			$V_{INH} = V_{IH}$						

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

Note 6: Adjust 0 dB for f = 1 kHz (Null R1/R_{ON} Attenuation).

AC Electrical Characteristics

V_{CC} = 2.0V – 6.0V, V_{EE} = 0V – 6V, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions		V_{EE}	V_{CC}	T_A=25°C		T_A=–40 to 85°C	Units
						Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out			GND	3.3V	25	35	40	ns
				GND	4.5V	5	12	15	ns
				–4.5V	4.5V	4	8	12	ns
				–6.0V	6.0V	3	7	11	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ		GND	3.3V	92	200	250	ns
				GND	4.5V		69	87	ns
				–4.5V	4.5V	16	46	58	ns
				–6.0V	6.0V	15	41	51	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay			GND	3.3V	65	170	210	ns
				GND	4.5V	28	58	73	ns
				–4.5V	4.5V	18	37	46	ns
				–6.0V	6.0V	16	32	41	ns
f_{MAX}	Minimum Switch			GND	4.5V	30			MHz
	Frequency Response			–4.5V	4.5V	35			MHz
	20 log (V_I/V_O) = 3 dB								
	Control to Switch	R_L = 600Ω,	V_{IS} = 4 V_{PP}	0V	4.5V	1080			mV
	Feedthrough Noise	f = 1 MHz,	V_{IS} = 8 V_{PP}	–4.5V	4.5V	250			mV
		C_L = 50 pF							
	Crosstalk between	R_L = 600Ω,	V_{IS} = 4 V_{PP}	0V	4.5	–52			dB
	any Two Switches	f = 1 MHz	V_{IS} = 8 V_{PP}	–4.5V	4.5V	–50			dB
	Switch OFF Signal	R_L = 600Ω,	V_{IS} = 4 V_{PP}	0V	4.5V	–42			dB
	Feedthrough	f = 1 MHz,	V_{IS} = 8 V_{PP}	–4.5V	4.5V	–44			dB
	Isolation	V_{CTL} = V_{IL}							
THD	Sinewave Harmonic	R_L = 10 kΩ,	V_{IS} = 4 V_{PP}	0V	4.5V	0.013			%
	Distortion	C_L = 50 pF,	V_{IS} = 8 V_{PP}	–4.5V	4.5V	0.008			%
		f = 1 kHz							
C_{IN}	Maximum Control Input Capacitance					5	10	10	pF
C_{IN}	Maximum Switch	Input				15			pF
	Input Capacitance	4051 Common				90			
		4052 Common				45			
		4053 Common				30			
C_{IN}	Maximum Feedthrough Capacitance					5			pF

AC Test Circuits and Switching Time Waveforms

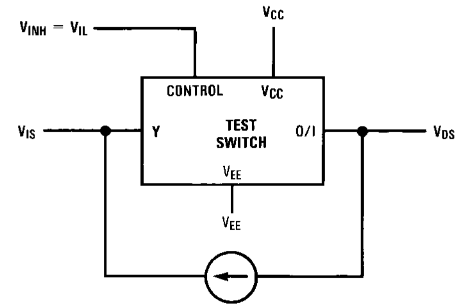


FIGURE 1. “ON” Resistance

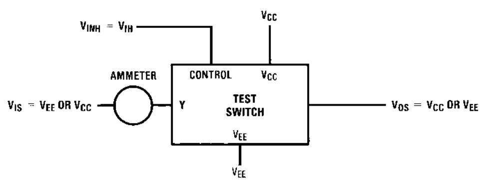


FIGURE 2. “OFF” Channel Leakage Current

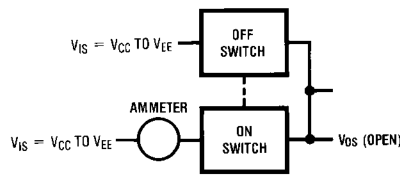


FIGURE 3. “ON” Channel Leakage Current

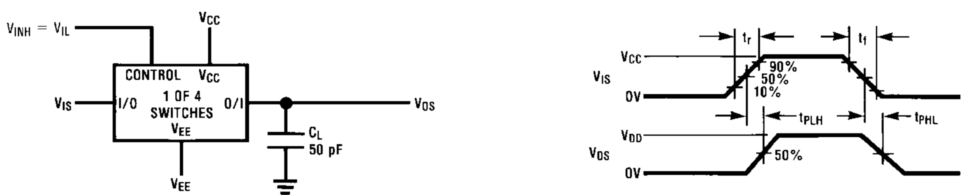


FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

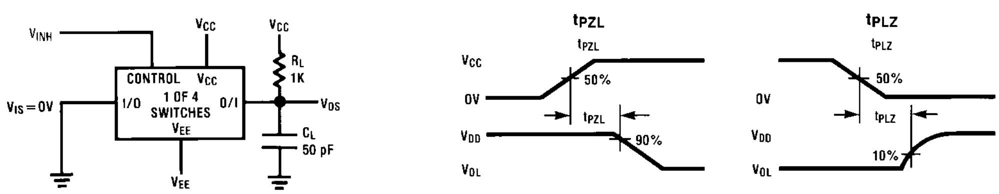


FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

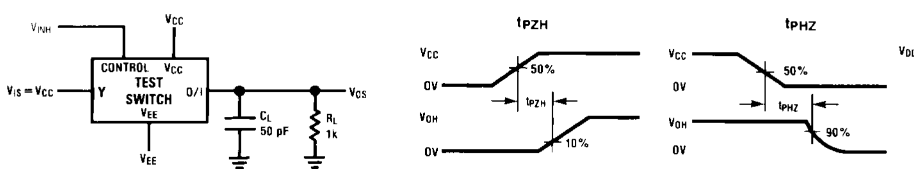


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay TIme Control to Signal Output

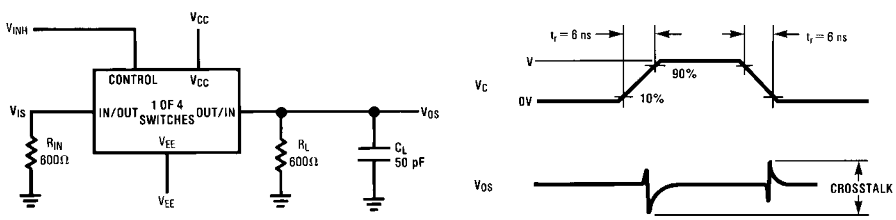


FIGURE 7. Crosstalk: Control Input to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

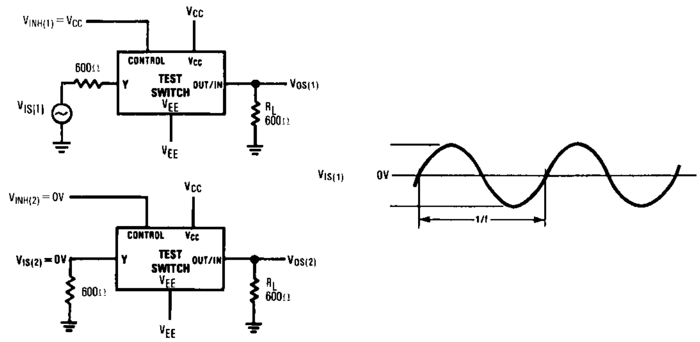
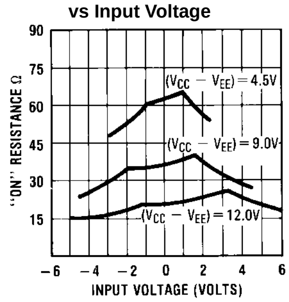


FIGURE 8. Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "On" Resistance vs Input Voltage

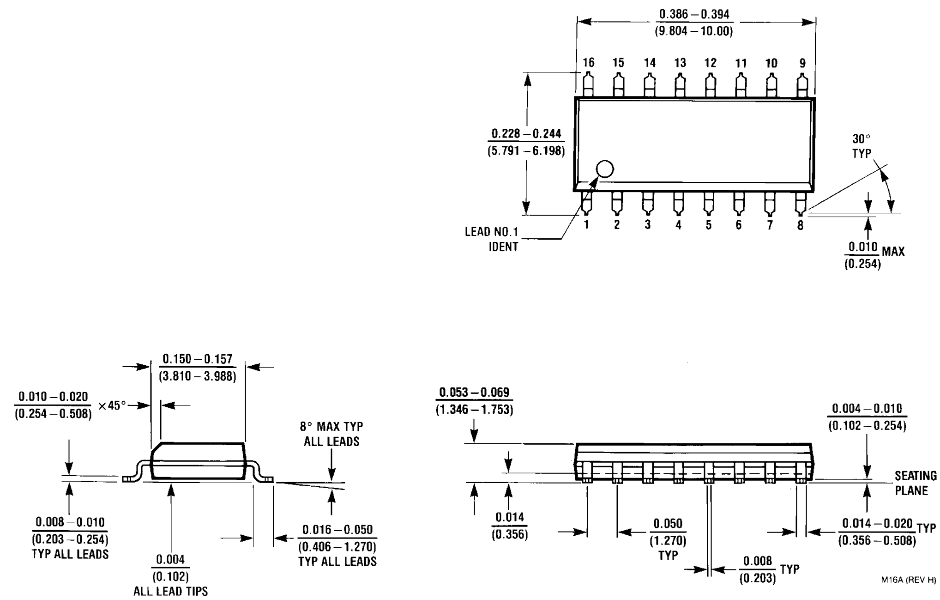


$V_{CC} = -V_{EE}$

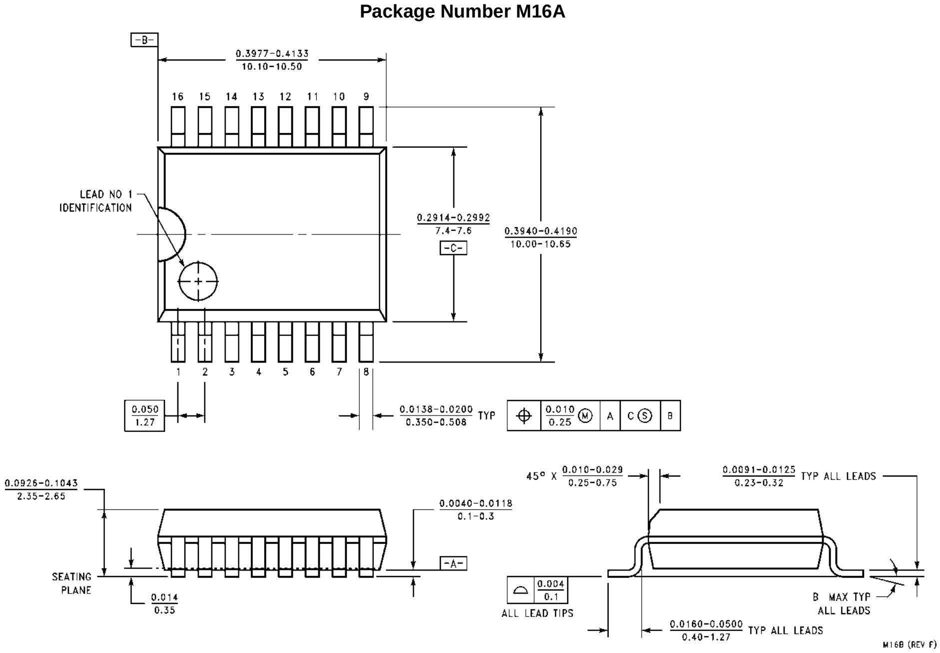
Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch pins, the voltage drop across the switch must not exceed 1.2V (calculated from the ON resistance).

Physical Dimensions inches (millimeters) unless otherwise noted

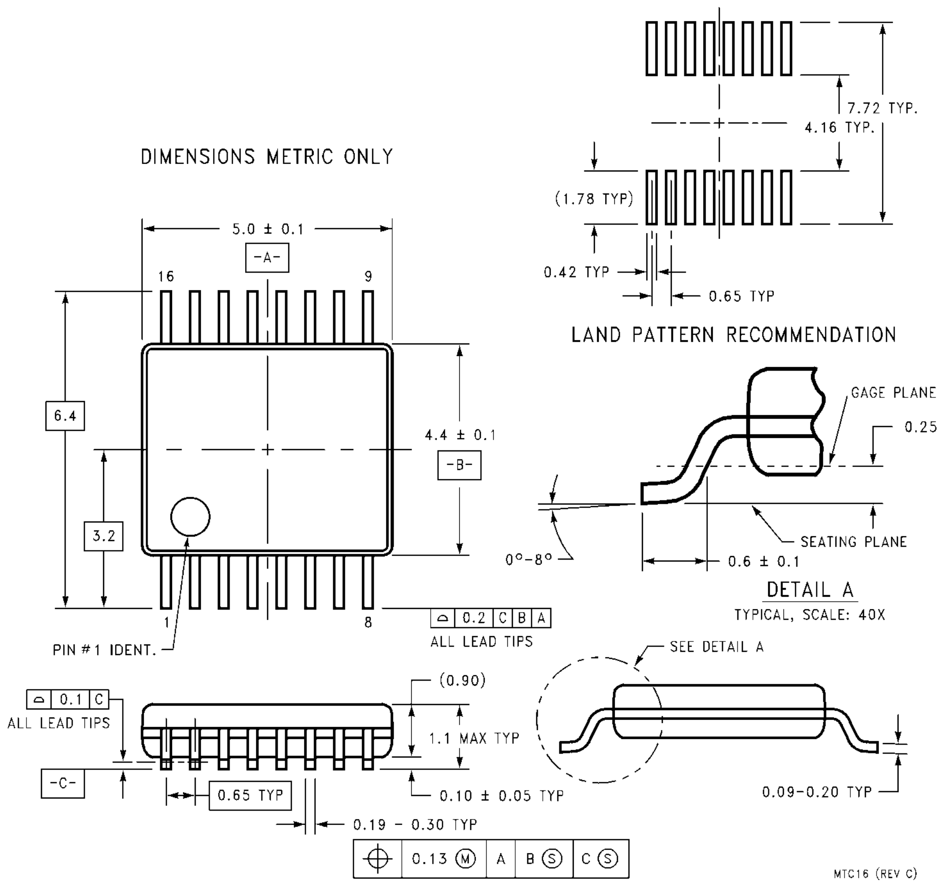


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A



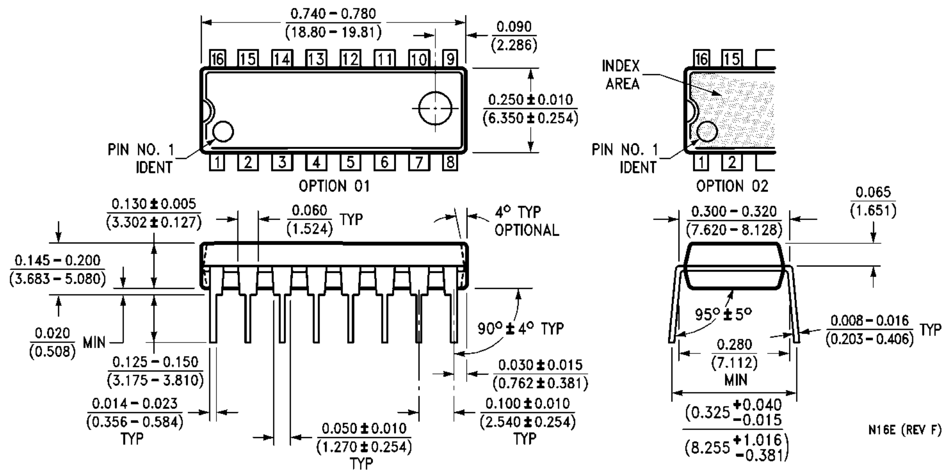
16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E