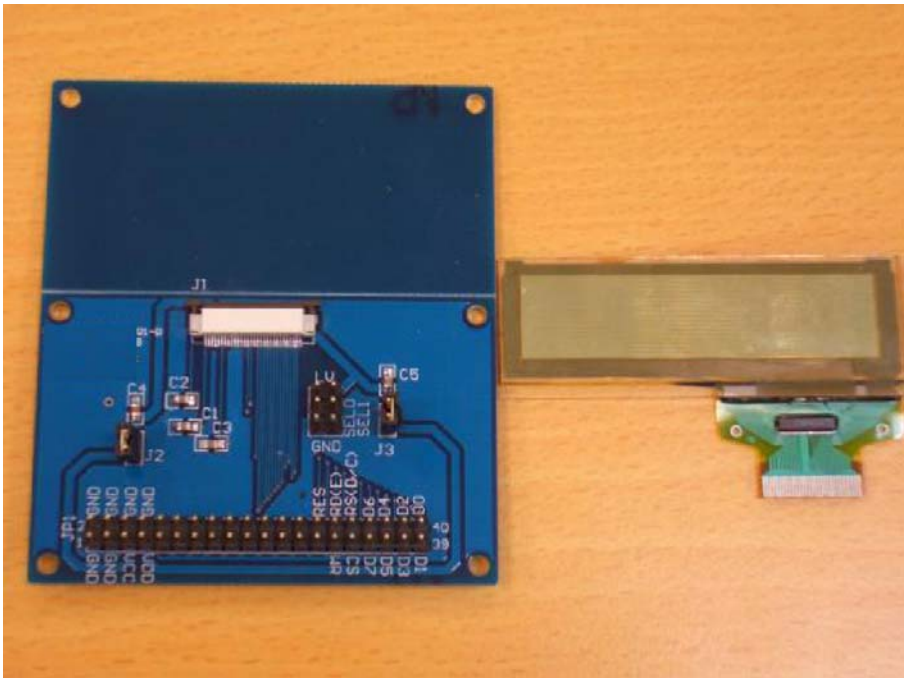
DENSITRON DISPLAYS

OLED DISPLAY MODULE

Application Notes

PRODUCT NUMBER	DD-12833BE-1A with EVK board



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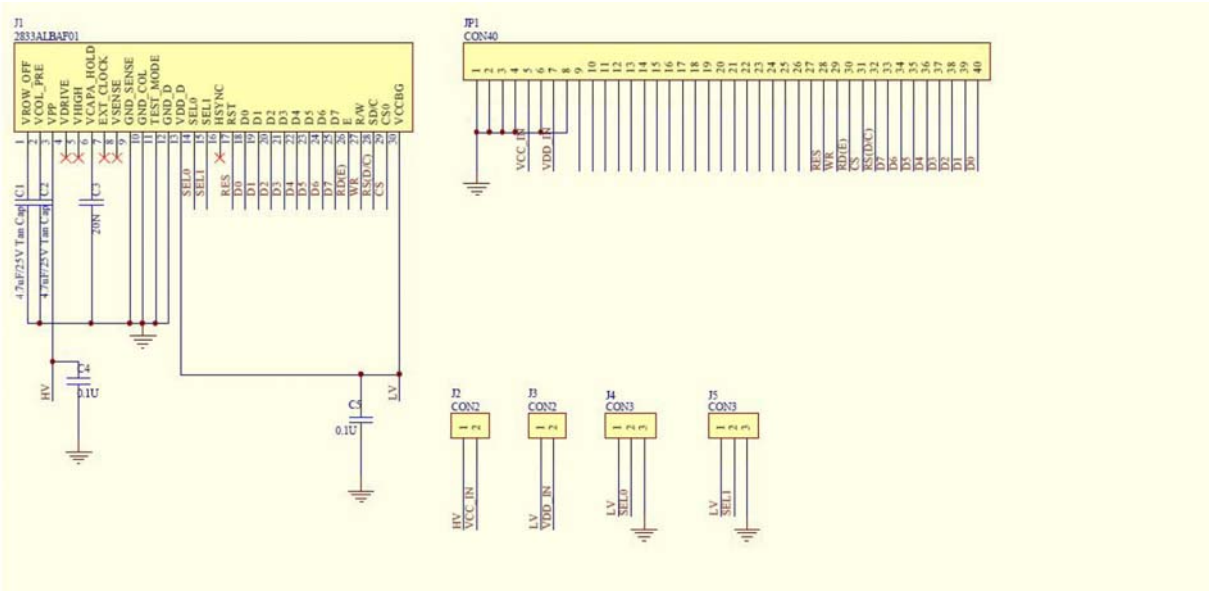
REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	16-Mar-06			First Issue	
B	13-OCT-06	4 6~11 17	1 3 6	Update Schematic；The EVK can use 80xx 、68xx 、SPI and I2C IF Initial code update	ECR_DE054

1 EVK Schematic



2 Symbol Definition

D0-D7：These pins are 8-bit bi-directional data bus to be connected to the MCU's data bus.

CS#: This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

SEL0, SEL1: These input pins are to configure MCU interface selection by appropriate logic settings as follows:

SEL1	SEL2	Interface
0	0	I2C(Standard or fast)
0	1	Serial
1	0	Parallel(68xx)
1	1	Parallel(80xx)

Table 1: MCU Interface Selection Setting

E/RD#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.
When connecting to an 8080-microprocessor, this pin receives the Read (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E (RD) must be connected to VSS.

R/W#：This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin is used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.
When 8080 interface mode is selected, this pin is the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W must be connected to VSS.

D/C#：This pin is Data/Command control pin. When the pin is pulled high, the data at D0-D7 is treated as display data. When the pin is pulled low, the data at D0-D7 is transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams at following pages and datasheet.

RES#：This pin is reset signal input. When the pin is low, initialization of the chip is executed.

HV：This is the most positive voltage supply pin of the chip.

LV：Power supply pin for logic operation of the driver.

GND：Power supply ground.

3 Timing characteristics

3.1 Mode (I²C Interface)

Write Mode

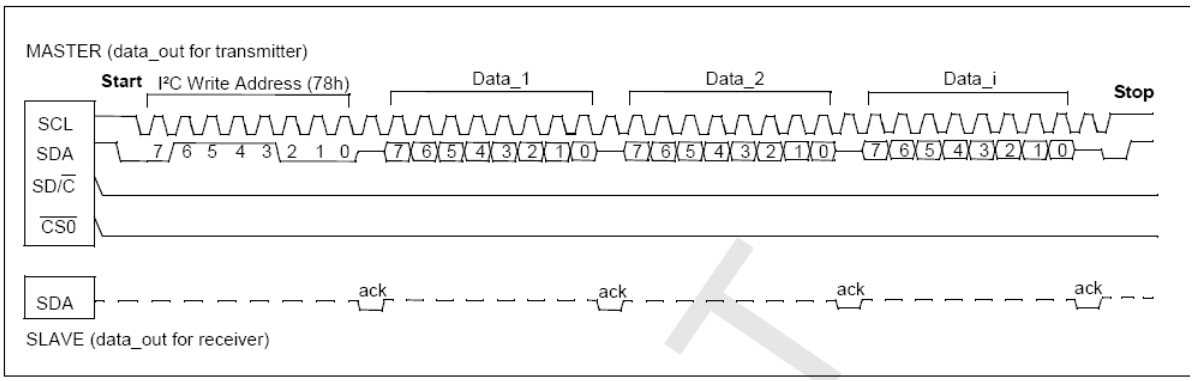


Figure 1：I²C Interface Timing Diagram for Register Write

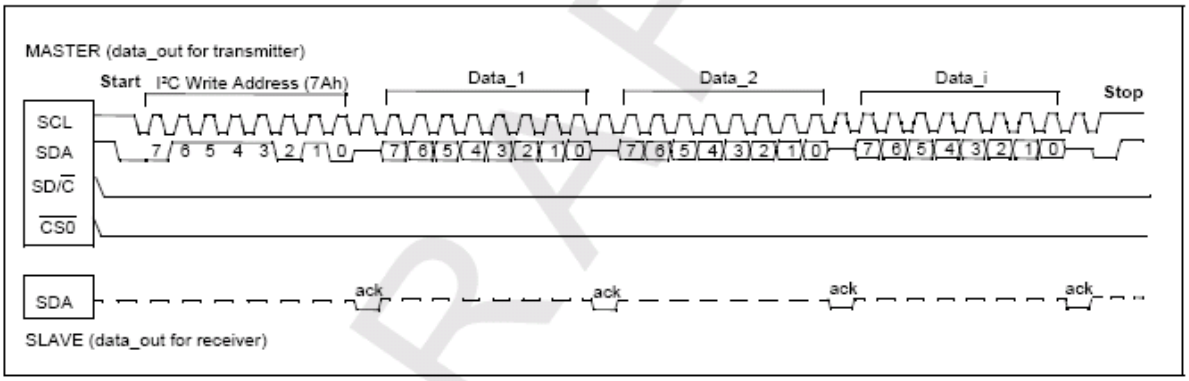


Figure 2：I²C Interface Timing Diagram for RAM Write

Item	Description	Min.	Typ.	Max.	Unit
Tscl_cycle		2.5			µs
Tscl_low / Tscl_high		100/100			ns
Tscl_rise / Tscl_fall				15/15	ns
Tdatas / Tdatah	Data setup & hold	100/100			ns
Tcs0s / Tcs0h	Chip Select setup & hold	120/120			ns

Table2: I²C Interface Write Timing

Read Mode

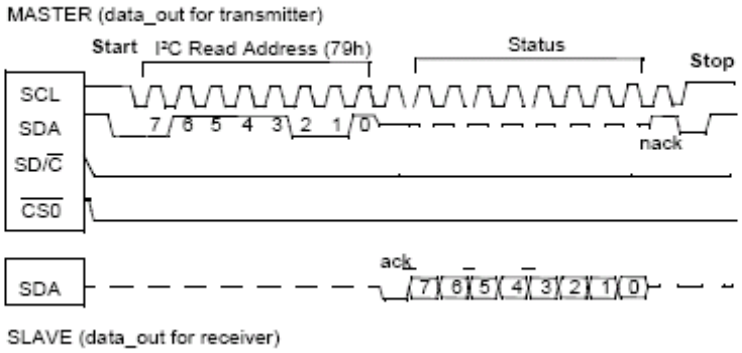


Figure 3：I²C Interface Read Timing Diagram (Register only)

Item	Description	Min.	Typ.	Max.	Unit
Tscl_cycle		2.5			μs
Tscl_low / Tscl_high		100/100			ns
Tscl_rise / Tscl_fall				15/15	ns
Tdatas / Tdatah	Data setup & hold	100/100			ns
Tcs0s / Tcs0h	Chip Select setup & hold	120/120			ns

Table3：I²C Interface Read Timing (Register only)

3.2 Serial Peripheral interface

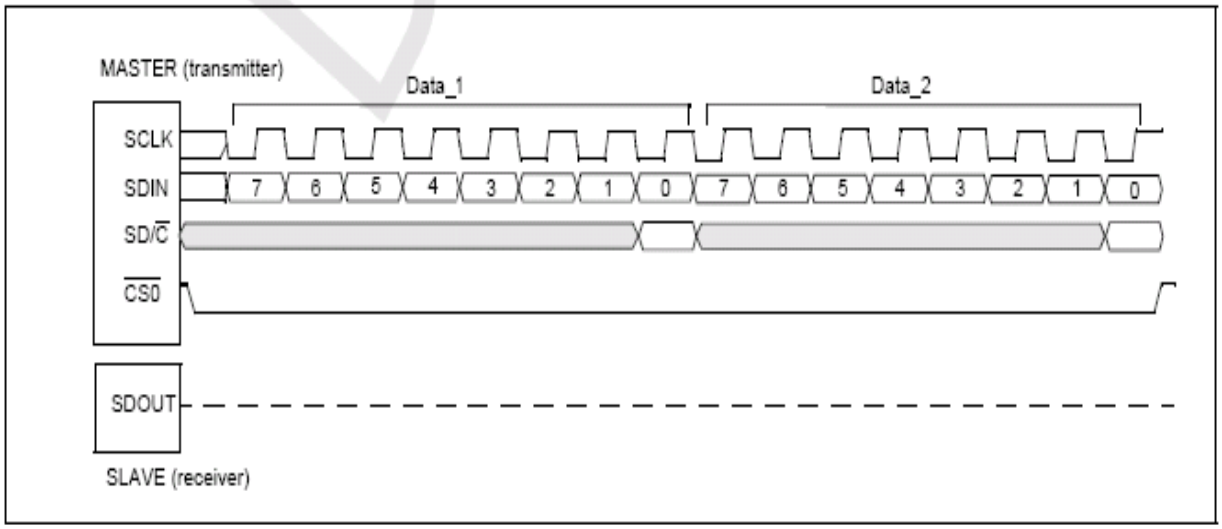


Figure 4：Serial Peripheral Interface Timing Diagram (Write Mode)

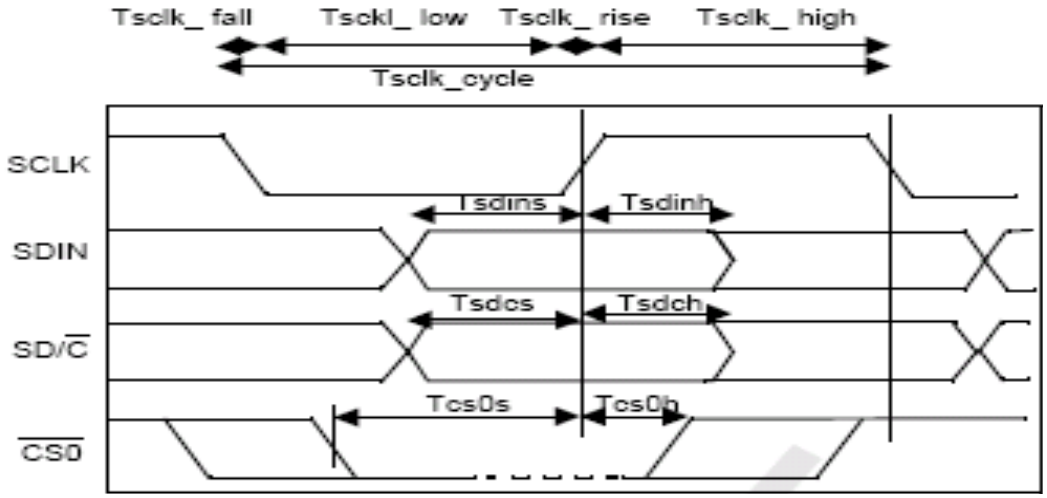


Figure 5：Serial Peripheral Interface Timing (Write Mode)

Item	Description	Min.	Typ.	Max.	Unit
Tsclk_cycle		250			ns
Tsclk_low / Tsclk_high		100/100			ns
Tsclk_rise / Tsclk_fall				15/15	ns
Tsdins / Tsdinh	SDIN setup & hold	100/100			ns
Tsdcs / Tsdch	SD/C setup & hold	150/150			ns
Tcs0s / Tcs0h	Chip Select setup & hold	150/150			ns

Table4：Serial Peripheral Interface Timing (Write Mode)

3.3 Mode 80-series (Parallel Interface)

Write Mode

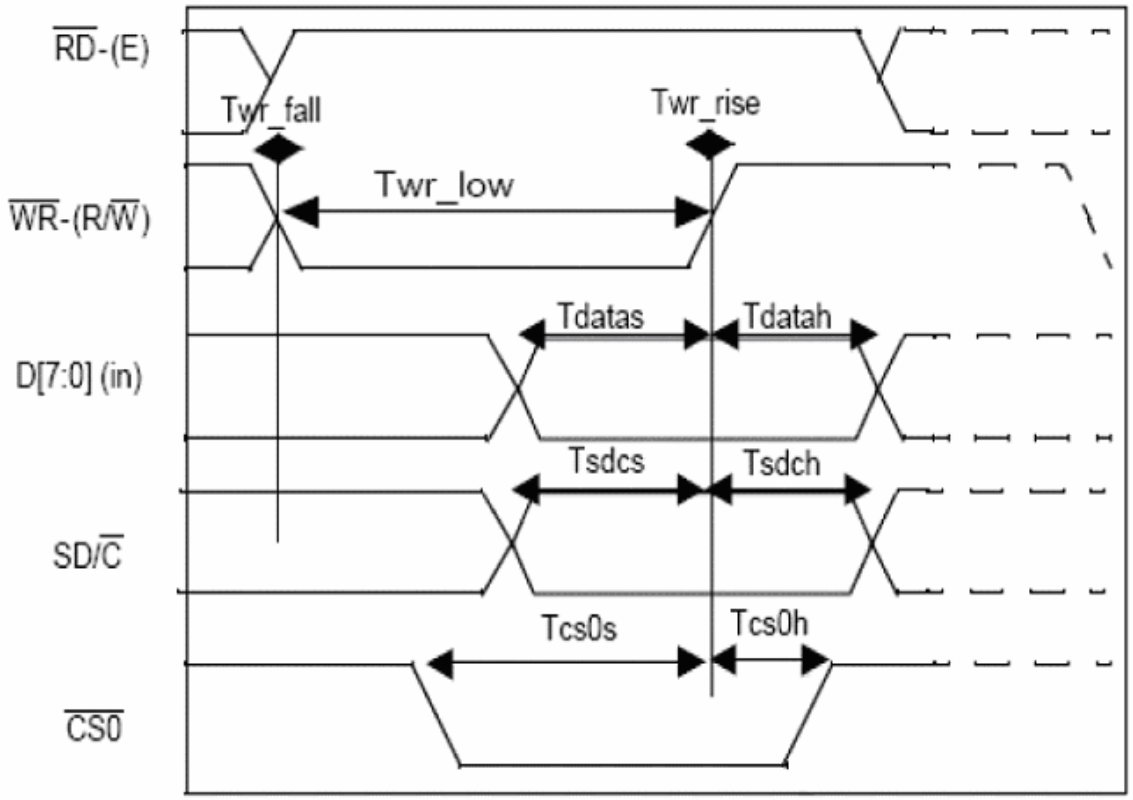


Figure 6: 80-series MPU 8-bit parallel interface Timing Diagram (write Mode)

Item	Description	Min.	Typ.	Max.	Unit
Twr_low		60			ns
Twr-rise / Twr_fall				15/15	ns
Tdatas / Tdatah	Data Address setup & hold	25/25			ns
Tsdcs / Tsdch	SD/C setup & hold	TBD	60/60		ns
Tcs0s / Tcs0h	Chip Select setup & hold	TBD	120/60		ns

Table 5: 80-series MPU 8-bit parallel interface Timing Diagram (write Mode)

Read Mode

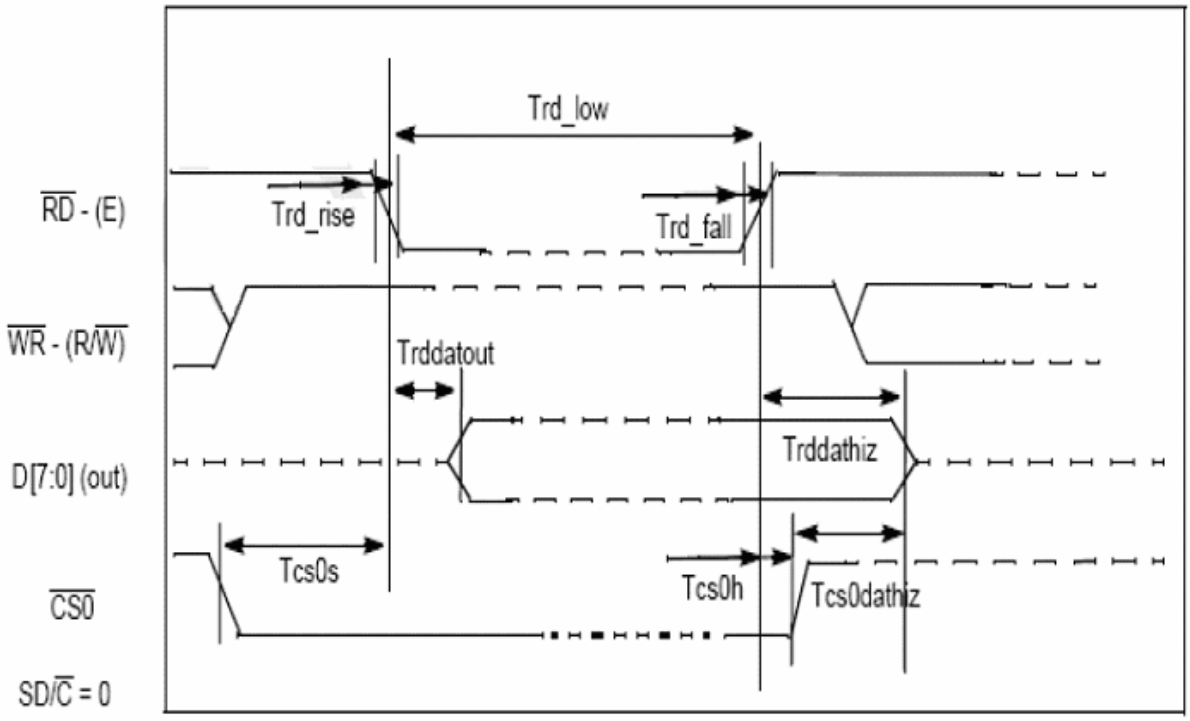


Figure 7: 80-series MPU 8-bit parallel interface Timing Diagram (Read Mode)

Item	Description	Min.	Typ.	Max.	Unit
Trd_low		120			ns
Trd_rise / Trd_fall				15/15	ns
Trddatout	Data out from RD falling edge (with CL = 100pF)		20	TBD	ns
Trddathiz	Data Hiz from RD rising edge (with CL = 100pF)			TBD	ns
Tcs0dathiz	Data Hiz from CS0 rising edge			TBD	
Tcs0s / Tcs0h	Chip Select setup & hold	120/60			ns

Table 6: 80-series MPU 8-bit parallel interface Timing Diagram (Read Mode)

3.4 Mode 68-series (Parallel Interface)

Write Mode

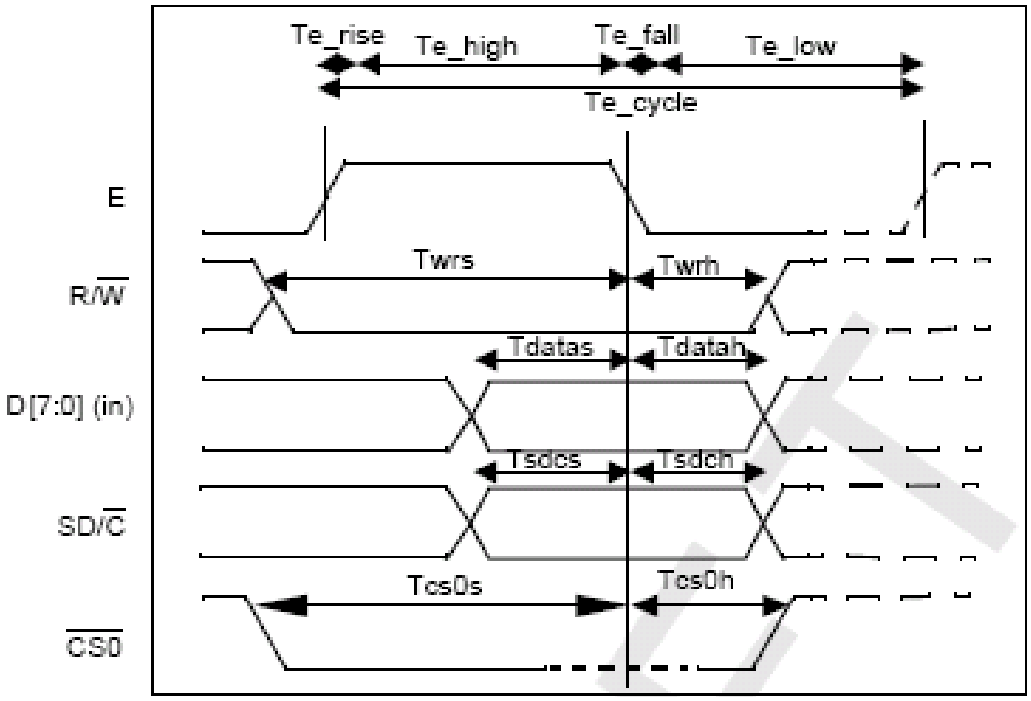


Figure 8：8-Bit Parallel 68XX interface Timing Diagram (Write Mode)

Item	Description	Min.	Typ.	Max.	Unit
Te_cycle		300			ns
Te_low / Te_high		60/60			ns
Te_rise / Te_fall				15/15	ns
Twrs / Twrh	Write Data setup & hold	TBD	50/50		ns
Tdatas / Tdatah	Data Address setup & hold	25/25			ns
Tsdcs / Tsdch	SD/C setup & hold	TBD	60/60		ns
Tcs0s / Tcs0h	Chip Select setup & hold	TBD	120/60		ns

Table7：8-bit Parallel 68XX Interface Timing (Write Mode)

Read Mode

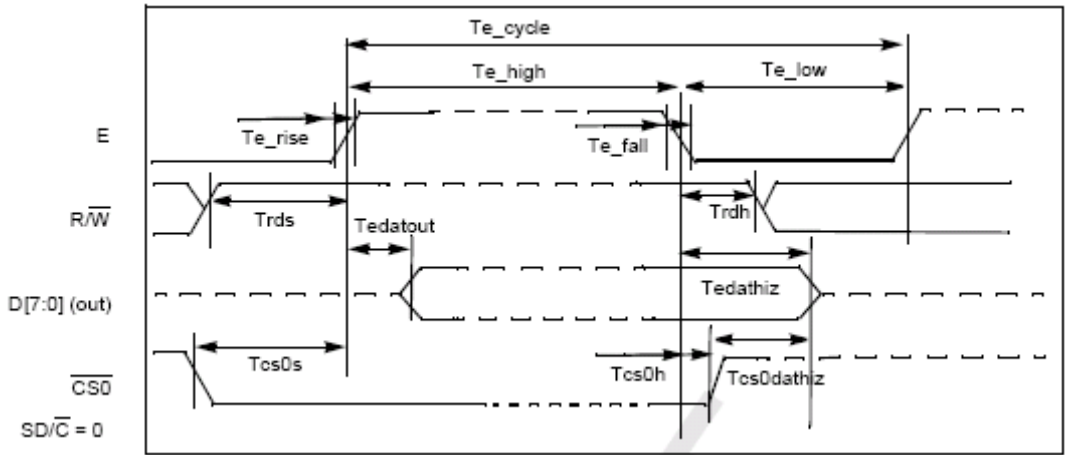


Figure 9: 8-Bit Parallel 68XX interface Timing Diagram for Register Read (only)

Item	Description	Min.	Typ.	Max.	Unit
Te_cycle		300			ns
Te_low / Te_high		120/60			ns
Te_rise / Te_fall				15/15	ns
Trds	READ setup to E rising edge (with CL = 100pF) A	TBD	50		ns
Trdh	READ hold from E falling edge (with CL = 100pF)	TBD	50		ns
Tedatout	Data out from E rising edge	-	20	TBD	ns
Tedathiz	Data Hiz from E falling edge	-		TBD	ns
Tcs0dathiz	Data Hiz from CS0 rising edge	-		TBD	ns
Tcs0s / Tcs0h	Chip Select setup & hold	120/60			ns

Table 15: 8-bit Parallel 68XX Interface Timing (Read Mode)

4 Connection Between OLED and EVK

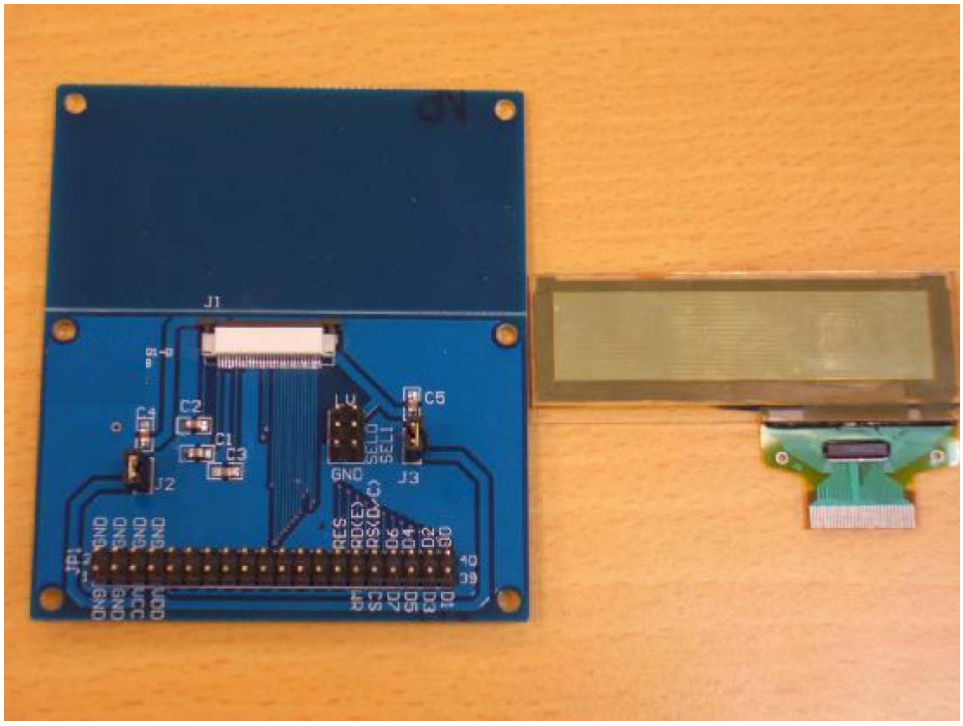


Figure 10: EVK PCB and DD-12833BE-1A Module

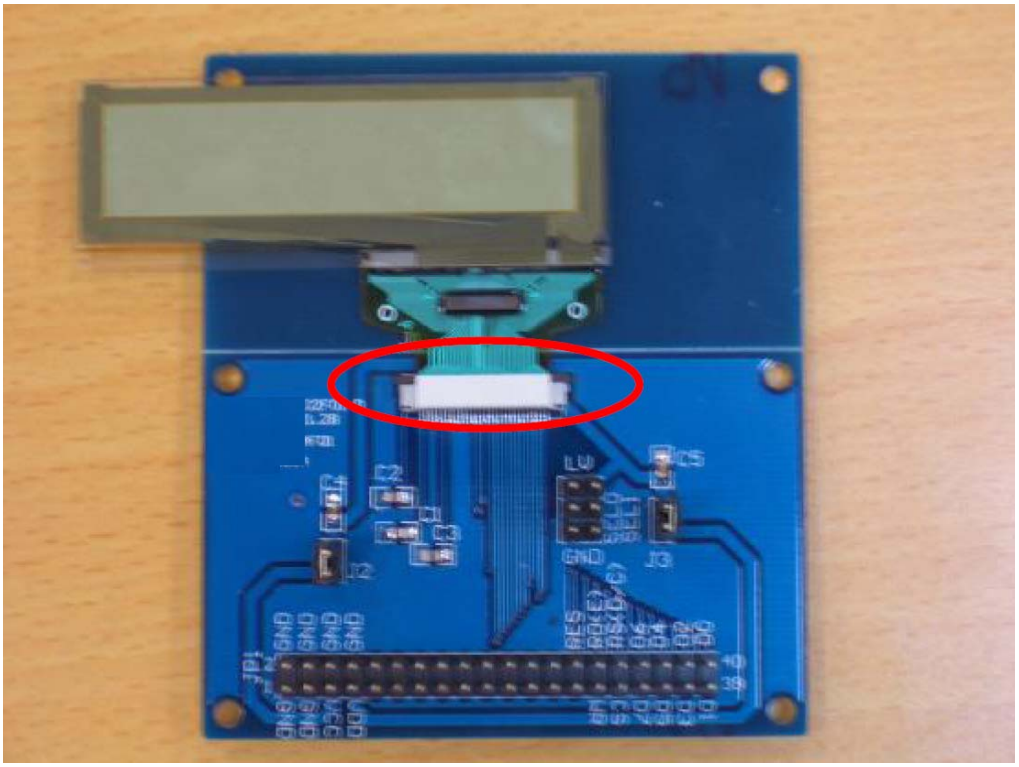


Figure 11: the DD-12833BE-1A and EVK assembled (Top view)

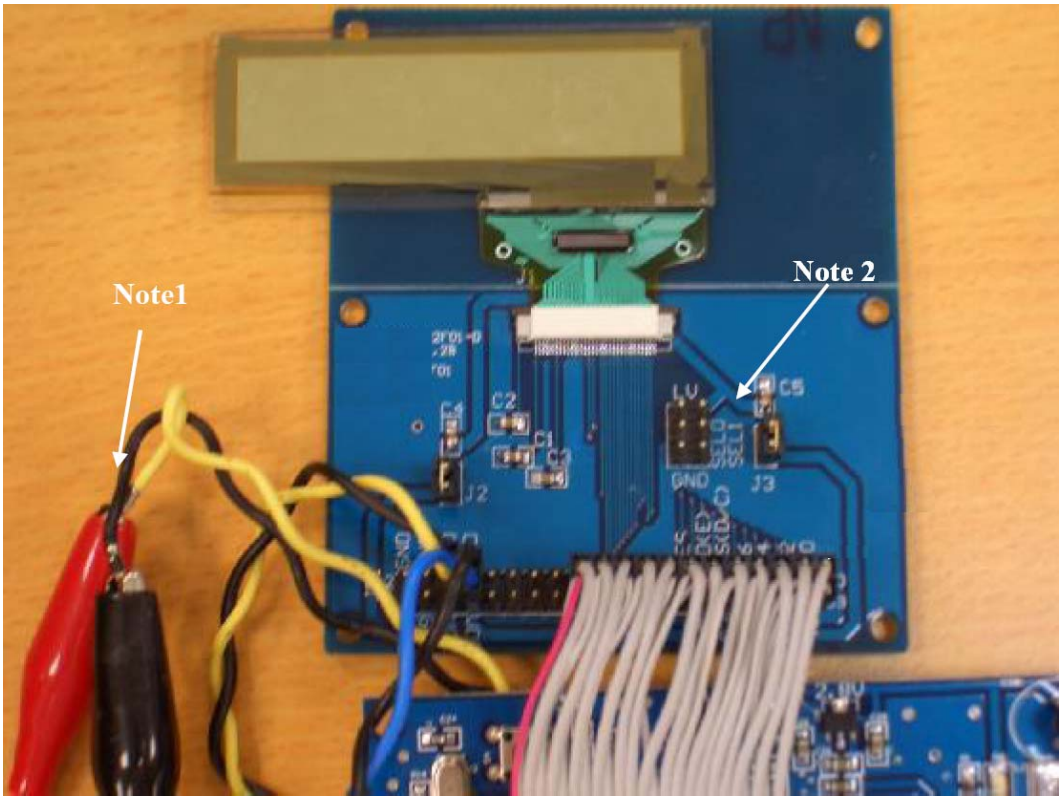


Figure 12: control MCU (not supplied) connected with EVK

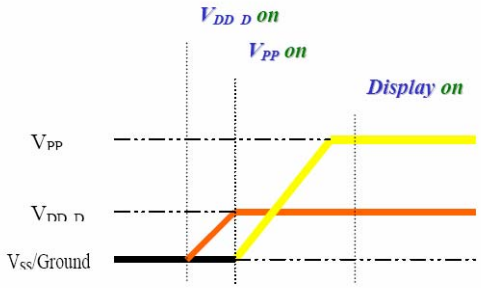
Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.
Note 2: Pins SEL0 and SEL1 is to select different types of interface

5 Power on Sequence:

To protect the OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

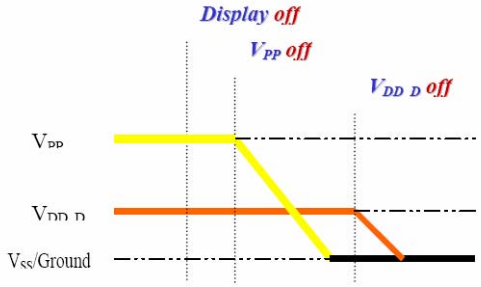
Power up Sequence:

1. Power up V_{DD_D}
2. Send Display off command
3. Driver IC initial Settings
4. Clear Screen
5. Power up V_{PP}
6. Delay 100ms (when V_{DD_D} is stable)
7. Send Display on command

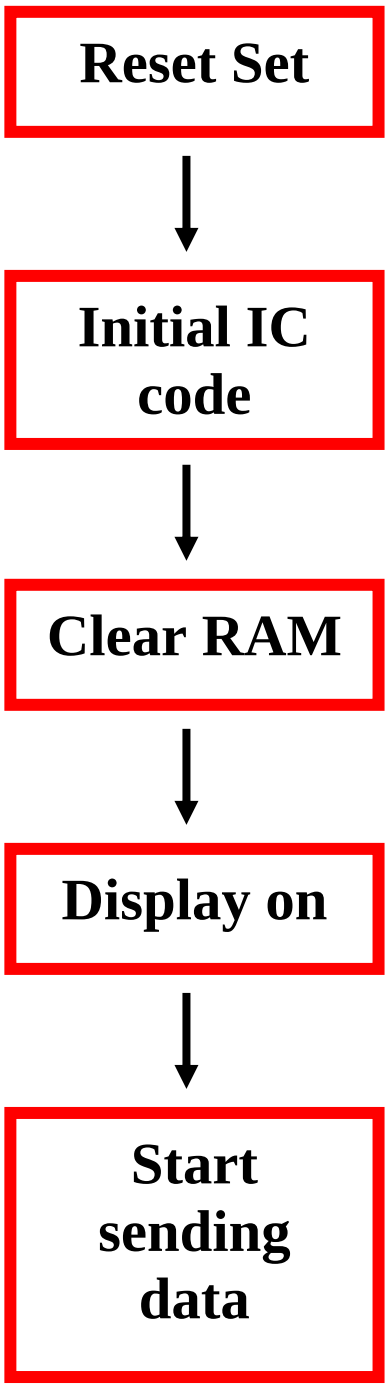


Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms (when V_{PP} reaches 0 and panel is completely discharges)
4. Power down V_{DD_D}



6 How to use the DD-12833BE-1A



RES#=0; Delay 10ms; RES#=1

Suggest all registers set again

6.1 Recommended Initial code

```
void Initial_ic(void)
{
        E_RD=1;
        D_C=0;
        R_W=0;
        CS=0;
        Reset_ST8102();
        write_c (0xCE);
        write_c (0xFF);
        write_c (0x2b); //'Set External MOS Enable
        write_c (0xC2); //'Set Horizontal Left Shift Limit
        write_c (0x0); //'no shift
        write_c (0xC0); //'Set Horizontal Right Shift Limit
        write_c (0x0); //'no shift
        write_c (0xC4); //'Set Horizontal Shift Selection
        write_c (0x0); //'no shift
        write_c (0x90); //'Set Screen Saver Horizontal Speed
        write_c (0xA0); //'Set Horizontal/Vertical Disable
        write_c (0xA2); //'Set Inverse Disable
        write_c (0x80);
        write_c (0x13); //'Set Clock Control,OSC Enable
        write_c (0xD6); //'Use Test Pattern Disable
        write_c (0xD8); //'Select Test Pattern
        write_c (0xB3); //'Set Mirror Effect Selection: MSB is bit0,Right to Left,Top to Bottom
        write_c (0xD0);
        write_c (0x0); //'Set Parallel,Selective discharge
        write_c (0x26); //'Set Pre-charge & Dis-charge
        write_c (0x2C); //'Set Internal Pre_charge Supply
        write_c (0xB8); //'Set RAM Access in ROW Mode Disable
        write_c (0xCC); //'Set Row Block Blanking
        write_c (0x1F); //'Set Duty=40
        write_c (0x28); //'Set In High Impedance state
        write_c (0x38); //'Row Mapping Selection
        write_c (0x2E); //'Set Internal row-off supply
        write_c (0xBA); //'Set utonatic Scan row blocks
        write_c (0x18); //'Set External supply on Vpp (No use DC-DC)
        write_c (0xC8); // 'Set Vertical Bottom Shift Limit is defult
        write_c (0xC6); // 'Set Vertical Top Shift Limit is defult
        write_c (0xA6); // 'Vpp Clamp Value=8
        write_c (0x14);
        write_c (0xCA); // 'Set Vertical Shift Selection is defult
        write_c (0x0);
        write_c (0x98); // Set Screen Saver Vertical Speed is defult
        write_c (0x0);
        write_c (0xAF); // 'Display On
}
void write_c(unsigned char out_command)
{
        R_W=0;
        CS=0;
        D_bus=out_command;
        D_C=0;
        R_W=1;
        CS=1;
        D_C=1;
}
```

```
void write_d(unsigned char out_data)
{
        R_W=0;
        CS=0;
        D_bus=out_data;
        D_C=1;
        R_W=1;
        CS=1;
        D_C=0;
}
void Reset_ST8102(void)
{
        RES=0;
        Delay_1ms(100);
        RES=1;
}
void Delay_1ms(int Cycle)
{
        unsigned int i,k;
        for (i=0 ;i<Cycle;i++)
        for(k=0;k<0x5f;k++);
}
```

Write_c= Write Command