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Jameco Part Number 976118

MC74HC273A

Octal D Flip-Flop with Common Clock and Reset

High-Performance Silicon-Gate CMOS

The MC74HC273A is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of eight D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active low.

Features

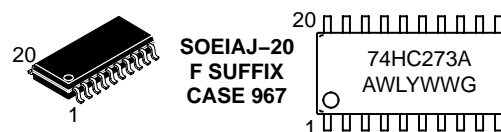
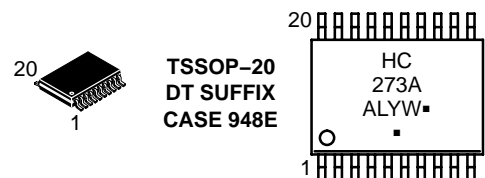
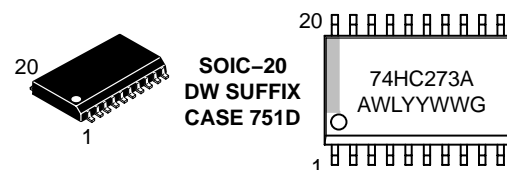
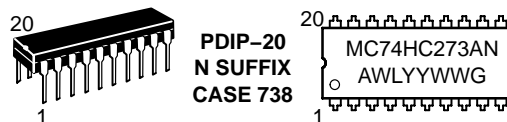
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates
- Pb-Free Packages are Available*



ON Semiconductor®

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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package
▪ = Pb-Free Package
(Note: Microdot may be in either location)

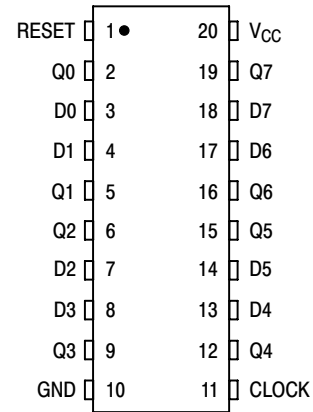
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

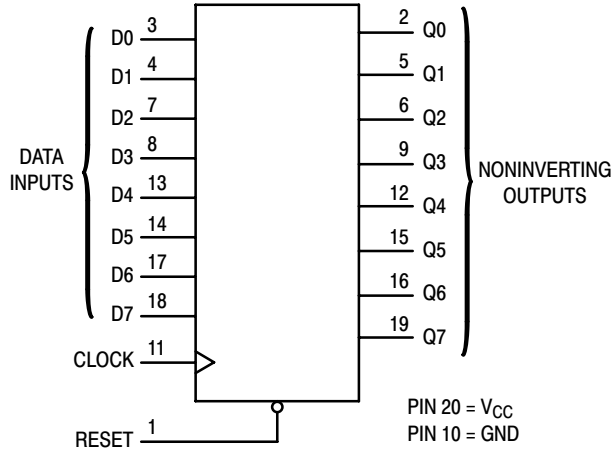
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC273A

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

| Inputs | | | Output |
|--------|-------|---|-----------|
| Reset | Clock | D | Q |
| L | X | X | L |
| H | | H | H |
| H | | L | L |
| H | L | X | No Change |
| H | | X | No Change |

| Design Criteria | Value | Units |
|---------------------------------|-------|---------|
| Internal Gate Count* | 66 | ea |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | μ W |
| Speed Power Product | .0075 | pJ |

*Equivalent to a two-input NAND gate.

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|---------------------------|------------------|
| MC74HC273AN | PDIP-20 | 18 Units / Rail |
| MC74HC273ANG | PDIP-20 (Pb-Free) | 18 Units / Rail |
| MC74HC273ADW | SOIC-20 WIDE | 38 Units / Rail |
| MC74HC273ADWG | SOIC-20 WIDE (Pb-Free) | 38 Units / Rail |
| MC74HC273ADWR2 | SOIC-20 WIDE | 1000 Tape & Reel |
| MC74HC273ADWR2G | SOIC-20 WIDE (Pb-Free) | 1000 Tape & Reel |
| MC74HC273ADT | TSSOP-20* | 75 Units / Rail |
| MC74HC273ADTG | TSSOP-20* | 75 Units / Rail |
| MC74HC273ADTR2 | TSSOP-20* | 2500 Tape & Reel |
| MC74HC273ADTR2G | TSSOP-20* | 2500 Tape & Reel |
| MC74HC273AF | SOEIAJ-20 | 40 Units / Rail |
| MC74HC273AFG | SOEIAJ-20 (Pb-Free) | 40 Units / Rail |
| MC74HC273AFEL | SOEIAJ-20 | 2000 Tape & Reel |
| MC74HC273AFELG | SOEIAJ-20 (Pb-Free) | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package† | 750 500 450 | mW |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|--|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | - 55 | + 125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figure 1) | $V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ | 0 1000 500 400 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | | | Unit |
|----------|-----------------------------------|---|-------------------|---|-------------------------|--------------------------|------|
| | | | | - 55 to 25°C | $\leq 85^\circ\text{C}$ | $\leq 125^\circ\text{C}$ | |
| V_{IH} | Minimum High-Level Input Voltage | $V_{out} = V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{out} = 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | | $V_{in} = V_{IH}$ | $ I_{out} \leq 2.4 \text{ mA}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$ | 3.0 4.5 6.0 | 2.48 3.98 5.48 | |
| V_{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | | $V_{in} = V_{IL}$ | $ I_{out} \leq 2.4 \text{ mA}$ $ I_{out} \leq 6.0 \text{ mA}$ $ I_{out} \leq 7.8 \text{ mA}$ | 3.0 4.5 6.0 | 0.26 0.26 0.26 | |

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| I _{in} | Maximum Input Leakage Current | V _{in} = V _{CC} or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 6.0 | ± 0.5 | ± 5.0 | ± 10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND I _{out} = 0 μA | 6.0 | 4.0 | 40 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|--------------------------------------|---|----------------------|------------------|--------|---------|------|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| f _{max} | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 2.0 | 6.0 | 5.0 | 4.0 | MHz |
| | | 3.0 | 15 | 10 | 8.0 | |
| | | 4.5 | 30 | 24 | 20 | |
| | | 6.0 | 35 | 28 | 24 | |
| t _{PLH} t _{PHL} | Maximum Propagation Delay, Clock to Q (Figures 1 and 4) | 2.0 | 145 | 180 | 220 | ns |
| | | 3.0 | 90 | 120 | 140 | |
| | | 4.5 | 29 | 36 | 44 | |
| | | 6.0 | 25 | 31 | 38 | |
| t _{PHL} | Maximum Propagation Delay, Reset to Q (Figures 2 and 4) | 2.0 | 145 | 180 | 220 | ns |
| | | 3.0 | 90 | 120 | 140 | |
| | | 4.5 | 29 | 36 | 44 | |
| | | 6.0 | 25 | 31 | 38 | |
| t _{TLH} t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0 | 75 | 95 | 110 | ns |
| | | 3.0 | 27 | 32 | 36 | |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| C _{in} | Maximum Input Capacitance | | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V _{CC} = 5.0 V | pF |
|-----------------|---|---|----|
| | | 48 | |

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

| Symbol | Parameter | Figure | V _{CC} Volts | Guaranteed Limit | | | | | | Unit |
|---------------------------------|--|--------|--------------------------|------------------|------|--------|------|---------|-----|------|
| | | | | - 55 to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| t _{su} | Minimum Setup Time, Data to Clock | 3 | 2.0 | 60 | | 75 | | 90 | ns | |
| | | | 3.0 | 23 | | 27 | | 32 | | |
| | | | 4.5 | 12 | | 15 | | 18 | | |
| | | | 6.0 | 10 | | 13 | | 15 | | |
| t _h | Minimum Hold Time, Clock to Data | 3 | 2.0 | 3.0 | | 3.0 | | 3.0 | ns | |
| | | | 3.0 | 3.0 | | 3.0 | | 3.0 | | |
| | | | 4.5 | 3.0 | | 3.0 | | 3.0 | | |
| | | | 6.0 | 3.0 | | 3.0 | | 3.0 | | |
| t _{rec} | Minimum Recovery Time, Reset Inactive to Clock | 2 | 2.0 | 5.0 | | 5.0 | | 5.0 | ns | |
| | | | 3.0 | 5.0 | | 5.0 | | 5.0 | | |
| | | | 4.5 | 5.0 | | 5.0 | | 5.0 | | |
| | | | 6.0 | 5.0 | | 5.0 | | 5.0 | | |
| t _w | Minimum Pulse Width, Clock | 1 | 2.0 | 60 | | 75 | | 90 | ns | |
| | | | 3.0 | 23 | | 27 | | 32 | | |
| | | | 4.5 | 12 | | 15 | | 18 | | |
| | | | 6.0 | 10 | | 13 | | 15 | | |
| t _w | Minimum Pulse Width, Reset | 2 | 2.0 | 60 | | 75 | | 90 | ns | |
| | | | 3.0 | 23 | | 27 | | 32 | | |
| | | | 4.5 | 12 | | 15 | | 18 | | |
| | | | 6.0 | 10 | | 13 | | 15 | | |
| t _r , t _f | Maximum Input Rise and Fall Times | 1 | 2.0 | | 1000 | | 1000 | 1000 | ns | |
| | | | 3.0 | | 800 | | 800 | 800 | | |
| | | | 4.5 | | 500 | | 500 | 500 | | |
| | | | 6.0 | | 400 | | 400 | 400 | | |

MC74HC273A

SWITCHING WAVEFORMS

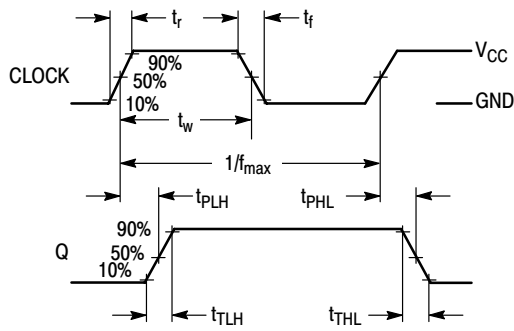


Figure 1.

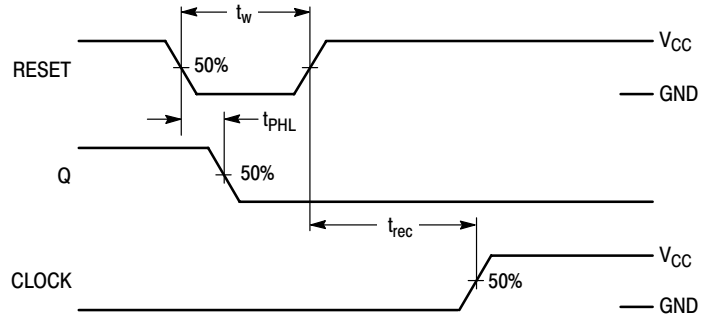


Figure 2.

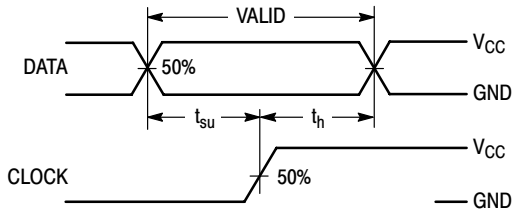
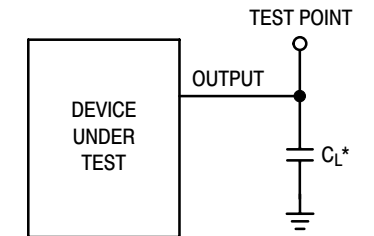


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

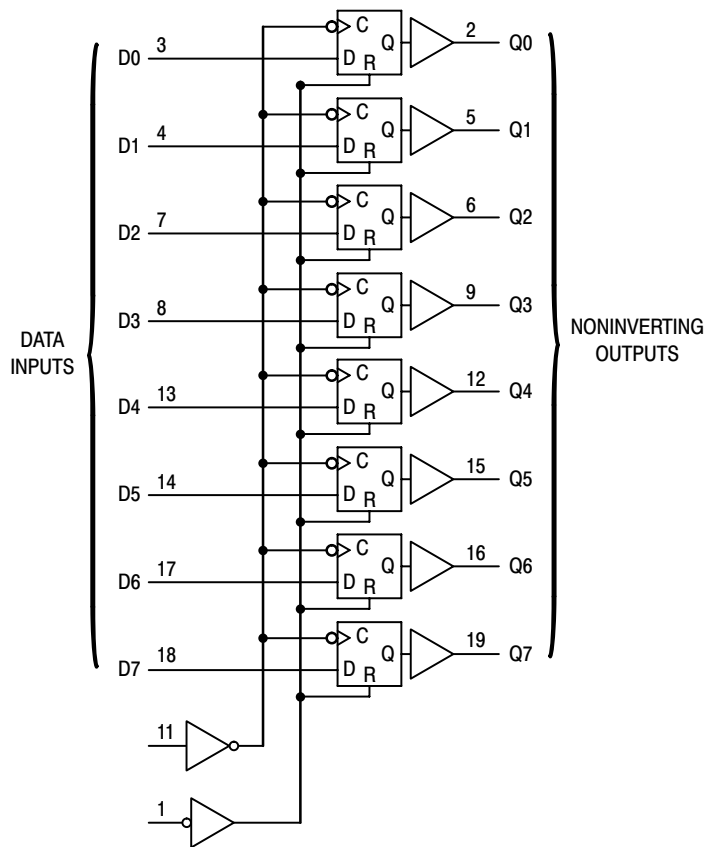
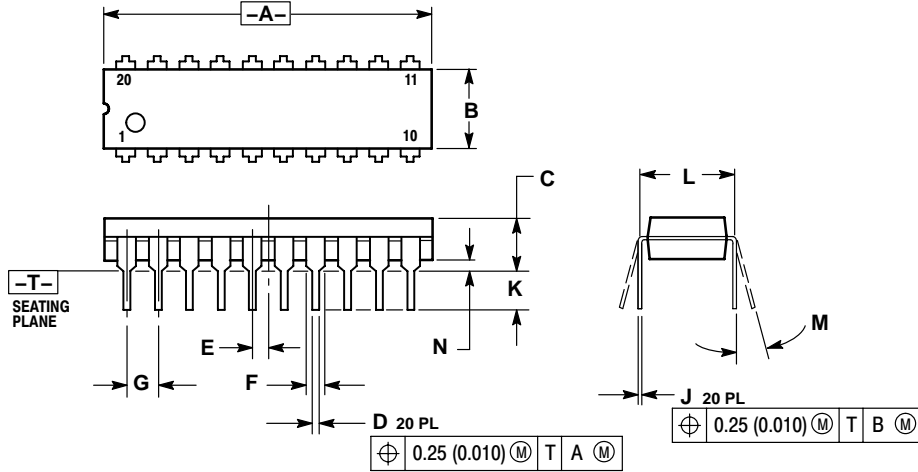


Figure 5. Expanded Logic Diagram

MC74HC273A

PACKAGE DIMENSIONS

PDIP-20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E

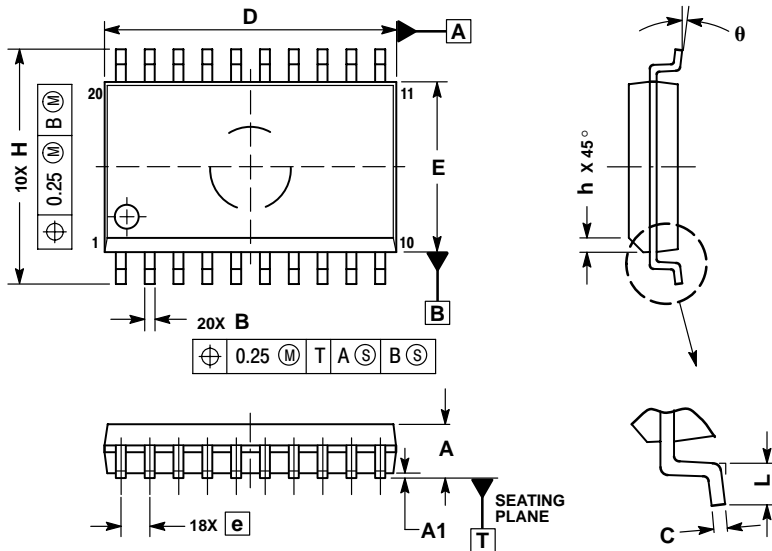


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

SOIC-20
DW SUFFIX
CASE 751D-05
ISSUE G



NOTES:

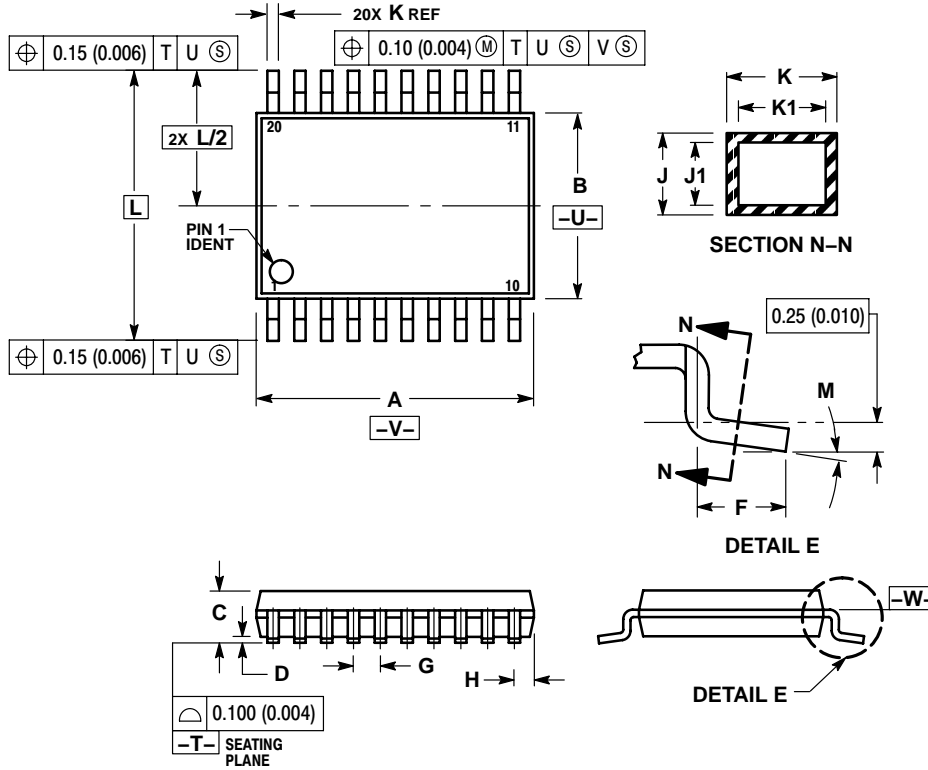
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-------|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| theta | 0° | 7° |

MC74HC273A

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE B



NOTES:

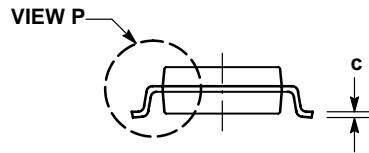
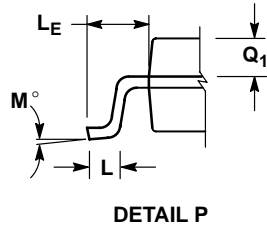
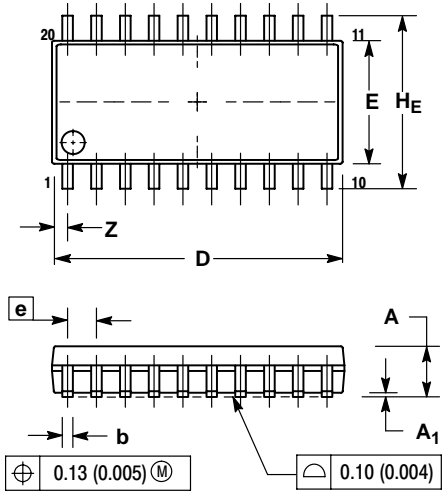
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74HC273A

PACKAGE DIMENSIONS

SOEIAJ-20
F SUFFIX
CASE 967-01
ISSUE O




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.81 | --- | 0.032 |

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