

## ESD PROTECTED, HIGH-SPEED USB 2.0 (480-Mbps) 1:2 MULTIPLEXER/DEMULTIPLEXER SWITCH WITH SINGLE ENABLE

Check for Samples: [TS3USB30E](#)

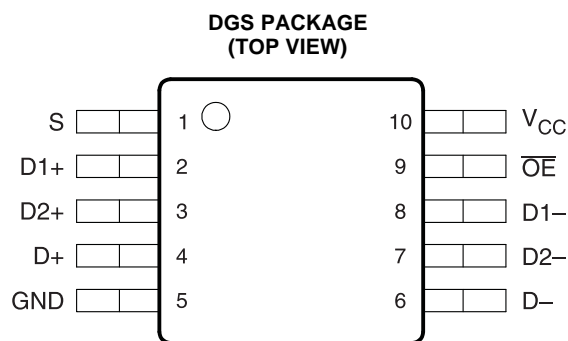
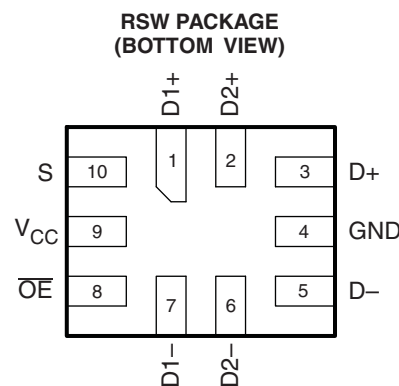
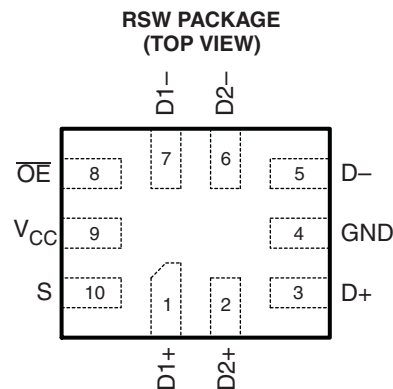
### FEATURES

- $V_{CC}$  Operation at 3 V to 4.3 V
- 1.8-V Compatible Control-Pin Inputs
- $I_{OFF}$  Supports Partial Power-Down-Mode Operation
  - D+/D– Pins Tolerate up to 5.25V
- $r_{ON} = 10 \Omega$  Max
- $\Delta r_{ON} = 0.35 \Omega$  Typ
- $C_{io(ON)} = 7.5$  pF Typ
- Low Power Consumption (1  $\mu$ A Max)
- –3 dB Bandwidth = 900 MHz Typ
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II <sup>(1)</sup>
- ESD Performance Tested Per JESD 22
  - 8000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance I/O Port to GND <sup>(2)</sup>
  - 15000-V Human-Body Model
- Packaged in 10-pin TQFN (1.4 mm × 1.8 mm)

### APPLICATIONS

- Routes Signals for USB 1.0, 1.1, and 2.0

- (1) Except  $\overline{OE}$  and S inputs  
 (2) High-voltage HBM is performed in addition to the standard HBM testing (A114-B, Class II) and applies to I/O ports tested with respect to GND only.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## DESCRIPTION/ORDERING INFORMATION

The TS3USB30E is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB30E integrates ESD protection cells on all pins, is available in a tiny  $\mu$ QFN package (1.8 mm x 1.4 mm), a DGS package, and is characterized over the free air temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1) (2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	UQFN – RSW	Tape and reel	TS3USB30ERSWR	LY_, L6_
	VSSOP – DGS	Tape and reel	TS3USB30EDGSR	L6R

- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).  
 (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).  
 (3) RSW: The actual top-side marking has one additional character that designates the assembly/test site.

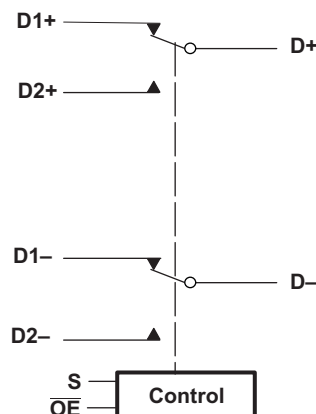
## PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{\text{OE}}$	Bus-switch enable
S	Select input
D+, D-, Dn+, Dn-	Data ports

## TRUTH TABLE

S	$\overline{\text{OE}}$	FUNCTION
X	H	Disconnect
L	L	D = D1
H	L	D = D2

## BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS<sup>(1) (2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_{IN}$	Control input voltage range <sup>(3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(3) (4)</sup>	Dn+, Dn-	-0.5 $V_{CC} + 0.3$	V
		D+, D- when $V_{CC} > 0$	-0.5 $V_{CC} + 0.3$	
		D+, D- when $V_{CC} = 0$	-0.5 5.25	
$I_{IK}$	Control input clamp current	$V_{IN} < 0$	-50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$	-50	mA
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		±64	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .

(5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .

**PACKAGE THERMAL IMPEDANCE<sup>(1)</sup>**

		TYP	UNIT
$\theta_{JA}$	Package thermal impedance	DGS package	56.5
		RSW package	175

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	4.3	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 3\text{ V to }3.6\text{ V}$	1.3	V
		$V_{CC} = 4.3\text{ V}$	1.7	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 3\text{ V to }3.6\text{ V}$	0.5	V
		$V_{CC} = 4.3\text{ V}$	0.7	
$V_{I/O}$	Data input/output voltage	0	$V_{CC}$	V
$T_A$	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$		$V_{CC} = 3\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$I_{IN}$	Control inputs	$V_{CC} = 4.3\text{ V}$ , 0 V,	$V_{IN} = 0\text{ to }4.3\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{OZ}$ <sup>(3)</sup>		$V_{CC} = 4.3\text{ V}$ , $V_I = 0$ ,	$V_O = 0\text{ to }3.6\text{ V}$ , Switch OFF			$\pm 1$	$\mu\text{A}$
$I_{OFF}$	D+ and D-	$V_{CC} = 0\text{ V}$ , $V_I = 0$ ,	$V_O = 0\text{ to }4.3\text{ V}$ , $V_{IN} = V_{CC}\text{ or GND}$			$\pm 2$	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 4.3\text{ V}$ ,	$I_{I/O} = 0$ ,			1	$\mu\text{A}$
$\Delta I_{CC}$ <sup>(4)</sup>	Control inputs	$V_{CC} = 4.3\text{ V}$ ,	$V_{IN} = 2.6\text{ V}$			10	$\mu\text{A}$
$C_{in}$	Control inputs	$V_{CC} = 0\text{ V}$ ,	$V_{IN} = V_{CC}\text{ or GND}$		1		pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$ ,	$V_{I/O} = 3.3\text{ V or }0$ ,	Switch OFF	2		pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$ ,	$V_{I/O} = 3.3\text{ V or }0$ ,	Switch ON	7.5		pF
$r_{on}$ <sup>(5)</sup>		$V_{CC} = 3\text{ V}$ ,	$V_I = 0.4$ ,	$I_O = -8\text{ mA}$	6	10	$\Omega$
$\Delta r_{on}$		$V_{CC} = 3\text{ V}$ ,	$V_I = 0.4$ ,	$I_O = -8\text{ mA}$	0.35		$\Omega$
$r_{on(flat)}$		$V_{CC} = 3\text{ V}$ ,	$V_I = 0\text{ V or }1\text{ V}$ ,	$I_O = -8\text{ mA}$	2		$\Omega$

(1)  $V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## DYNAMIC ELECTRICAL CHARACTERISTICS

 over operating range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 10\%$ ,  $\text{GND} = 0\text{ V}$ 

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	UNIT
X <sub>TALK</sub>	Crosstalk	$R_L = 50\ \Omega$ , $f = 240\text{ MHz}$ , See <a href="#">Figure 10</a>	-54	dB
O <sub>ISO</sub>	OFF isolation	$R_L = 50\ \Omega$ , $f = 240\text{ MHz}$ , See <a href="#">Figure 9</a>	-40	dB
BW	Bandwidth (-3 dB)	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 11</a>	900	MHz

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

## SWITCHING CHARACTERISTICS

 over operating range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 10\%$ ,  $\text{GND} = 0\text{ V}$ 

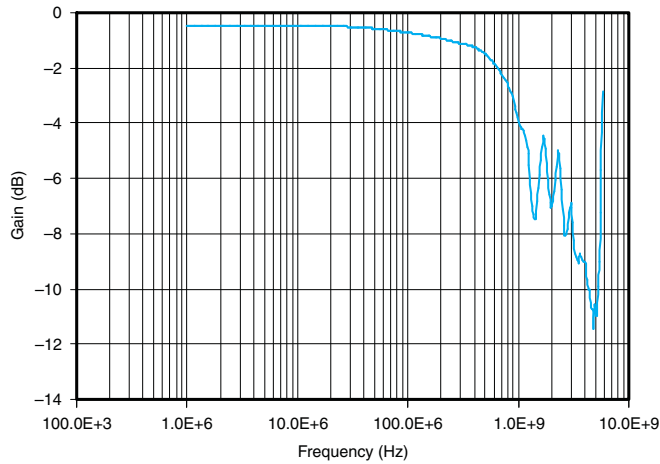
PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>pd</sub>	Propagation delay <sup>(2) (3)</sup>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 12</a>		0.25		ns
t <sub>ON</sub>	Line enable time, SEL to D, nD	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 8</a>			30	ns
t <sub>OFF</sub>	Line disable time, SEL to D, nD	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 8</a>			25	ns
t <sub>ON</sub>	Line enable time, $\overline{\text{OE}}$ to D, nD	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 8</a>			30	ns
t <sub>OFF</sub>	Line disable time, $\overline{\text{OE}}$ to D, nD	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 8</a>			25	ns
t <sub>SK(O)</sub>	Output skew between center port to any other port <sup>(2)</sup>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 13</a>			50	ps
t <sub>SK(P)</sub>	Skew between opposite transitions of the same output (t <sub>PHL</sub> - t <sub>PLH</sub> ) <sup>(2)</sup>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , See <a href="#">Figure 13</a>			20	ps
t <sub>J</sub>	Total jitter <sup>(2)</sup>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , t <sub>R</sub> = t <sub>F</sub> = 500 ps at 480 Mbps (PRBS = 2 <sup>15</sup> - 1)			20	ps

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

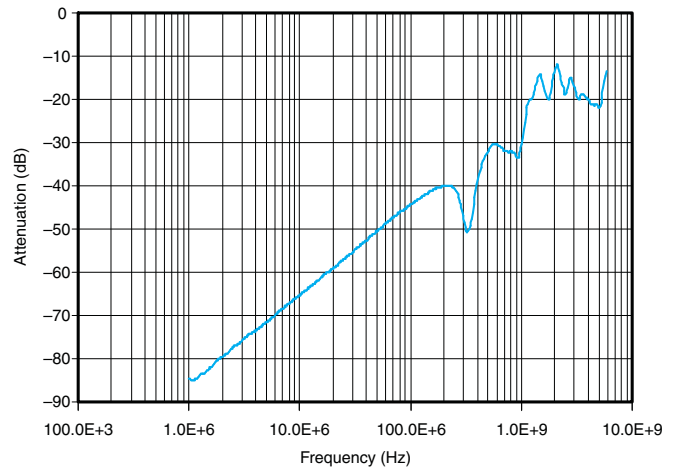
(2) Specified by design

(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

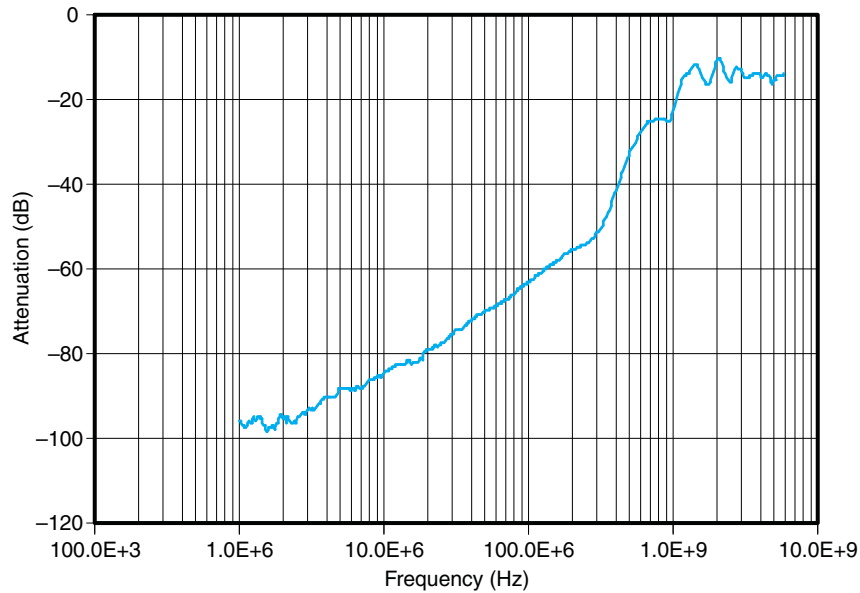
**APPLICATION INFORMATION**



**Figure 1. Gain vs Frequency**



**Figure 2. OFF Isolation**



**Figure 3. Crosstalk**

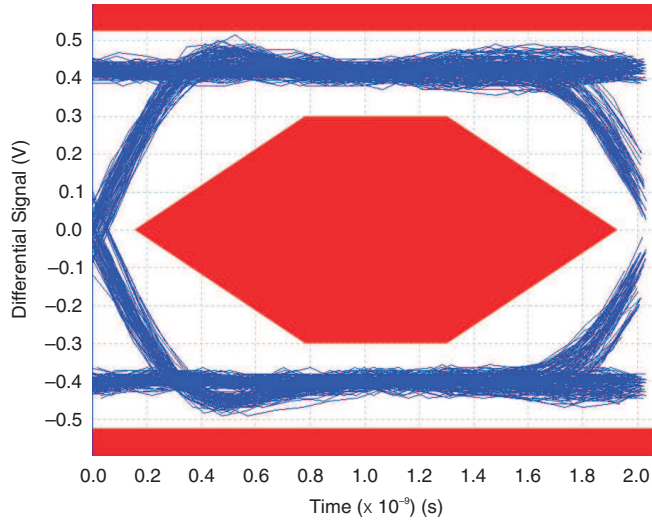


Figure 4. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

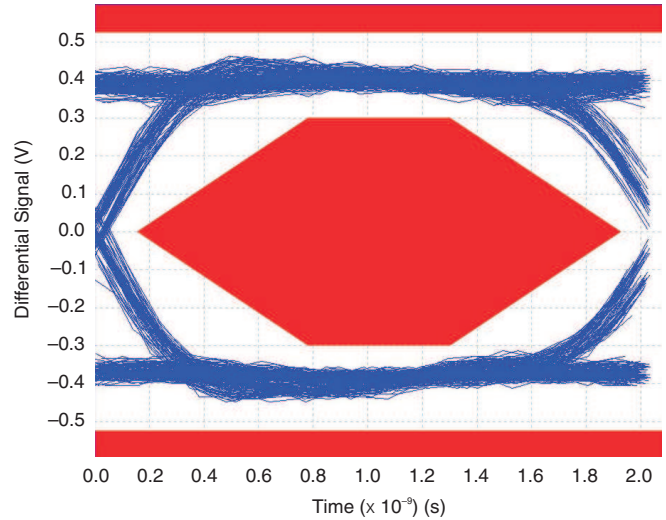


Figure 5. Eye Pattern: 480-Mbps USB Signal With Switch NC Path

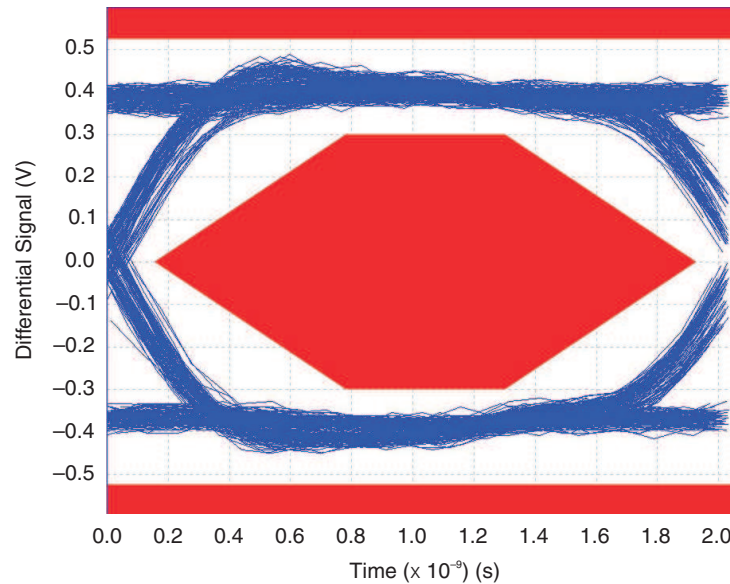


Figure 6. Eye Pattern: 480-Mbps USB Signal With Switch NO Path

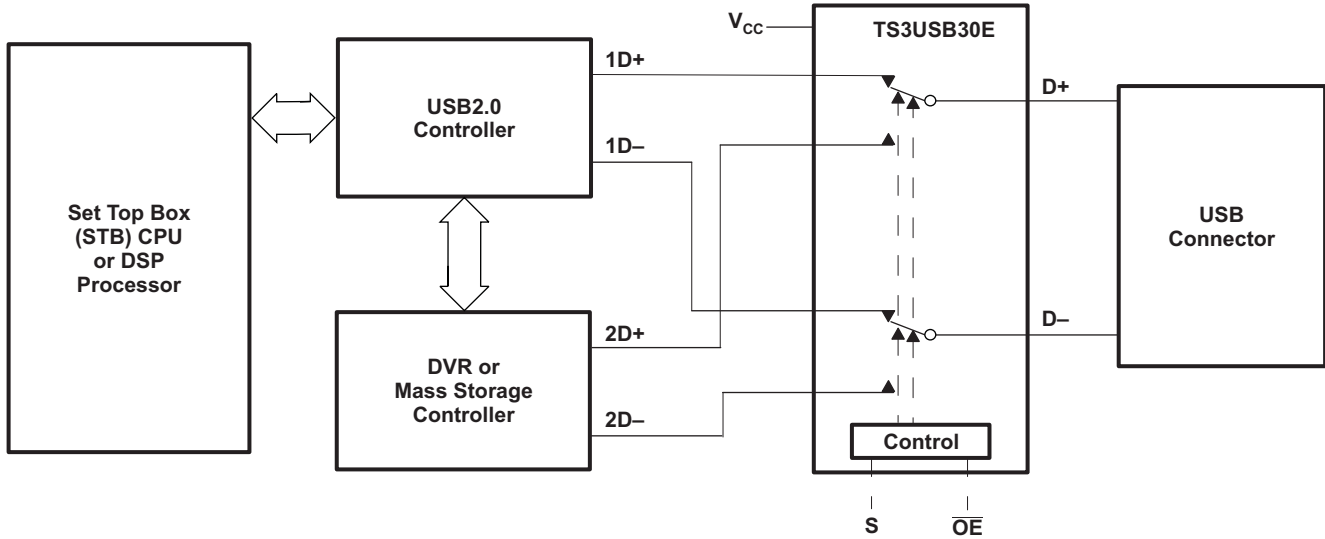
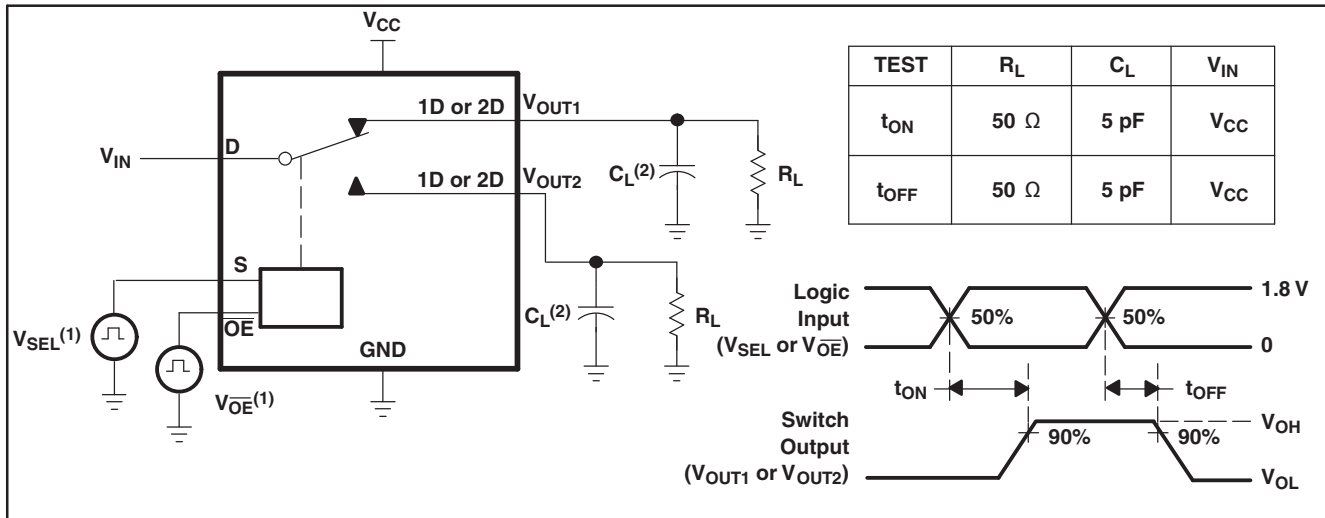


Figure 7. Application Diagram

PARAMETER MEASUREMENT INFORMATION



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.  
 (2) C<sub>L</sub> includes probe and jig capacitance.

Figure 8. Turn-On (t<sub>ON</sub>) and Turn-Off Time (t<sub>OFF</sub>)



PARAMETER MEASUREMENT INFORMATION (continued)

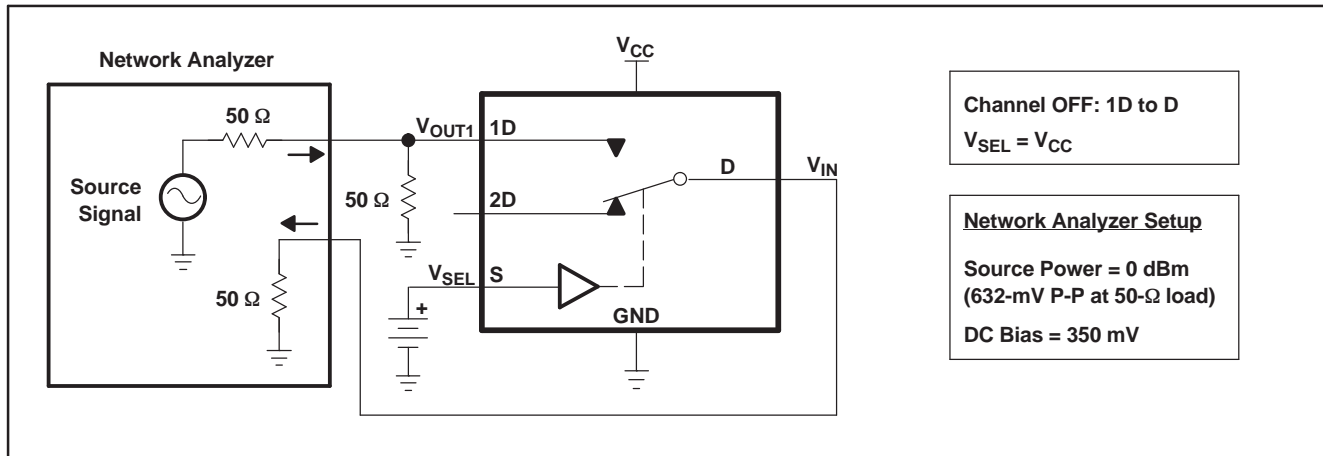


Figure 9. OFF Isolation ( $O_{ISO}$ )

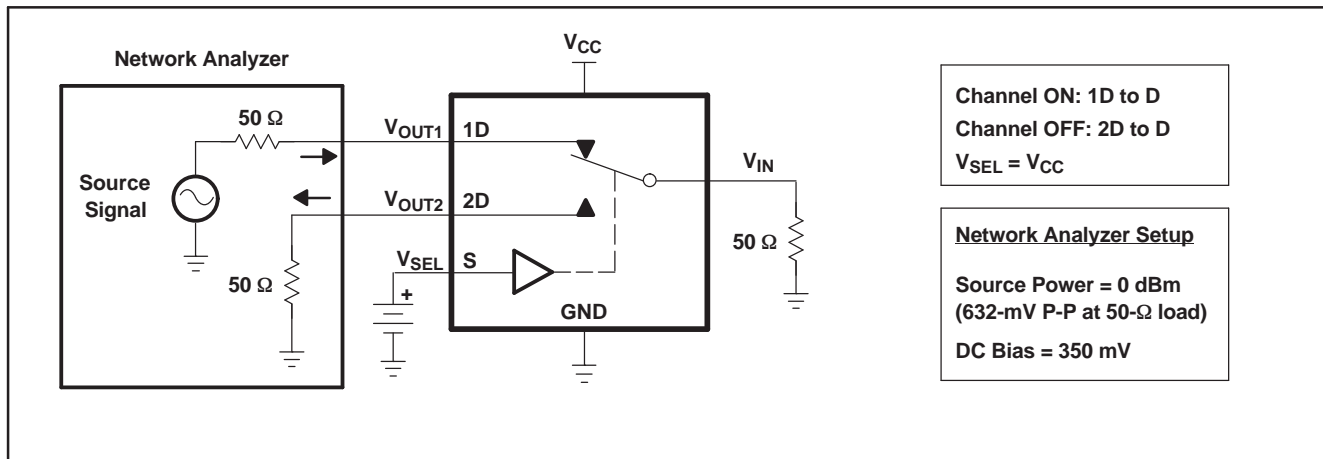


Figure 10. Crosstalk ( $X_{TALK}$ )

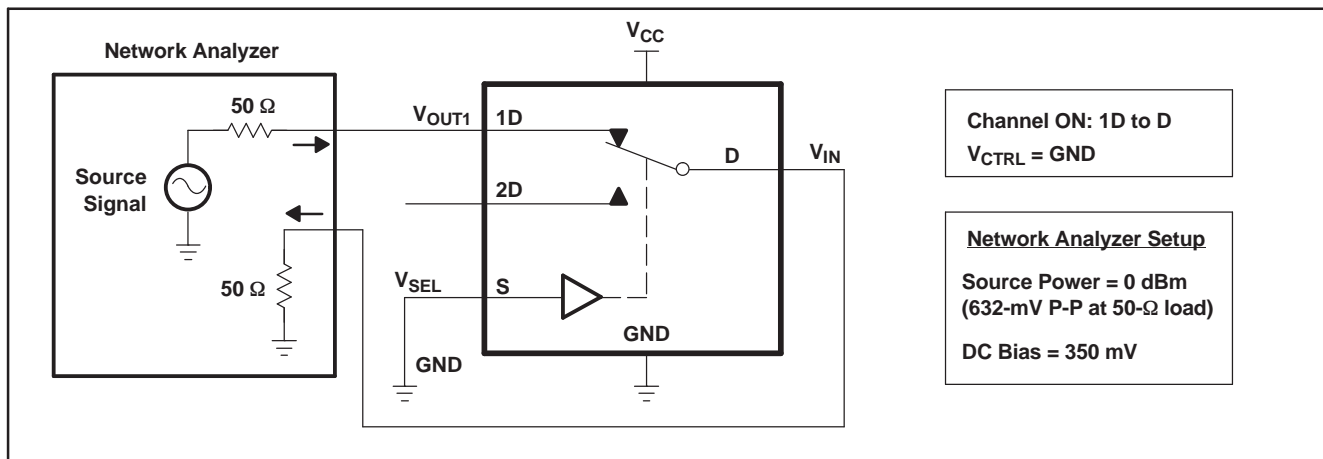
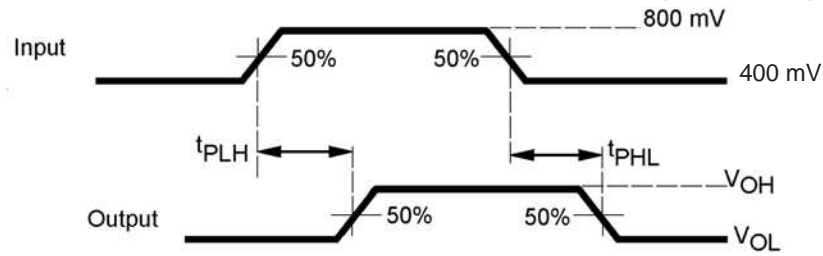
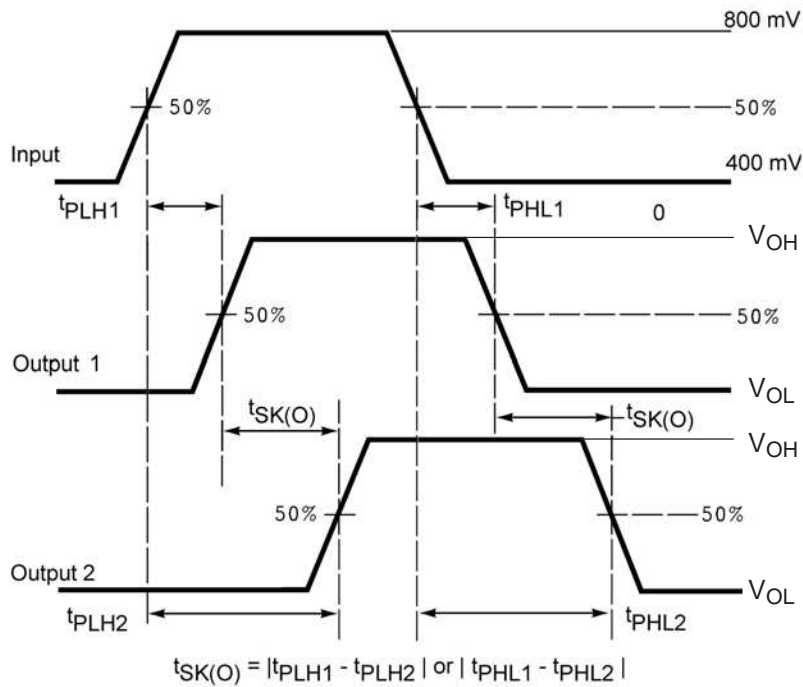
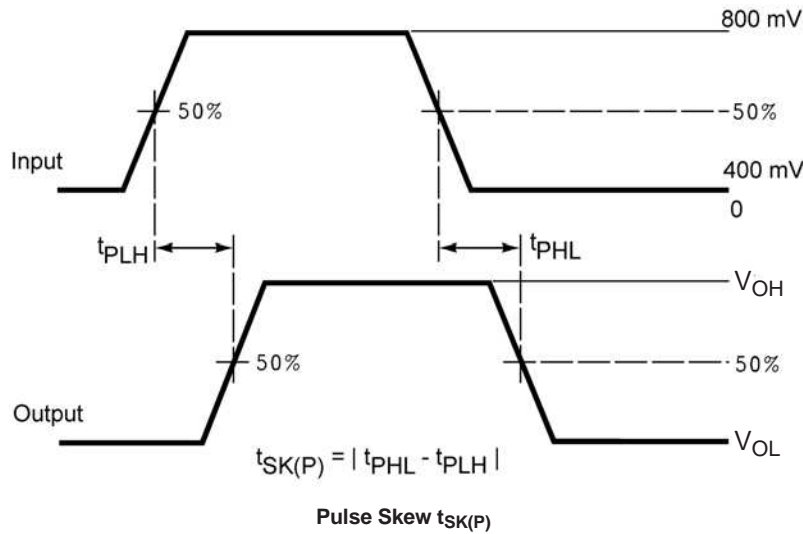


Figure 11. Bandwidth (BW)

**PARAMETER MEASUREMENT INFORMATION (continued)**



**Figure 12. Propagation Delay**



**Figure 13. Skew Test**

PARAMETER MEASUREMENT INFORMATION (continued)

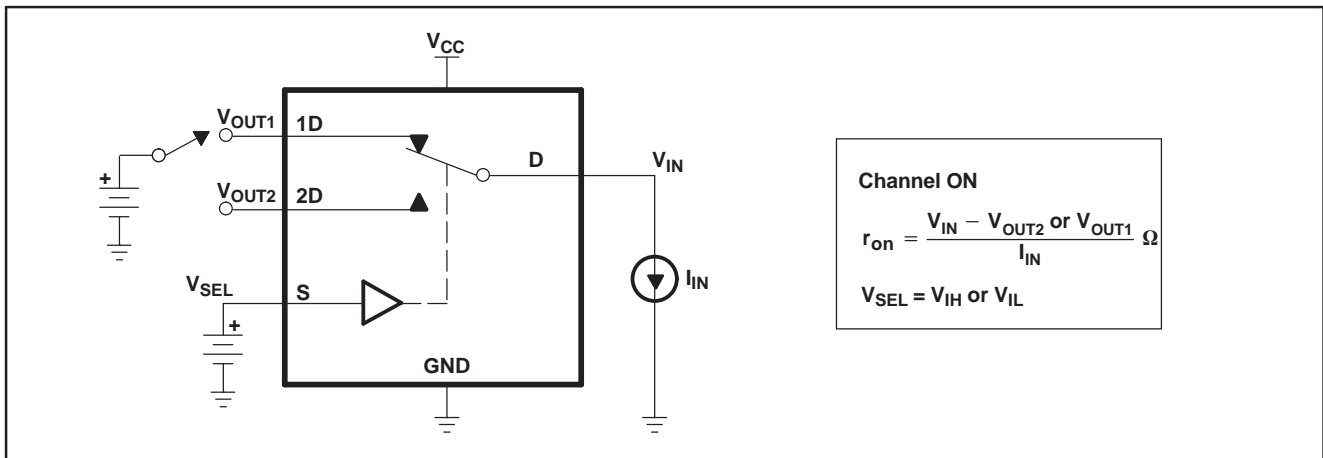


Figure 14. ON-State Resistance ( $r_{on}$ )

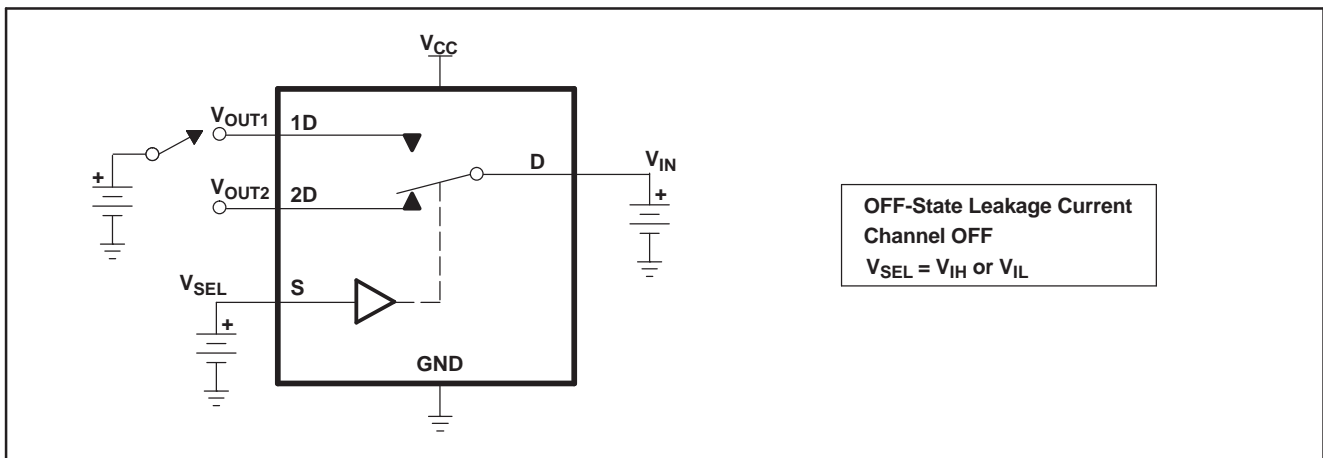


Figure 15. OFF-State Leakage Current

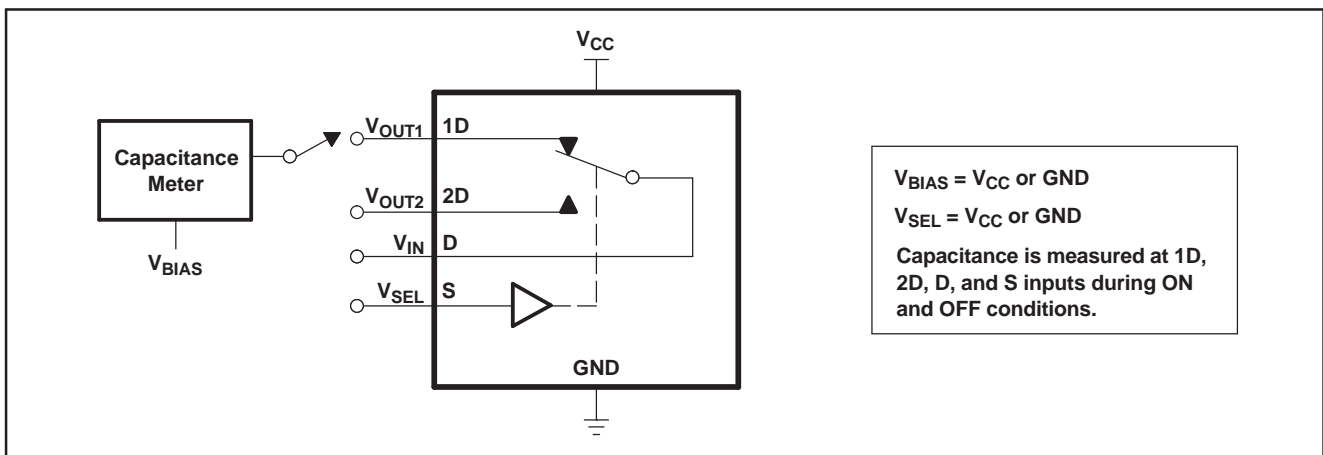


Figure 16. Capacitance

## REVISION HISTORY

Changes from Revision D (September 2010) to Revision E	Page
• Updated ORDERING INFORMATION TABLE. ....	<a href="#">2</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB30EDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L6Q ~ L6R)	<a href="#">Samples</a>
TS3USB30ERSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LY7 ~ LYO)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB30EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS3USB30ERSWR	UQFN	RSW	10	3000	179.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
TS3USB30ERSWR	UQFN	RSW	10	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

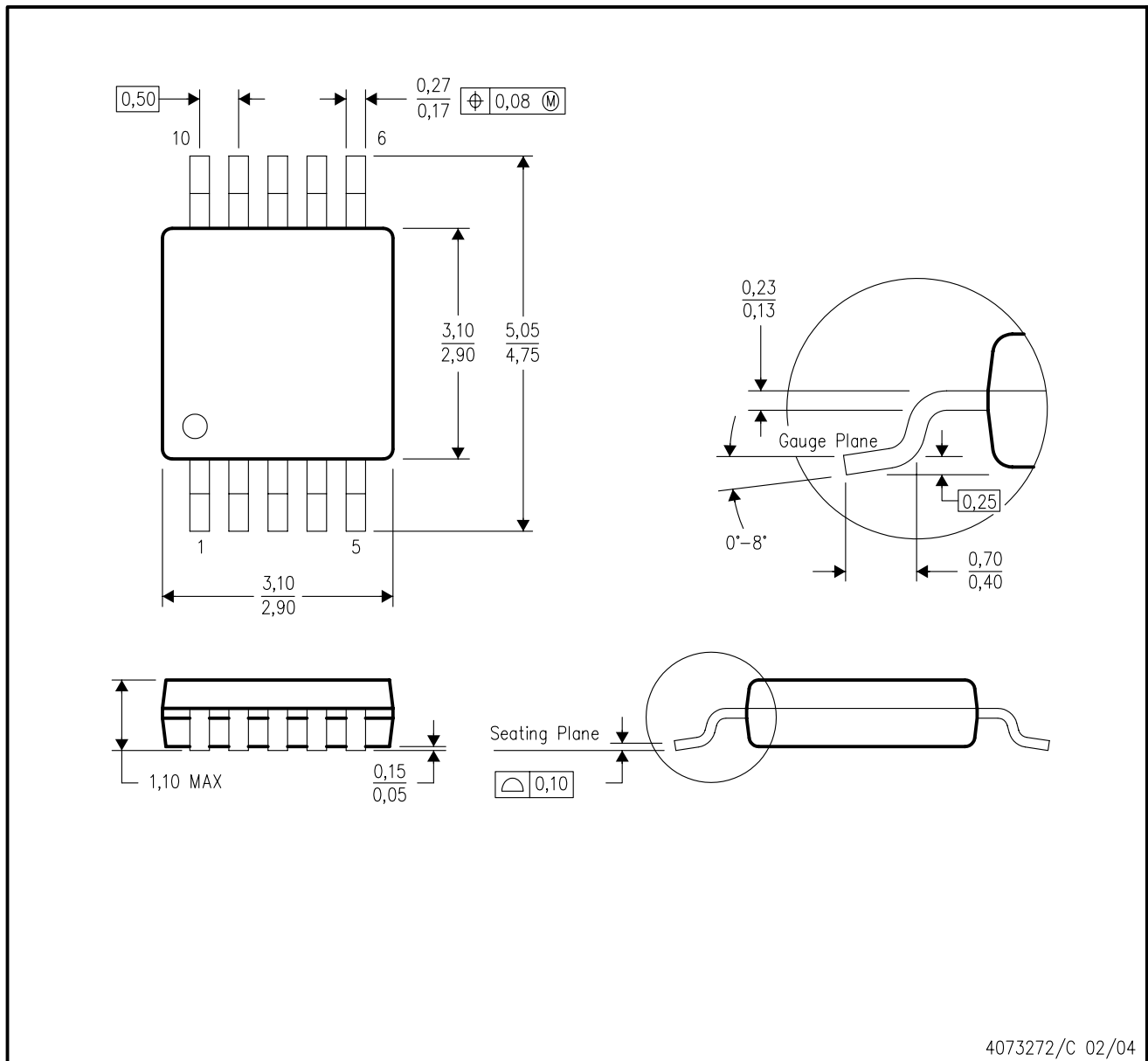

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB30EDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS3USB30ERSWR	UQFN	RSW	10	3000	203.0	203.0	35.0
TS3USB30ERSWR	UQFN	RSW	10	3000	184.0	184.0	19.0



DGS (S-PDSO-G10)

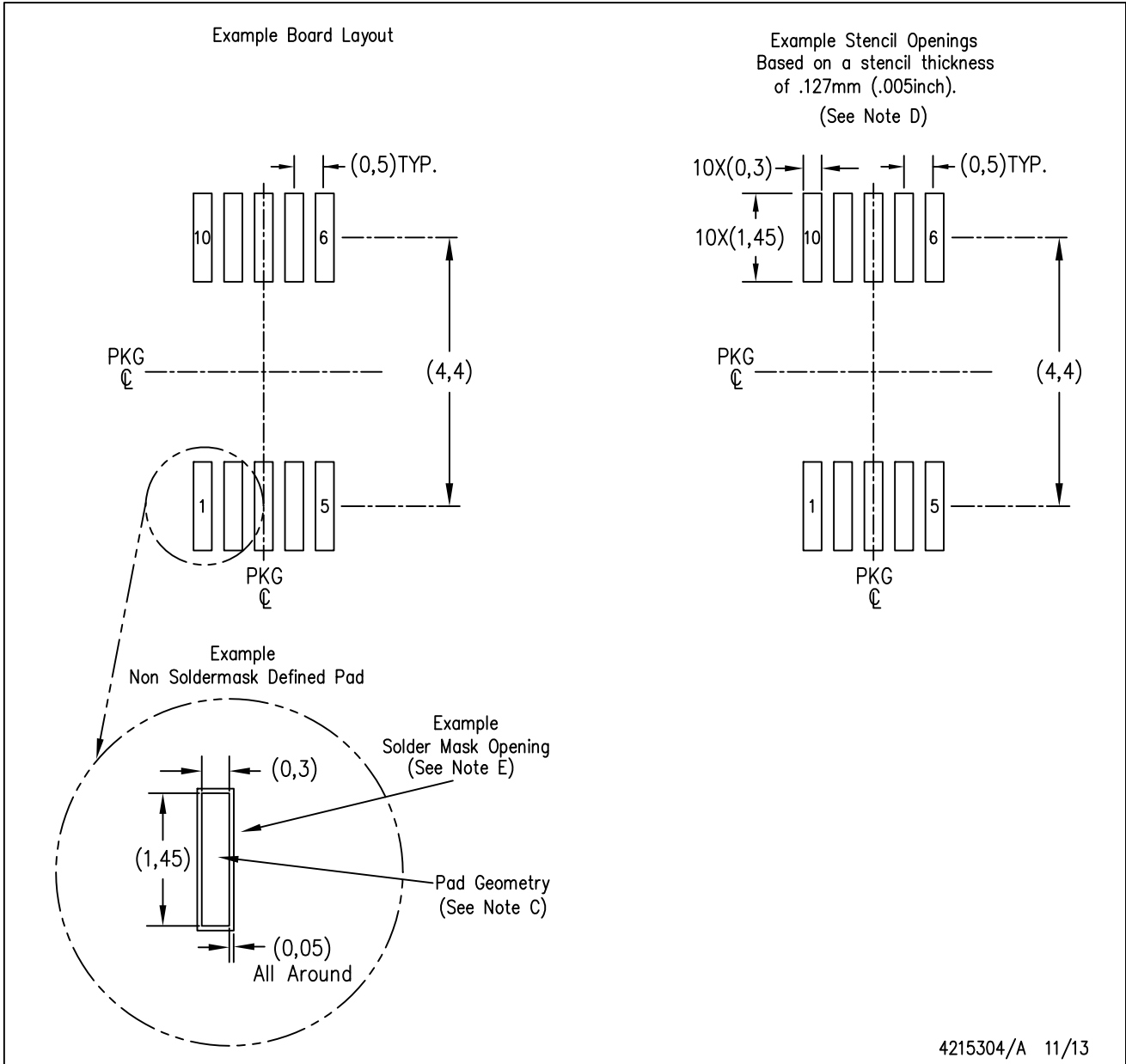
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

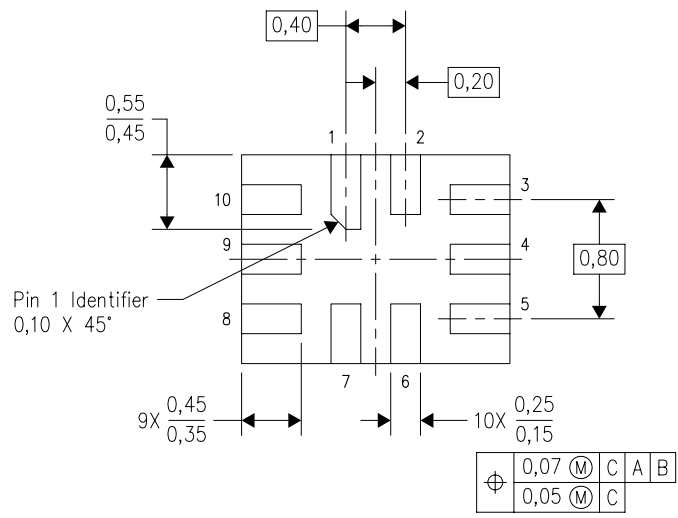
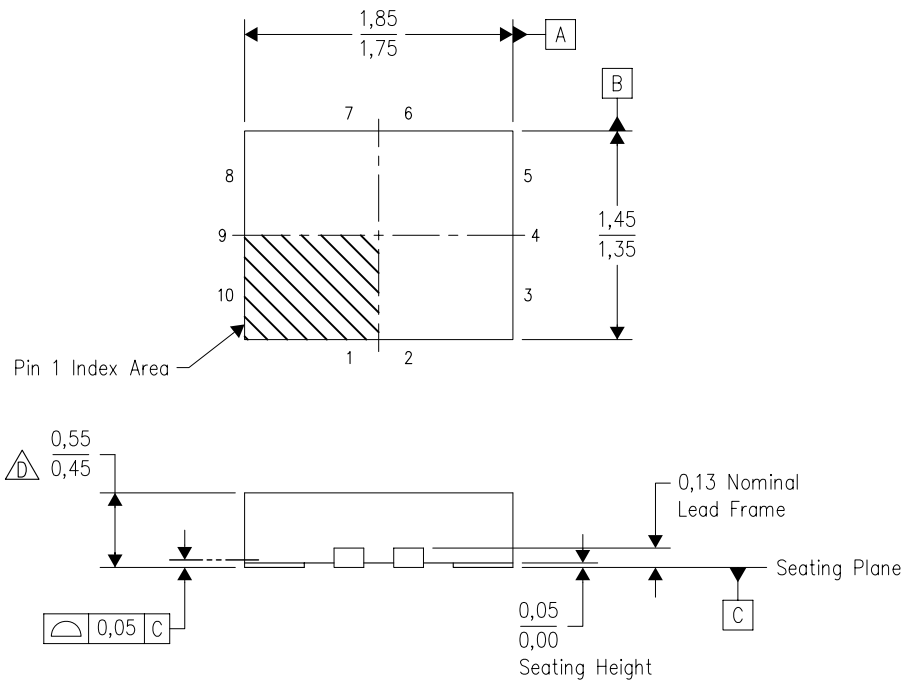
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSW (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



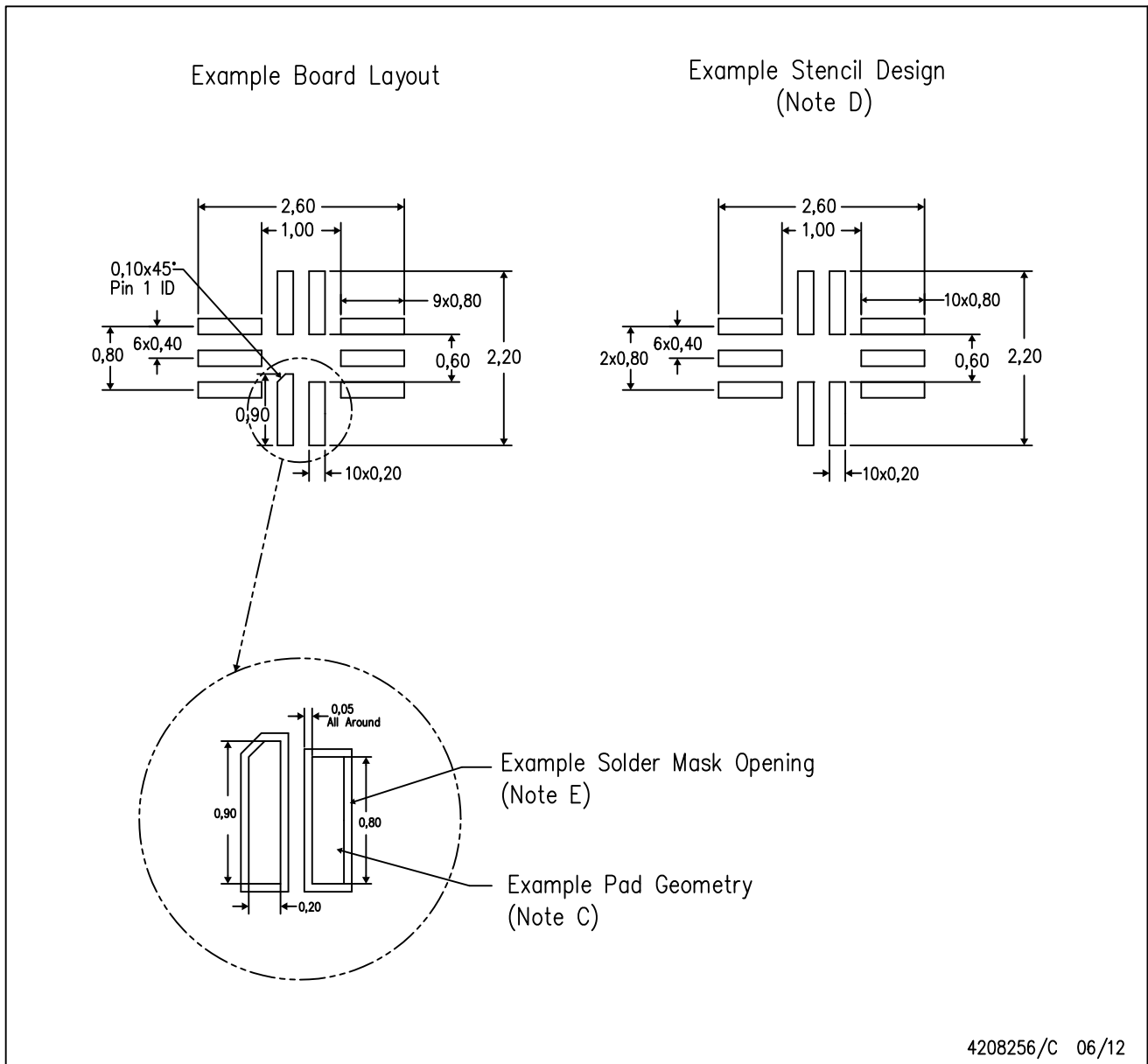
Bottom View

4208097/C 07/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-lead) package configuration.
- This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

RSW (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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