











DS26C31M, DS26C31T

SNLS375C -JUNE 1998-REVISED JANUARY 2015

DS26C31x CMOS Quad Tri-State Differential Line Driver

Features

- TTL Input Compatible
- Typical Propagation Delays: 6 ns
- Typical Output Skew: 0.5 ns
- Outputs Will Not Load Line When $V_{CC} = 0 \text{ V}$
- DS26C31T Meets the Requirements of EIA Standard RS-422
- Operation From Single 5-V Supply
- Tri-State Outputs for Connection to System Buses
- Low Quiescent Current
- Available in Surface Mount
- Mil-Std-883C Compliant

Applications

Differential Line Driver for RS-422 Applications

3 Description

The DS26C31 device is a guad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken⁽²⁾. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

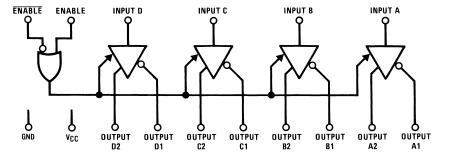
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS26C31M	SNLS3759577	9.90 mm × 3.91 mm
DS20C3TW	PDIP (16)	19.304 mm × 6.35 mm
DCCCCCAT	SNLS3759577	9.90 mm × 3.91 mm
DS26C31T	PDIP (16)	19.304 mm × 6.35 mm

- (1) For all available packages, see the orderable addendum at the end of the datasheet.
- The DS26C31M (-55°C to 125°C) is tested with VOLIT between 6 V and 0 V while RS-422A condition is 6 V and -0.25 V.

4 Device Logic Diagram





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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C

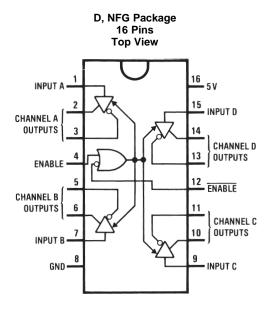
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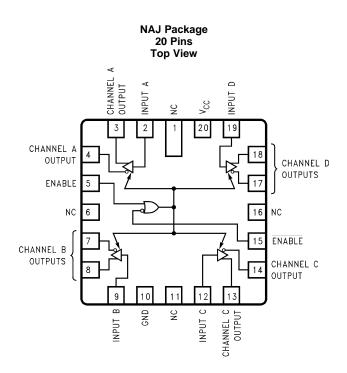
Changes from Revision A (April 2013) to Revision B

Page



6 Pin Configuration and Functions





Pin Functions

PI	N	I/O	DESCRIPTION
NAME	NO. ⁽¹⁾	1/0	DESCRIPTION
DIFFERENTIAL SI	GNALING I/O		
CHANNEL A OUTPUTS (-, +)	3, 2	0	Channel A inverting and non-inverting differential driver outputs
CHANNEL B OUTPUTS (-, +)	5, 6	0	Channel B inverting and non-inverting differential driver outputs
CHANNEL C OUTPUTS (-, +)	11, 10	0	Channel C inverting and non-inverting differential driver outputs
CHANNEL D OUTPUTS (-, +)	13, 14	0	Channel D inverting and non-inverting differential driver outputs
INPUT A	1	I	TTL/CMOS compatible input for channel A
INPUT B	7	I	TTL/CMOS compatible input for channel B
INPUT C	9	I	TTL/CMOS compatible input for channel C
INPUT D	15	I	TTL/CMOS compatible input for channel D
CONTROL PINS		•	
ENABLE	4	I	Logic-high ENABLE Control
ENABLE	12	I	Logic-low ENABLE Control
POWER		•	
GND	8	_	GND Pin
VCC	16		Supply pin, provide 5 V supply

(1) Pin numbers correspond to PDIP and SOIC packages.



7 Specifications

7.1 Absolute Maximum Ratings (1)(2)(3)

		MIN	MAX	UNIT
Supply Voltage (V _{CC})		-0.5	7	V
DC Input Voltage (V _{IN})		-1.5	V _{CC} +1.5	V
DC Output Voltage (V _{OUT})		-0.5	7	V
Clamp Diode Current (I _{IK} , I _{OK})		-20	20	mA
DC Output Current, per pin (I _{OUT})		-150	150	mA
DC V _{CC} or GND Current, per pin (I _{CC})				
Max Power Dissipation (P _D) at 25°C (4)	Ceramic "NFE" package		2419	mW
	Plastic "NFG" package		1736	mW
	SOIC "D" package		1226	mW
	Ceramic "NAD" package		1182	mW
	Ceramic "NAJ" package		2134	mW
Lead Temperature (T _L)	(Soldering, 4 s)		260	°C
Storage Temperature, T _{stg}		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply Voltage (V _{CC})	4.50	5.50	V	
DC Input or Output Voltage	(V _{IN} , V _{OUT})	0	V_{CC}	V
Operating Temperature Range (T _A)	DS26C31T	-40	85	°C
	DS26C31M	-55	125	°C
Input Rise or Fall Times (t _r , t _f)			500	ns

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⁽²⁾ Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

⁽³⁾ If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

⁽⁴⁾ Ratings apply to ambient temperature at 25°C. Above this temperature derate NFG package at 13.89 mW/°C, NFE package 16.13 mW/°C, D package 9.80 mW/°C, NAJ package 12.20 mW/°C, and NAD package 6.75 mW/°C.



7.3 DC Electrical Characteristics

 $V_{CC} = 5 \text{ V} \pm 10\% \text{ (unless otherwise specified)}^{(1)}$

	PARAMETER	TE	ST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	High Level Input Voltage			2.0			V
V _{IL}	Low Level Input Voltage					0.8	V
V _{OH}	High Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	,	2.5	3.4		V
		I _{OUT} = −20 mA					
V _{OL}	Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}	,		0.3	0.5	V
		$I_{OUT} = 20 \text{ mA}$					
V _T	Differential Output Voltage	$R_L = 100 \Omega$		2.0	3.1		V
		See ⁽²⁾					
$ V_T - \overline{V_T} $	Difference In Differential Output	$R_L = 100 \Omega$				0.4	V
		See ⁽²⁾					
V _{OS}	Common Mode Output Voltage	$R_L = 100 \Omega$			1.8	3.0	V
		See ⁽²⁾					
$ V_{OS} - \overline{V}_{OS} $ Difference In Common Mode		$R_L = 100 \Omega$			0.4	V	
	Output	See ⁽²⁾					
I _{IN}	Input Current	$V_{IN} = V_{CC}$, GNE	O, V _{IH} , or V _{IL}			±1.0	μΑ
I _{CC}	Quiescent Supply Current (3)	DS26C31T	$V_{IN} = V_{CC}$ or GND		200	500	μΑ
		$I_{OUT} = 0 \mu A$	$V_{IN} = 2.4 \text{ V or } 0.5 \text{ V}^{(3)}$		0.8	2.0	mA
		DS26C31M	$V_{IN} = V_{CC}$ or GND		200	500	μΑ
		$I_{OUT} = 0 \mu A$	$V_{IN} = 2.4 \text{ V or } 0.5 \text{ V}^{(3)}$		0.8	2.1	mA
I_{OZ}	TRI-STATE Output Leakage	$V_{OUT} = V_{CC}$ or Q	GND				
	Current	ENABLE = V _{IL}		±0.5	±5.0	μΑ	
		ENABLE = V _{IH}					
I _{SC}	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GI	ND ⁽²⁾⁽⁴⁾	-30		-150	mA
I _{OFF}	Output Leakage Current Power	DS26C31T	V _{OUT} = 6 V			100	μΑ
	Off ⁽²⁾	$V_{CC} = 0 V$	V _{OUT} = −0.25 V			-100	μΑ
		DS26C31M	V _{OUT} = 6 V			100	μΑ
		$V_{CC} = 0 V$	$V_{OUT} = 0 V^{(5)}$			-100	μΑ

⁽¹⁾ Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

⁽²⁾ See EIA Specification RS-422 for exact test conditions.

⁽³⁾ Measured per input. All other inputs at V_{CC} or GND.

⁽⁴⁾ This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

⁽⁵⁾ The DS26C31M (-55°C to +125°C) is tested with V_{OUT} between +6 V and 0 V while RS-422A condition is +6 V and -0.25 V.



7.4 Switching Characteristics

 $V_{CC} = 5 \text{ V} \pm 10\%$, $t_r \le 6 \text{ ns}$, $t_f \le 6 \text{ ns}$ (Figure 22, Figure 23, Figure 24, Figure 25)⁽¹⁾

	PARAMETER	TEST CONDITIONS	MIN	TYP	DS26C31T	DS26C31M	UNIT
PARAMETER		TEST CONDITIONS	IVIIIN	ITP	MAX	MAX	UNII
t _{PLH} , t _{PHL}	Propagation Delays Input to Output	S1 Open	2	6	11	14	ns
Skew	(2)	S1 Open		0.5	2.0	3.0	ns
t _{TLH} , t _{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	14	ns
t _{PZH}	Output Enable Time	S1 Closed		11	19	22	ns
t _{PZL}	Output Enable Time	S1 Closed		13	21	28	ns
t _{PHZ}	Output Disable Time (3)	S1 Closed		5	9	12	ns
t _{PLZ}	Output Disable Time ⁽³⁾	S1 Closed		7	11	14	ns
C _{PD}	Power Dissipation Capacitance (4)			50			pF
C _{IN}	Input Capacitance			6			pF

- (1) Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for V_{CC} = 5 V and T_A = 25°C.
- (2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
- (3) Output disable time is the delay from ENABLE or ENABLE being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
- (4) C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}2 f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

7.5 Comparison Table of Switching Characteristics into "LS-Type" Load

 $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, $t_r \le 6 \text{ ns}$, $t_f \le 6 \text{ ns}$ (Figure 23, Figure 25, Figure 26, Figure 27) (1)

	DADAMETED	TEST	DS26C	31T	DS26LS	31C	UNIT
	PARAMETER	CONDITIONS	TYP	MAX	TYP	MAX	UNII
t _{PLH} , t _{PHL}	Propagation Delays Input to Output	C _L = 30 pF					
		S1 Closed	6	8	10	15	ns
		S2 Closed					
Skew	See ⁽²⁾	C _L = 30 pF					
		S1 Closed	0.5	1.0	2.0	6.0	ns
		S2 Closed					
t _{THL} , t _{TLH}	Differential Output Rise and Fall	C _L = 30 pF					
	Times	S1 Closed	4	6			ns
		S2 Closed					
t _{PLZ}	Output Disable Time ⁽³⁾	C _L = 10 pF					
		S1 Closed	6	9	15	35	ns
		S2 Open					
t _{PHZ}	Output Disable Time ⁽³⁾	C _L = 10 pF					
		S1 Open	4	7	15	25	ns
		S2 Closed					
t _{PZL}	Output Enable Time	C _L = 30 pF					
		S1 Closed	14	20	20	30	ns
		S2 Open					
t _{PZH}	Output Enable Time	C _L = 30 pF					
		S1 Open	11	17	20	30	ns
		S2 Closed					

⁽¹⁾ This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or verified.

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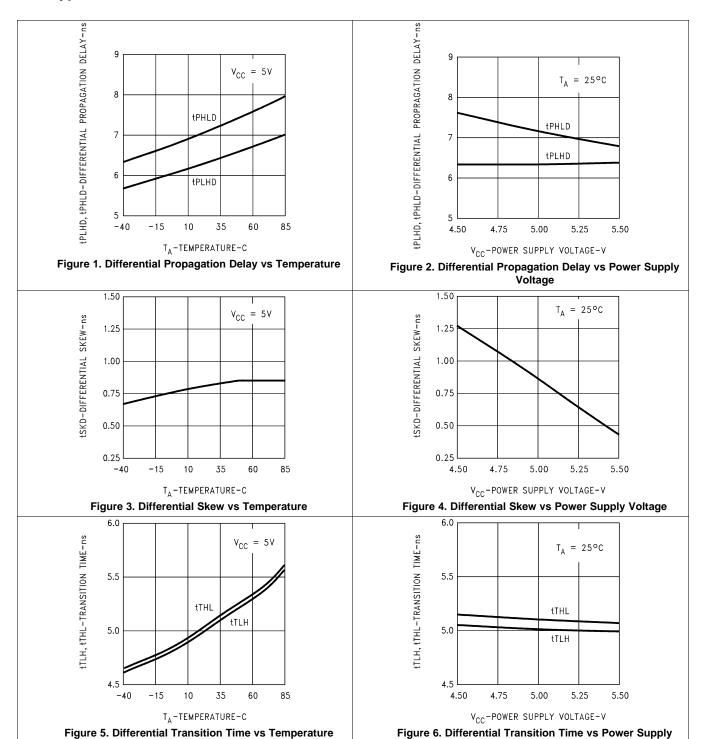
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⁽²⁾ Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

⁽³⁾ Output disable time is the delay from ENABLE or ENABLE being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.



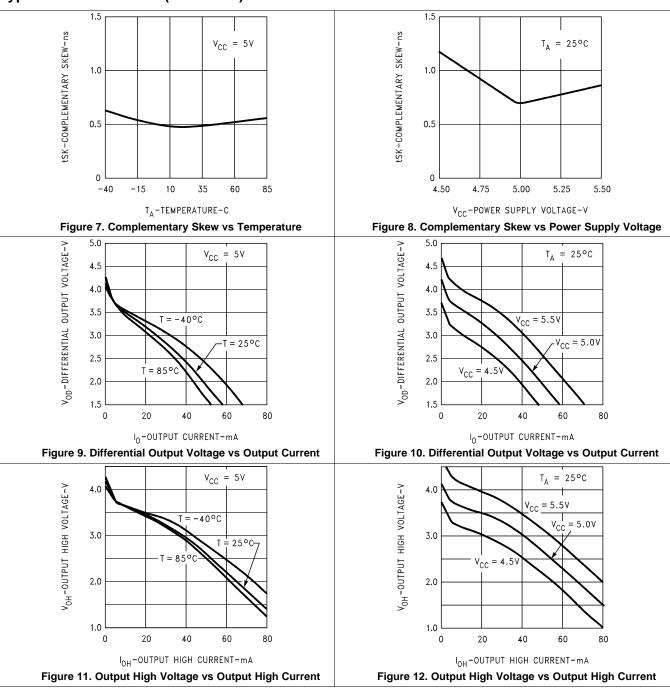
7.6 Typical Characteristics



Voltage

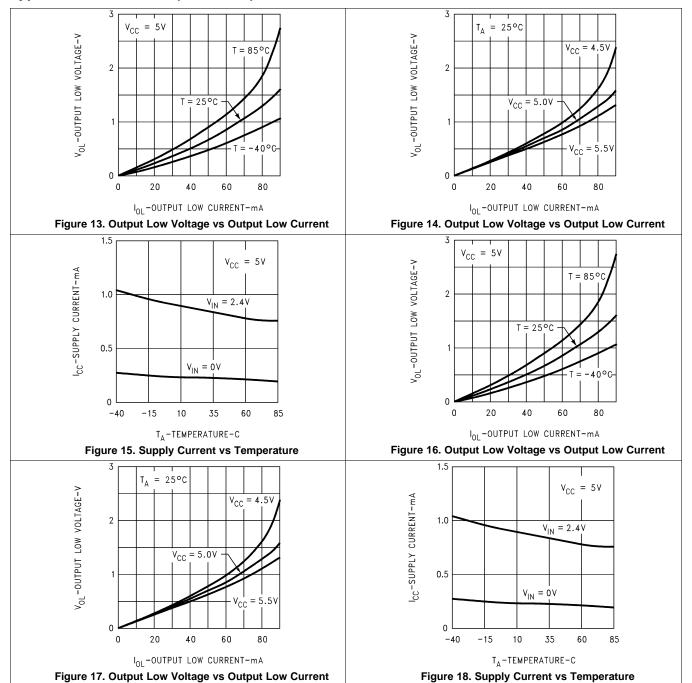


Typical Characteristics (continued)



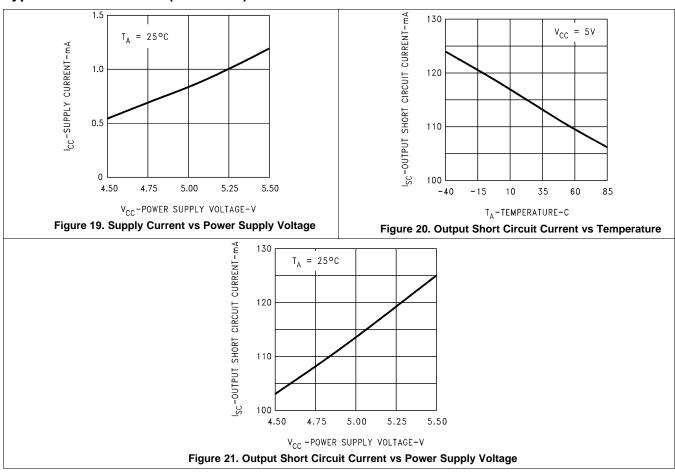


Typical Characteristics (continued)



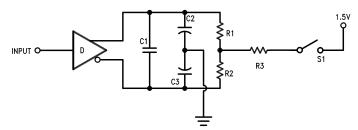


Typical Characteristics (continued)





8 Parameter Measurement Information



Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω , R3 = 500Ω .

Figure 22. AC Test Circuit

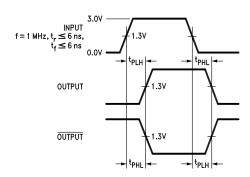


Figure 23. Propagation Delays

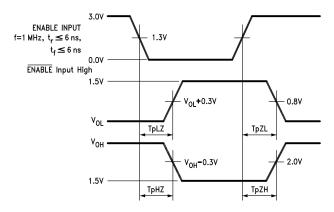
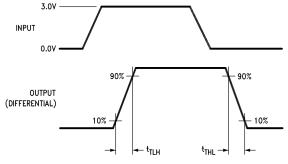


Figure 24. Enable and Disable Times



Input pulse; f = 1 MHz, 50%; $t_r \le 6$ ns, $t_f \le 6$ ns

Figure 25. Differential Rise and Fall Times

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Parameter Measurement Information (continued)

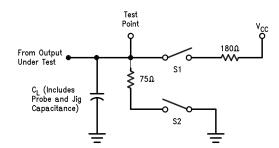


Figure 26. Load AC Test Circuit for "LS-Type" Load

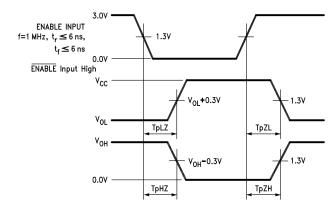


Figure 27. Enable and Disable Times for "LS-Type" Load

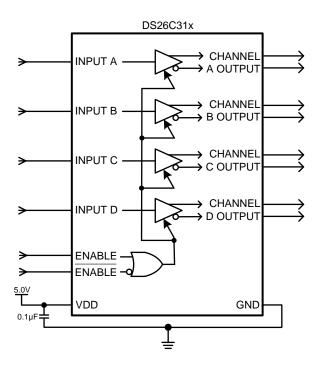


9 Detailed Description

9.1 Overview

The DS26C31 is a quad differential line driver designed for data transmission over balanced cable or printed circuit board traces. The DS26C31M supports a temperature range of -55°C to 125°C, while the DS26C31T supports a temperature range of -40°C to 85°C.

9.2 Functional Block Diagram



9.3 Feature Description

Each driver converts the TTL or CMOS signal at its input to a pair of complementary differential outputs. The drivers are enabled when the ENABLE control pin is a logic HIGH or when the ENABLE control pin is a logic LOW.

9.4 Device Functional Modes

Table 1. Function Table (1)

ENABLE	ENABLE	INPUT	NON-INVERTING OUTPUT	INVERTING OUTPUT
L	Н	X	Z	Z
All other combinatio	ns of enable inputs	L	L	Н
		Н	Н	L

(1) L = Low logic state

X = Irrelevant

H = High logic state

Z = Tri-state (high impedance)



10 Application and Implementation

NOTE

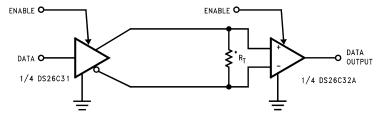
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DS26C31 is a quad differential line driver designed for applications that require long distance digital data transmission over balanced cables. The DS26C31 can be used in applications that require conversion from TTL or CMOS input levels to differential signal levels, compatible to RS-422. The use of complimentary signaling in a balanced transmission media provides good immunity in the midst of noisy environments or shifts in ground reference potential.

10.2 Typical Application

Figure 28 depicts a typical implementation of the DS26C31x device in a RS-422 application.



*R_T is optional although highly recommended to reduce reflection.

Figure 28. Two-Wire Balanced System, RS-422

10.2.1 Design Requirements

- Apply TTL or LVCMOS signal to driver input lines INPUT A-D.
- Transmit complementary outputs at OUTPUT A-D.
- Use controlled-impedance transmission lines such as printed circuit board traces, twisted-pair wires or parallel wire cable.
- Place a terminating resistor at the far end of the differential pair.

10.2.2 Detailed Design Procedure

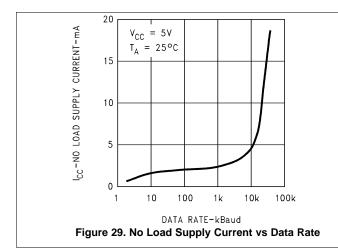
- Connect VCC and GND pins to the power and ground planes of the PCB with a 0.1-µF bypass capacitor.
- Use TTL/LVCMOS logic levels at INPUT A-D.
- Use controlled-impedance transmission media for the differential output signals.
- Place an optional terminating resistor at the far-end of the differential pair to avoid reflection.

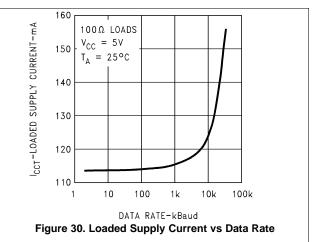
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Typical Application (continued)

10.2.3 Application Curves







11 Power Supply Recommendations

It is recommended that the supply (VCC) and ground (GND) pins be connected to power planes that are placed in the inner layers of the printed circuit board. A 0.1-µF bypass capacitor should be connect to the VCC pin such that the capacitor is as close as possible to the device.

12 Layout

12.1 Layout Guidelines

The output differential signals of the device should be routed on one layer of the board, and clearance should be provided in order to minimize crosstalk between differential pairs that may be running in parallel over a long distance. Additionally, the differential pairs should have a controlled impedance with minimum impedance discontinuities and be terminated at the far-end, near the receiver, with a resistor that is closely matched to the differential pair impedance in order to minimize transmission line reflections. The differential pairs should be routed with uniform trace width and spacing to minimize impedance mismatching.

12.2 Layout Example

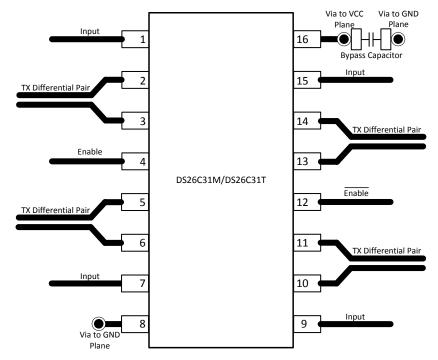


Figure 31. DS26C31 Example Layout

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13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
DS26C31M	226C31M Click here		Click here	Click here	Click here	
DS26C31T	DS26C31T Click here		Click here	Click here	Click here	

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Product Folder Links: DS26C31M DS26C31T





12-Oct-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty		Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
DS26C31TM	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS26C31TM	
DS26C31TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C31TM	Samples
DS26C31TMX	NRND	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS26C31TM	
DS26C31TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN Call TI	Level-1-260C-UNLIM	-40 to 85	DS26C31TM	Samples
DS26C31TN	NRND	PDIP	NFG	16	25	TBD	Call TI	Call TI	-40 to 85	DS26C31TN	
DS26C31TN/NOPB	ACTIVE	PDIP	NFG	16	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	DS26C31TN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

12-Oct-2014

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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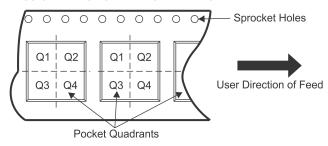
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

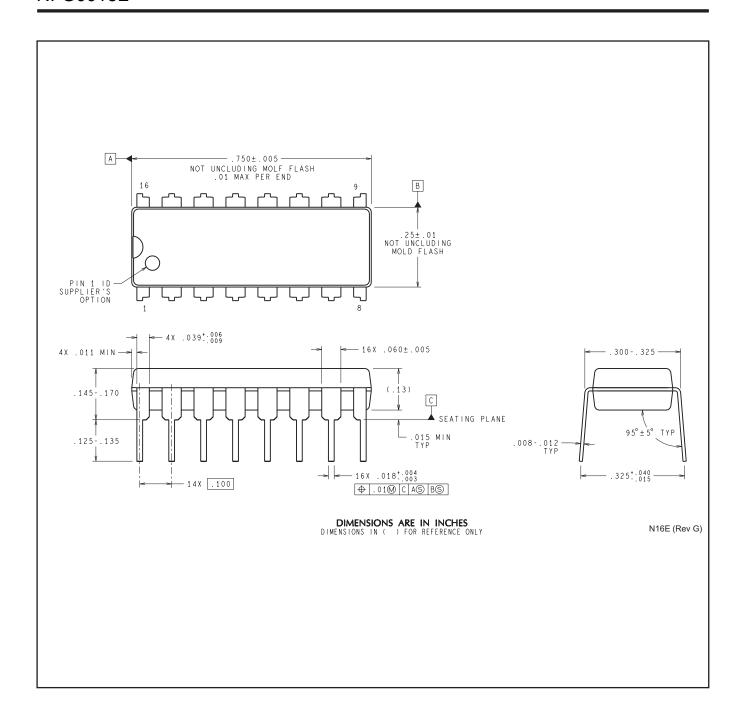
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26C31TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS26C31TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

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*All dimensions are nominal

Device Package Typ		Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
DS26C31TMX	SOIC	D	16	2500	367.0	367.0	35.0	
DS26C31TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0	



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



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