LP38691
LP38693 500mA Low Dropout CMOS Linear Regulators
Stable with Ceramic Output Capacitors

Check for Samples: LP38691, LP38693

FEATURES

- **All WSON Options are Available as AEC-Q100 Grade 1**
- **2.0% Output Accuracy (25°C)**
- **Low Dropout Voltage: 250 mV @ 500mA (typ, 5V out)**
- **Wide Input Voltage Range (2.7V to 10V)**
- **Precision (Trimmed) Bandgap Reference**
- **Ensured Specs for -40°C to +125°C**
- **1μA Off-State Quiescent Current**
- **Thermal Overload Protection**
- **Foldback Current Limiting**
- **PFM, SOT-223 and 6-Lead WSON Packages**
- **Enable Pin (LP38693)**

APPLICATIONS

- **Hard Disk Drives**
- **Notebook Computers**
- **Battery Powered Devices**
- **Portable Instrumentation**

DESCRIPTION

The LP38691/3 low dropout CMOS linear regulators provide tight output tolerance (2.0% typical), extremely low dropout voltage (250 mV @ 500mA load current, V_{OUT} = 5V), and excellent AC performance utilizing ultra low ESR ceramic output capacitors.

The low thermal resistance of the WSON, SOT-223 and PFM packages allow the full operating current to be used even in high ambient temperature environments.

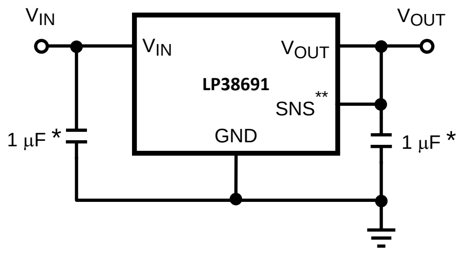
The use of a PMOS power transistor means that no DC base drive current is required to bias it allowing ground pin current to remain below 100 μA regardless of load current, input voltage, or operating temperature.

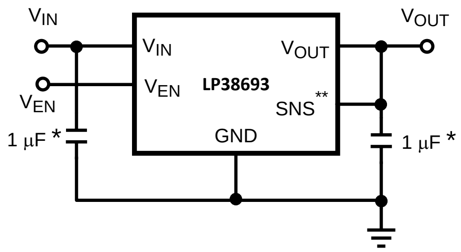
Dropout Voltage: 250 mV (typ) @ 500mA (typ. 5V out).

Ground Pin Current: 55 μA (typ) at full load.

Precision Output Voltage: 2.0% (25°C) accuracy.

Typical Application Circuits





* Minimum value required for stability.
**WSON package devices only.

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Connection Diagrams

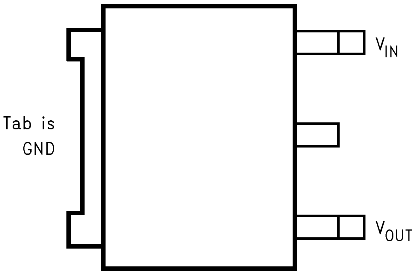


Figure 1. PFM (LP38691DT-X.X) – Top View
See Package Number NDP0003B

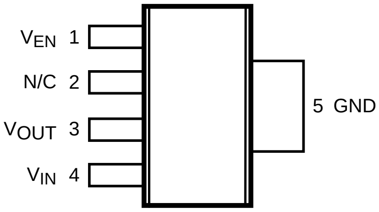


Figure 2. SOT-223 (LP38693MP-X.X) – Top View
See Package Number NDC0005A

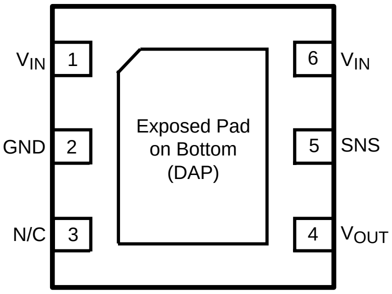


Figure 3. 6-Lead WSON (LP38691SD-X.X) – Top View
See Package Number NGG0006A

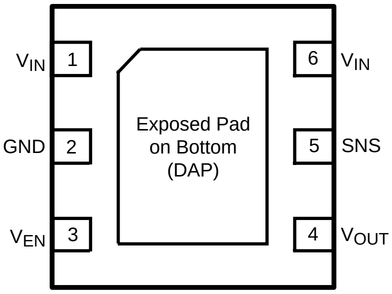


Figure 4. 6-Lead WSON (LP38693SD-X.X) – Top View
See Package Number NGG

PIN DESCRIPTIONS

Pin	Description
V_{IN}	This is the input supply voltage to the regulator. For WSON devices, both V_{IN} pins must be tied together for full current operation (250mA maximum per pin).
GND	Circuit ground for the regulator. For the PFM and SOT-223 packages this is thermally connected to the die and functions as a heat sink when the soldered down to a large copper plane.
SNS	Output sense pin allows remote sensing at the load which will eliminate the error in output voltage due to voltage drops caused by the resistance in the traces between the regulator and the load. This pin must be tied to V_{OUT}.
V_{EN}	The enable pin allows the part to be turned ON and OFF by pulling this pin high or low.
V_{OUT}	Regulated output voltage
DAP	WSON Only - The DAP (Exposed Pad) functions as a thermal connection when soldered to a copper plane. See WSON MOUNTING section in APPLICATION HINTS for more information.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating(3)	2 kV
Power Dissipation(4)	Internally Limited
V(max) All pins (with respect to GND)	-0.3V to 12V
I_{OUT}(5)	Internally Limited
Junction Temperature	−40°C to +150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) ESD is tested using the human body model which is a 100pF capacitor discharged through a 1.5k resistor into each pin.

(4) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink values (if a heatsink is used). The junction-to-ambient thermal resistance ($\theta_{J\text{-}A}$) for the PFM is approximately 90°C/W for a PC board mounting with the device soldered down to minimum copper area (less than 0.1 square inch). If one square inch of copper is used as a heat dissipator for the PFM, the $\theta_{J\text{-}A}$ drops to approximately 50°C/W. The SOT-223 package has a $\theta_{J\text{-}A}$ of approximately 125°C/W when soldered down to a minimum sized pattern (less than 0.1 square inch) and approximately 70°C/W when soldered to a copper area of one square inch. The $\theta_{J\text{-}A}$ values for the WSON package are also dependent on trace area, copper thickness, and the number of thermal vias used (refer to the TI (AN-1187 Application Report) and the WSON MOUNTING section in this datasheet). If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

OPERATING RATINGS

V_{IN} Supply Voltage	2.7V to 10V
Operating Junction Temperature Range	−40°C to +125°C

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for $T_J = 25°C$, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{OUT} + 1V$, $C_{IN} = C_{OUT} = 10\ \mu F$, $I_{LOAD} = 10mA$. Min/Max limits are specified through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
V_O	Output Voltage Tolerance		-2.0		2.0	$\%V_{OUT}$
		$100\ \mu A < I_L < 0.5A$ $V_O + 1V \le V_{IN} \le 10V$	**-4.0**		**4.0**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation(2)	$V_O + 0.5V \le V_{IN} \le 10V$ $I_L = 25mA$		0.03	**0.1**	%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation(3)	$1\ mA < I_L < 0.5A$ $V_{IN} = V_O + 1V$		1.8	**5**	%/A
$V_{IN} - V_{OUT}$	Dropout Voltage(4)	$(V_O = 2.5V)$ $I_L = 0.1A$ $I_L = 0.5A$		80 430	**145** **725**	mV
		$(V_O = 3.3V)$ $I_L = 0.1A$ $I_L = 0.5A$		65 330	**110** **550**	
		$(V_O = 5V)$ $I_L = 0.1A$ $I_L = 0.5A$		45 250	**100** **450**	
I_Q	Quiescent Current	$V_{IN} \le 10V$, $I_L = 100\ \mu A - 0.5A$		55	**100**	µA
		$V_{EN} \le 0.4V$, (LP38693 Only)		0.001	1	
$I_L(MIN)$	Minimum Load Current	$V_{IN} - V_O \le 4V$			**100**	
I_{FB}	Foldback Current Limit	$V_{IN} - V_O > 5V$		350		mA
		$V_{IN} - V_O < 4V$		850		
PSRR	Ripple Rejection	$V_{IN} = V_O + 2V(DC)$, with 1V(p-p) / 120Hz Ripple		55		dB
T_{SD}	Thermal Shutdown Activation (Junction Temp)			160		°C
T_{SD} (HYST)	Thermal Shutdown Hysteresis (Junction Temp)			10		
e_n	Output Noise	BW = 10Hz to 10kHz $V_O = 3.3V$		0.7		$\mu V/\sqrt{Hz}$
V_O (LEAK)	Output Leakage Current	$V_O = V_O(NOM) + 1V$ @ $10V_{IN}$		0.5	12	µA
V_{EN}	Enable Voltage (LP38693 Only)	Output = OFF			**0.4**	V
		Output = ON, $V_{IN} = 4V$	**1.8**			
		Output = ON, $V_{IN} = 6V$	**3.0**			
		Output = ON, $V_{IN} = 10V$	**4.0**			
I_{EN}	Enable Pin Leakage (LP38693 Only)	$V_{EN} = 0V$ or $10V$, $V_{IN} = 10V$	-1	0.001	1	µA

(1) Typical numbers represent the most likely parametric norm for 25°C operation.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from 1mA to full load.
(4) Dropout voltage is defined as the minimum input to output differential required to maintain the output within 100mV of nominal value.

BLOCK DIAGRAMS

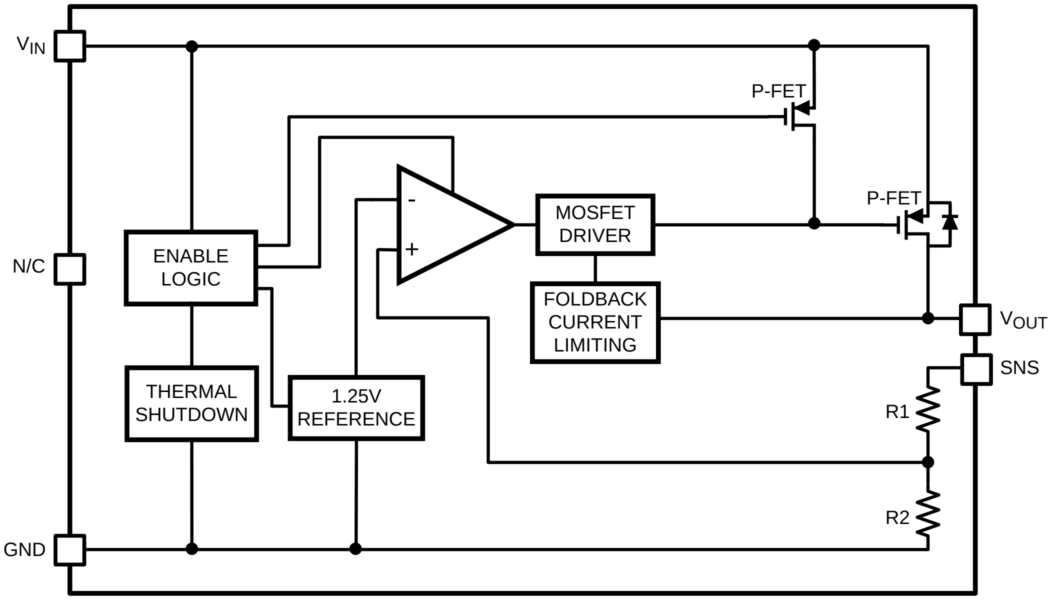


Figure 5. LP38691 Functional Diagram (WSON)

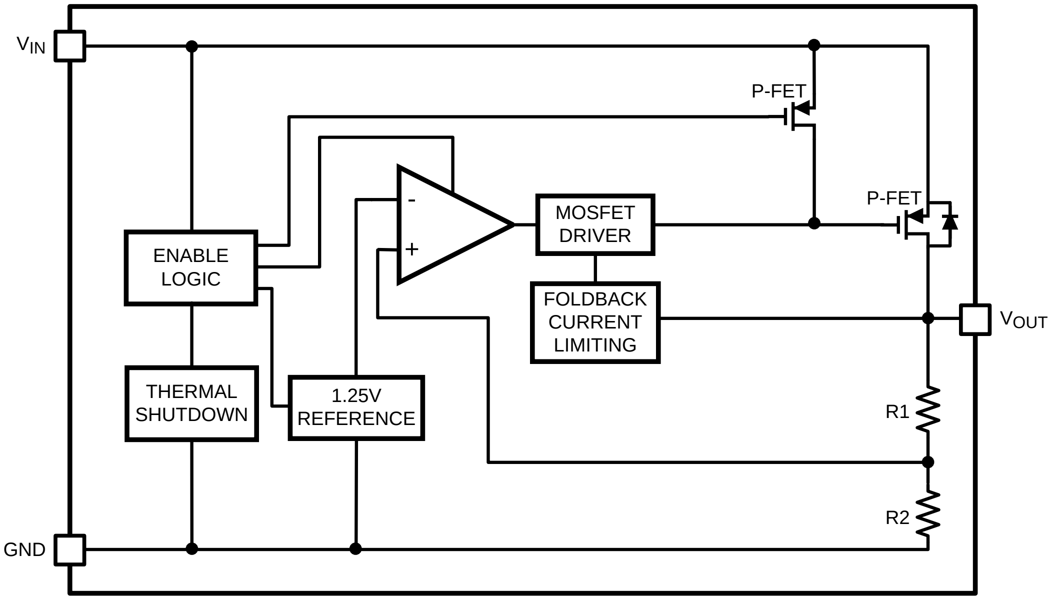


Figure 6. LP38691 Functional Diagram (PFM)

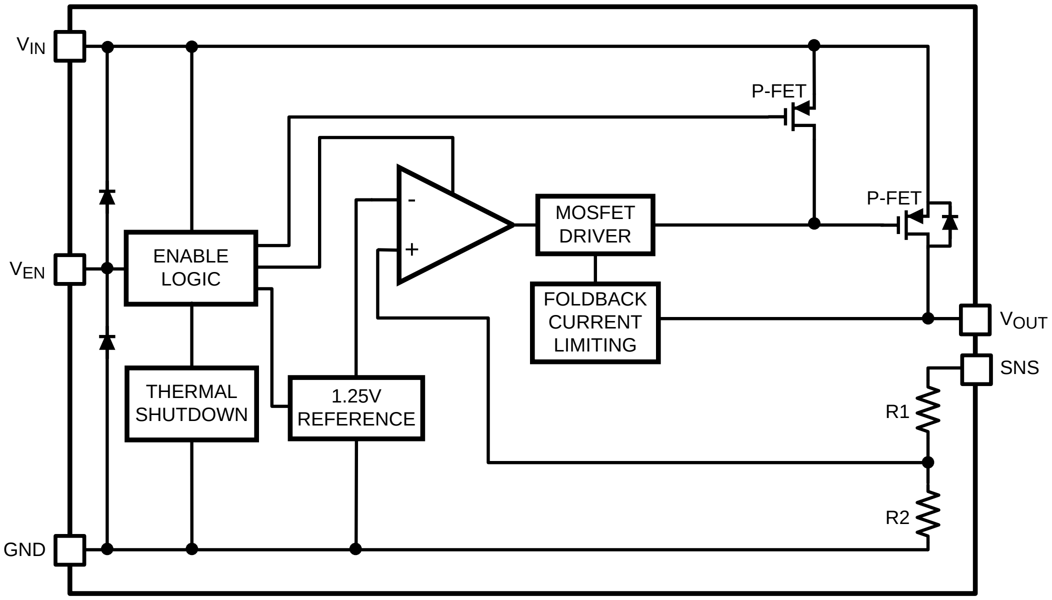


Figure 7. LP38693 Functional Diagram (WSON)

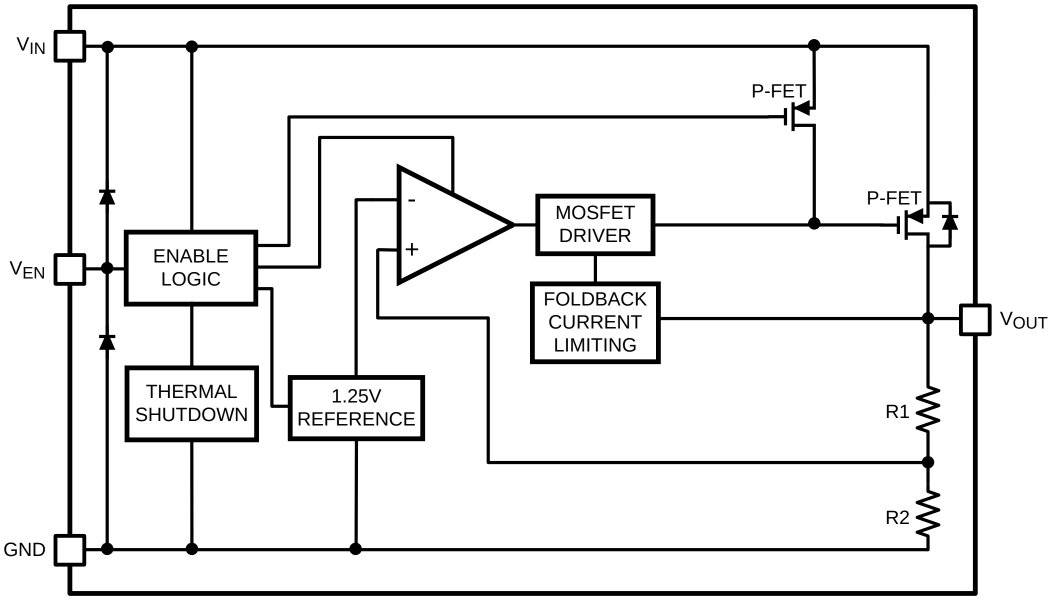


Figure 8. LP38693 Functional Diagram (SOT-223)

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, Enable pin is tied to V_{IN} (LP38693 only), V_{OUT} = 1.8V, V_{IN} = V_{OUT} +1V, I_L = 10mA.

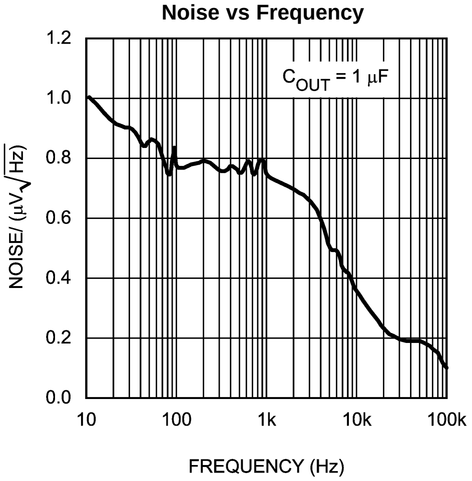
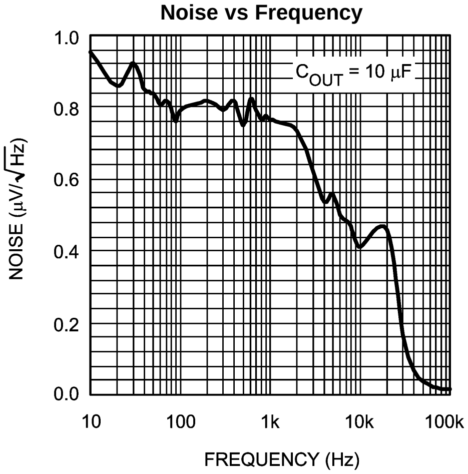


Figure 9.



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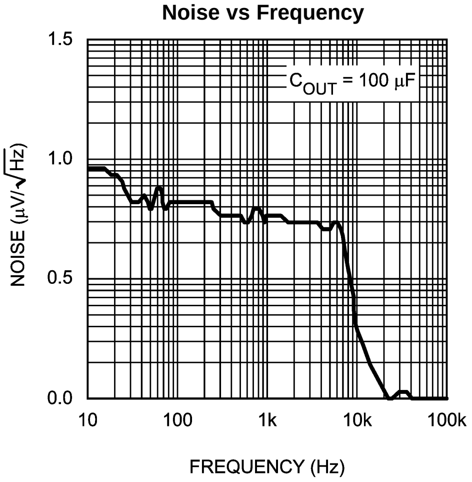

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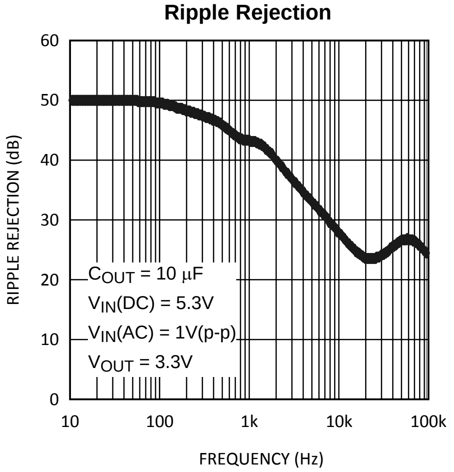

Figure 12.

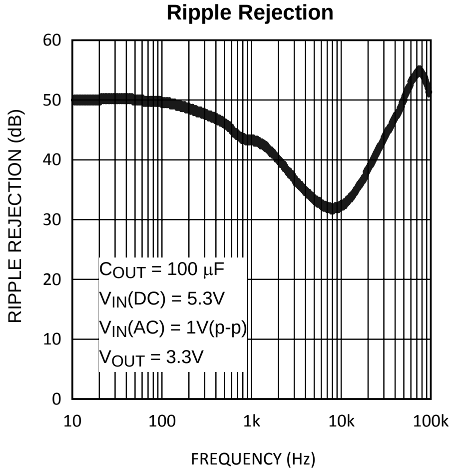

Figure 13.

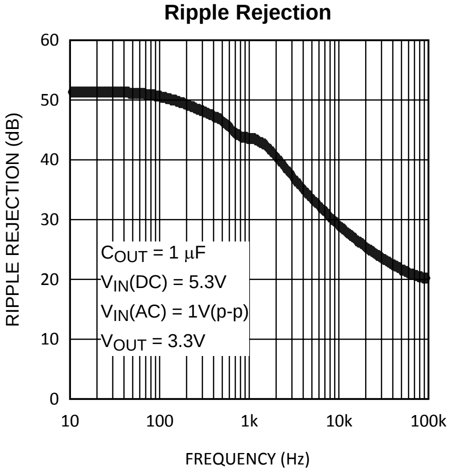

Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, $C_{IN} = C_{OUT}$ = 10 µF, Enable pin is tied to V_{IN} (LP38693 only), V_{OUT} = 1.8V, $V_{IN} = V_{OUT}$ +1V, I_L = 10mA.

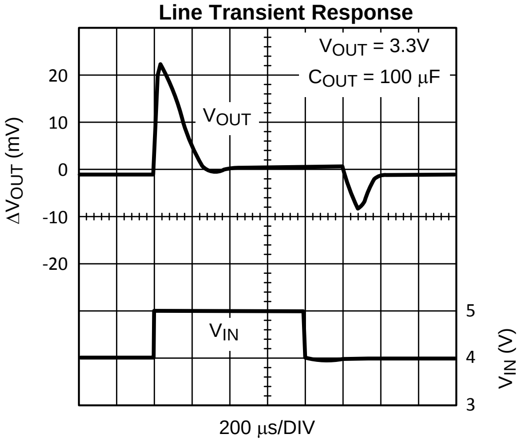

Figure 15.

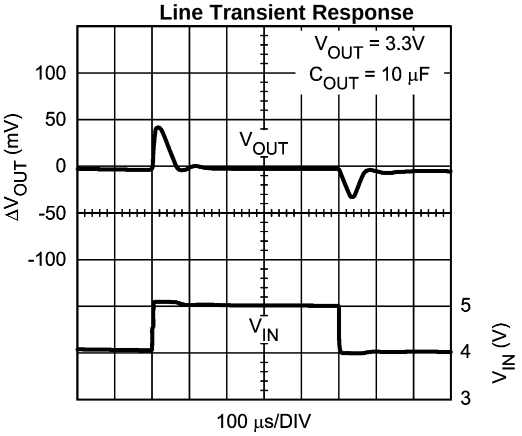

Figure 16.

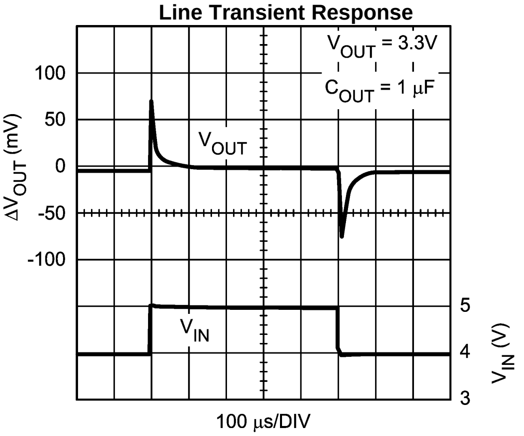

Figure 17.

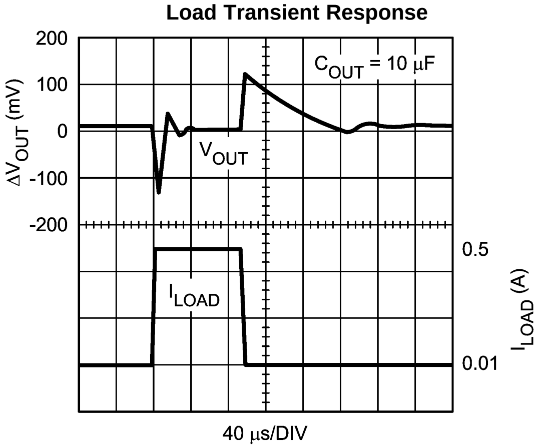

Figure 18.

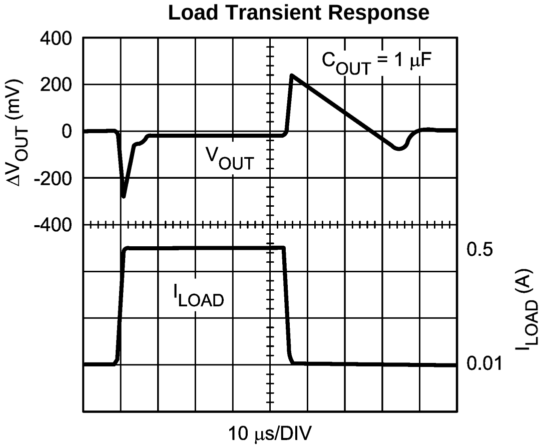

Figure 19.

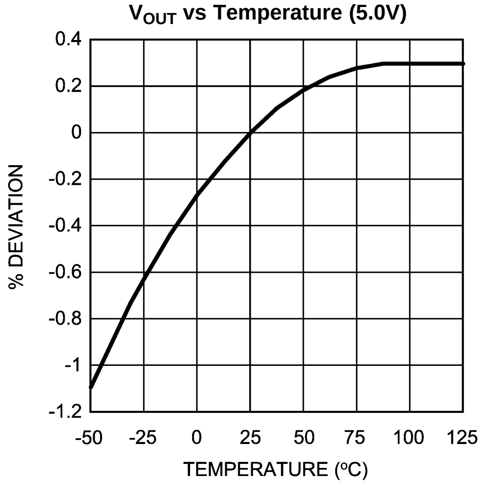

Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, Enable pin is tied to V_{IN} (LP38693 only), V_{OUT} = 1.8V, V_{IN} = V_{OUT} +1V, I_L = 10mA.

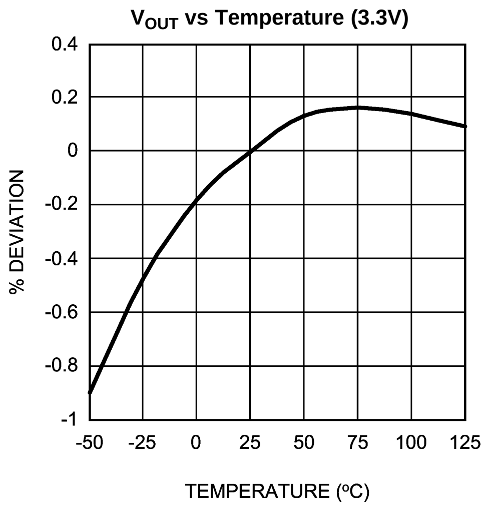
V_{OUT} vs Temperature (3.3V)

Figure 21.

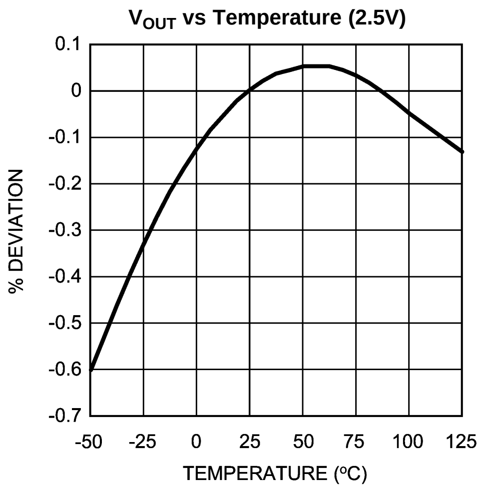
V_{OUT} vs Temperature (2.5V)

Figure 22.

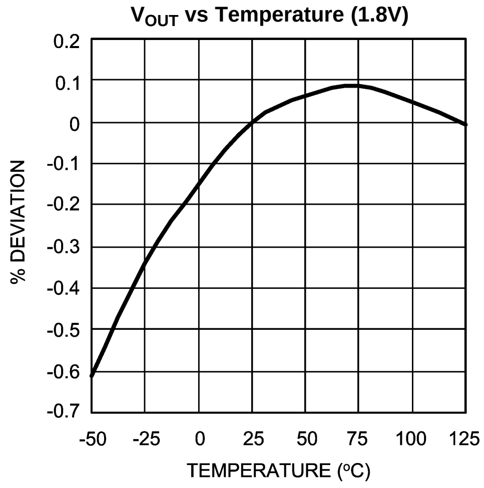
V_{OUT} vs Temperature (1.8V)

Figure 23.

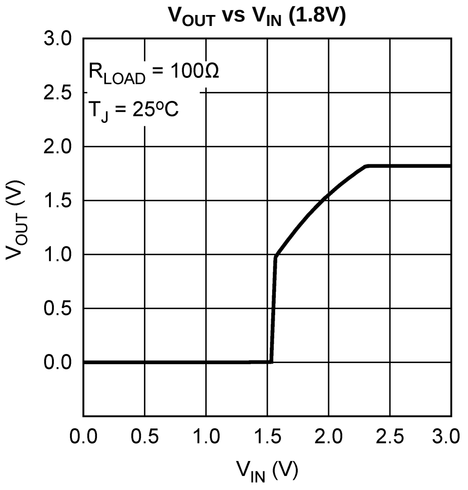
V_{OUT} vs V_{IN} (1.8V)

Figure 24.

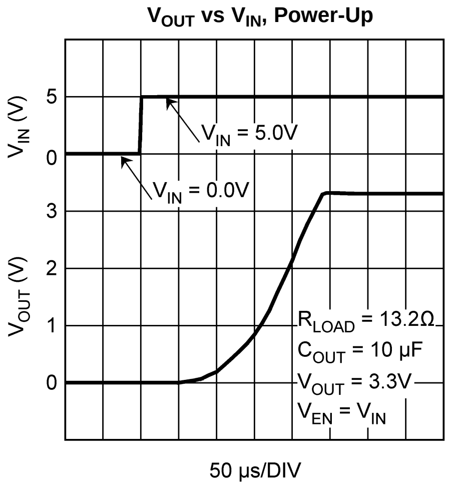
V_{OUT} vs V_{IN}, Power-Up

Figure 25.

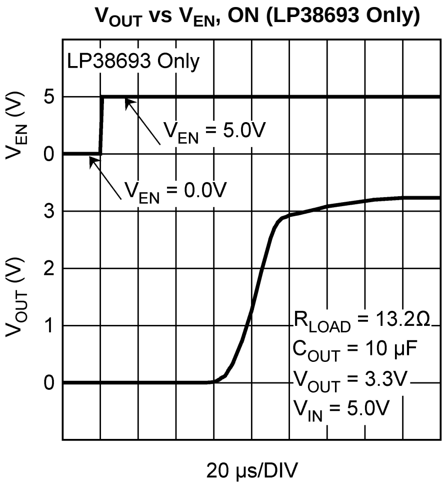
V_{OUT} vs V_{EN}, ON (LP38693 Only)

Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J = 25°C$, $C_{IN} = C_{OUT} = 10\ \mu F$, Enable pin is tied to V_{IN} (LP38693 only), $V_{OUT} = 1.8V$, $V_{IN} = V_{OUT} +1V$, $I_L = 10mA$.

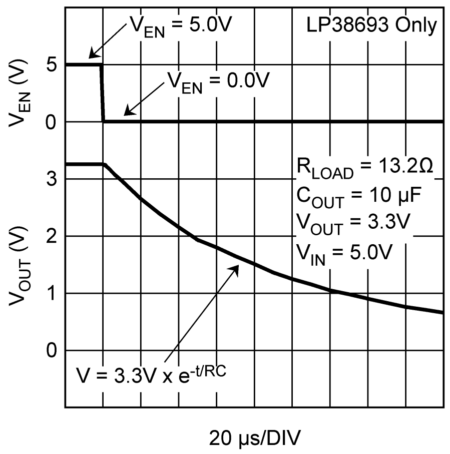
V_{OUT} vs V_{EN}, OFF (LP38693 Only)

Figure 27.

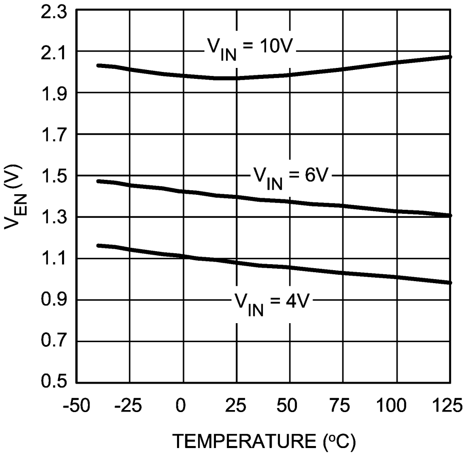
Enable Voltage vs Temperature

Figure 28.

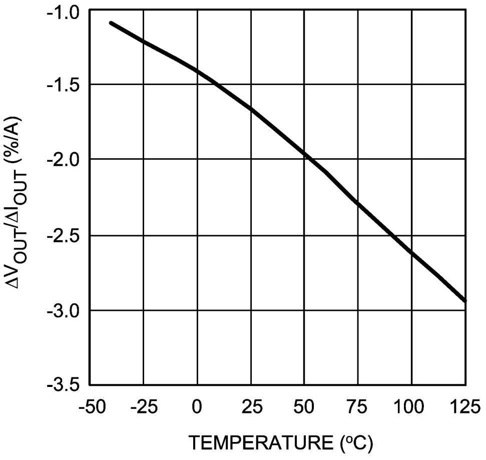
Load Regulation vs Temperature

Figure 29.

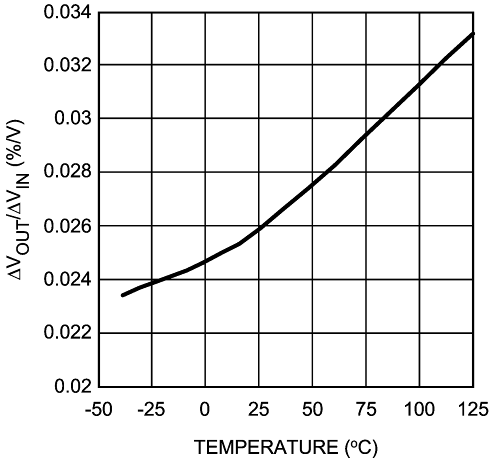
Line Regulation vs Temperature

Figure 30.

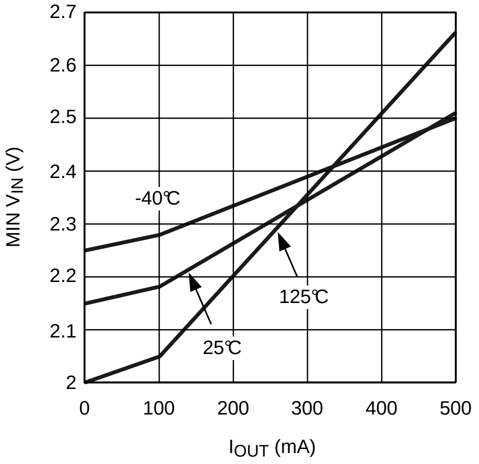
MIN V_{IN} vs I_{OUT}

Figure 31.

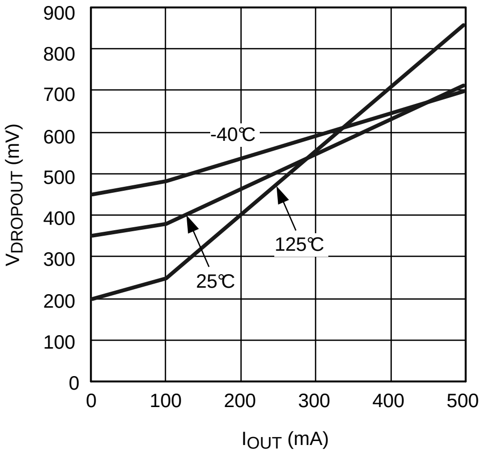
Dropout Voltage vs I_{OUT}

Figure 32.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR:

An input capacitor of at least 1µF is required (ceramic recommended). The capacitor must be located not more than one centimeter from the input pin and returned to a clean analog ground.

OUTPUT CAPACITOR:

An output capacitor is required for loop stability. It must be located less than 1 centimeter from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them.

The minimum amount of output capacitance that can be used for stable operation is 1µF. Ceramic capacitors are recommended (the LP38691/3 was designed for use with ultra low ESR capacitors). The LP38691/3 is stable with any output capacitor ESR between zero and 100 Ohms.

ENABLE PIN (LP38693 only):

The LP38693 has an Enable pin (EN) which allows an external control signal to turn the regulator output On and Off. The Enable On/Off threshold has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through the ON and OFF voltage thresholds. The Enable pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively. If the Enable pin is driven from a source that actively pulls high and low, the drive voltage should not be allowed to go below ground potential or higher than V_{IN}. If the application does not require the Enable function, the pin should be connected directly to the V_{IN} pin.

Foldback Current Limiting:

Foldback current limiting is built into the LP38691/3 which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between V_{IN} and V_{OUT}. Typically, when this differential voltage exceeds 5V, the load current will limit at about 350 mA. When the V_{IN} - V_{OUT} differential is reduced below 4V, load current is limited to about 850 mA.

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range.

Capacitor Characteristics

CERAMIC

For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM

Solid Tantalum capacitors have good temperature stability: a high quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of -40°C to +125°C. ESR will vary only about 2X going from the high to low temperature limits.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

1. While V_{IN} is high enough to keep the control circuity alive, and the Enable pin (LP38693 only) is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. If the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full ON condition. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the Enable pin is low this condition will be prevented.
2. The internal PFET pass element has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, when V_{IN} is below the value where the control circuity is alive, or the Enable pin is low (LP38693 only), and the output voltage is more than 500 mV (typical) above the input voltage the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

   If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground to limit the negative voltage transition. A Schottky diode is recommended for this protective clamp.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it’s capacitors fixed the problem. Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

WSON MOUNTING

The NGG0006A (No Pullback) 6-Lead WSON package requires specific mounting techniques which are detailed in the TI AN-1187 Application Report. Referring to the section PCB Design Recommendations (Page 5), it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The input current is split between two V_{IN} pins, 1 and 6. The two V_{IN} pins must be connected together to ensure that the device can meet all specifications at the rated current.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 2 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP38691SD and LP38693SD in the NGG0006A 6-Lead WSON package, the junction-to-case thermal rating, θJC, is 10.4°C/W, where the case is the bottom of the package at the center of the DAP. The junction-to-ambient thermal performance for the LP38691SD and LP38693SD in the NGG0006A 6-Lead WSON package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	**Thermal Vias**	θ_{JC}	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	10.4°C/W	237° C/W
JEDEC 4-Layer JESD 51-7	1	10.4°C/W	74° C/W
	2	10.4°C/W	60° C/W
	4	10.4°C/W	49° C/W
	6	10.4°C/W	45° C/W

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/ EMI can cause ground bounce across the ground plane. In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways: **Spot Noise** or **Output Noise Density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency. **Total Output Noise** or **Broad-Band Noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/root-Hz or nV/root-Hz and total output noise is measured in µV(rms)

The primary source of noise in low-dropout regulators is the internal reference. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current).

REVISION HISTORY

Changes from Revision J (April 2013) to Revision K	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38691DT-1.8	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LP38691 DT-1.8	
LP38691DT-1.8/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-1.8	Samples
LP38691DT-2.5	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LP38691 DT-2.5	
LP38691DT-2.5/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-2.5	Samples
LP38691DT-3.3	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LP38691 DT-3.3	
LP38691DT-3.3/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-3.3	Samples
LP38691DT-5.0	ACTIVE	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125		Samples
LP38691DT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-5.0	Samples
LP38691DTX-1.8	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125		Samples
LP38691DTX-1.8/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-1.8	Samples
LP38691DTX-2.5	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125		Samples
LP38691DTX-2.5/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-2.5	Samples
LP38691DTX-3.3	NRND	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125	LP38691 DT-3.3	
LP38691DTX-3.3/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-3.3	Samples
LP38691DTX-5.0	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125		Samples
LP38691DTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38691 DT-5.0	Samples
LP38691QSD-1.8/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L256B	Samples
LP38691QSD-2.5/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L257B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38691QSD-3.3/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L258B	Samples
LP38691QSD-5.0/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L259B	Samples
LP38691QSDX-1.8/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L256B	Samples
LP38691QSDX-2.5/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L257B	Samples
LP38691QSDX-3.3/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L258B	Samples
LP38691QSDX-5.0/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L259B	Samples
LP38691SD-1.8	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L118B	
LP38691SD-1.8/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L118B	Samples
LP38691SD-2.5/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L119B	Samples
LP38691SD-3.3/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L120B	Samples
LP38691SD-5.0/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L121B	Samples
LP38691SDX-1.8/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L118B	Samples
LP38691SDX-2.5/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L119B	Samples
LP38691SDX-3.3/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L120B	Samples
LP38691SDX-5.0/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L121B	Samples
LP38693MP-1.8	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LJVB	
LP38693MP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJVB	Samples
LP38693MP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJXB	Samples
LP38693MP-3.3	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LJYB	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38693MP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJYB	Samples
LP38693MP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJZB	Samples
LP38693MPX-1.8/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJVB	Samples
LP38693MPX-2.5/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJXB	Samples
LP38693MPX-3.3	NRND	SOT-223	NDC	5	2000	TBD	Call TI	Call TI	-40 to 125	LJYB	
LP38693MPX-3.3/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJYB	Samples
LP38693MPX-5.0/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJZB	Samples
LP38693QSD-1.8/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L260B	Samples
LP38693QSD-2.5/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L261B	Samples
LP38693QSD-3.3/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L262B	Samples
LP38693QSD-5.0/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L263B	Samples
LP38693QSDX-1.8/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L260B	Samples
LP38693QSDX-2.5/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L261B	Samples
LP38693QSDX-3.3/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L262B	Samples
LP38693QSDX-5.0/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L263B	Samples
LP38693SD-1.8	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L128B	
LP38693SD-1.8/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L128B	Samples
LP38693SD-2.5/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L129B	Samples
LP38693SD-3.3	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L130B	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38693SD-3.3/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L130B	Samples
LP38693SD-5.0	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L131B	
LP38693SD-5.0/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L131B	Samples
LP38693SDX-1.8/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L128B	Samples
LP38693SDX-2.5/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L129B	Samples
LP38693SDX-3.3/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	L130B	Samples
LP38693SDX-5.0/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L131B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LP38691, LP38691-Q1, LP38693, LP38693-Q1 :

- Catalog: LP38691, LP38693

- Automotive: LP38691-Q1, LP38693-Q1

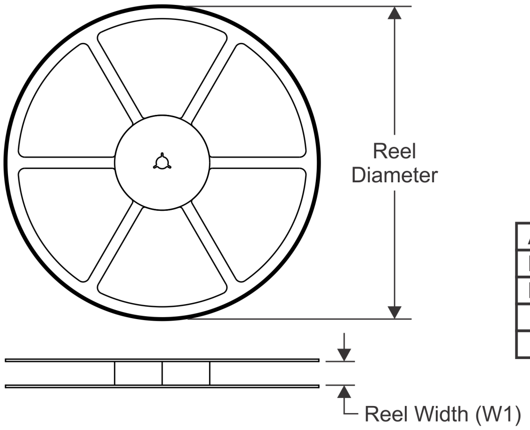
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

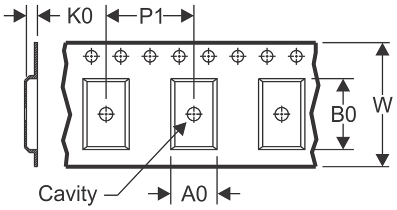
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

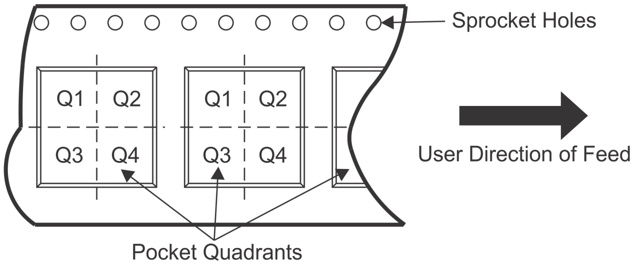


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

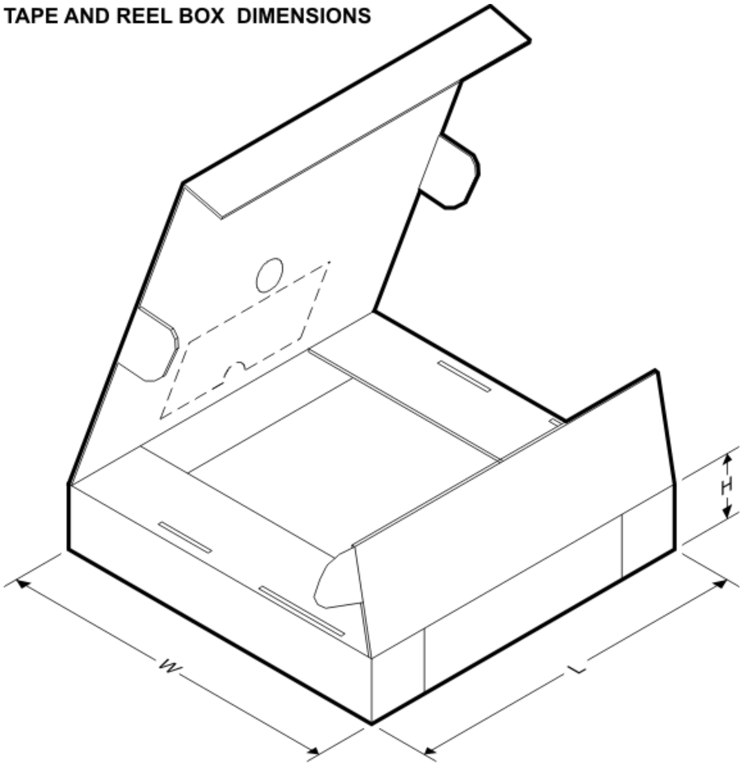


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38691DTX-1.8/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38691DTX-2.5/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38691DTX-3.3	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38691DTX-3.3/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38691DTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38691QSD-1.8/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSD-2.5/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSD-3.3/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSD-5.0/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSDX-1.8/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSDX-2.5/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSDX-3.3/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691QSDX-5.0/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-1.8	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-1.8/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-2.5/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-3.3/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SD-5.0/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38691SDX-1.8/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SDX-2.5/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SDX-3.3/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38691SDX-5.0/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693MP-1.8	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MP-3.3	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MP-5.0/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-1.8/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-2.5/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-3.3	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-3.3/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693MPX-5.0/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38693QSD-1.8/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSD-2.5/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSD-3.3/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSD-5.0/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSDX-1.8/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSDX-2.5/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSDX-3.3/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693QSDX-5.0/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-1.8	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-1.8/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-2.5/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-3.3	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-3.3/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-5.0	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SD-5.0/NOPB	WSON	NGG	6	1000	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SDX-1.8/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SDX-2.5/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SDX-3.3/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38693SDX-5.0/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

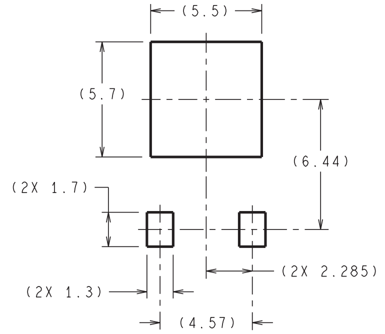


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38691DTX-1.8/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38691DTX-2.5/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38691DTX-3.3	TO-252	NDP	3	2500	367.0	367.0	35.0
LP38691DTX-3.3/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38691DTX-5.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38691QSD-1.8/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38691QSD-2.5/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38691QSD-3.3/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38691QSD-5.0/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38691QSDX-1.8/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38691QSDX-2.5/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38691QSDX-3.3/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38691QSDX-5.0/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38691SD-1.8	WSON	NGG	6	1000	210.0	185.0	35.0
LP38691SD-1.8/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38691SD-2.5/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38691SD-3.3/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38691SD-5.0/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38691SDX-1.8/NOPB	WSON	NGG	6	4500	346.0	346.0	35.0
LP38691SDX-2.5/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

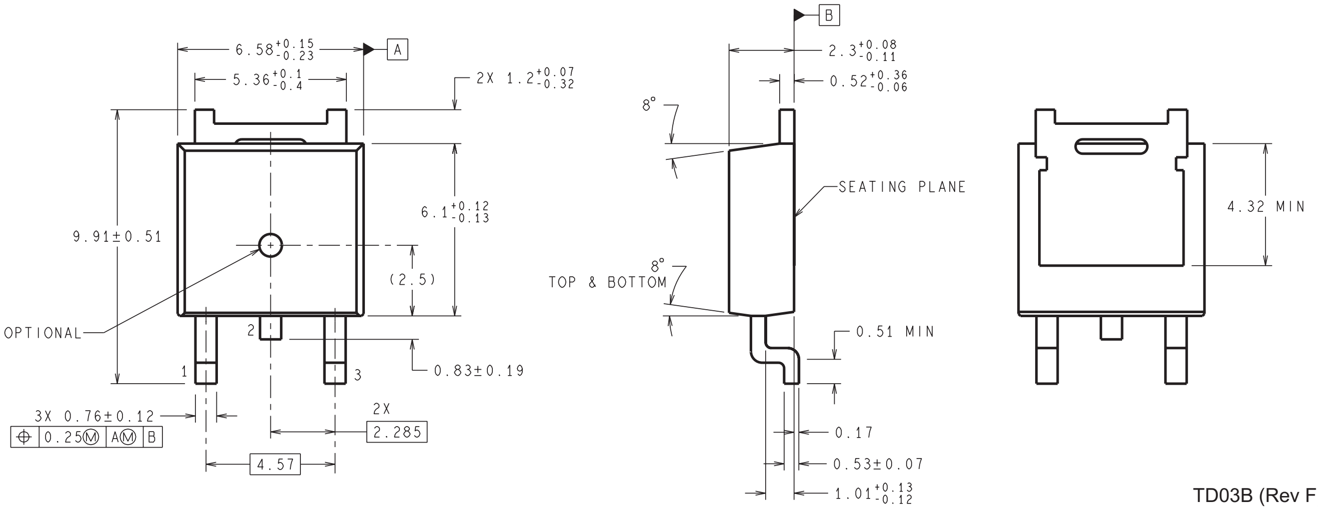
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38691SDX-3.3/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38691SDX-5.0/NOPB	WSON	NGG	6	4500	346.0	346.0	35.0
LP38693MP-1.8	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38693MP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38693MP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38693MP-3.3	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38693MP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38693MP-5.0/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38693MPX-1.8/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38693MPX-2.5/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38693MPX-3.3	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38693MPX-3.3/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38693MPX-5.0/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38693QSD-1.8/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693QSD-2.5/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693QSD-3.3/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693QSD-5.0/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693QSDX-1.8/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693QSDX-2.5/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693QSDX-3.3/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693QSDX-5.0/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693SD-1.8	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693SD-1.8/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38693SD-2.5/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693SD-3.3	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693SD-3.3/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38693SD-5.0	WSON	NGG	6	1000	210.0	185.0	35.0
LP38693SD-5.0/NOPB	WSON	NGG	6	1000	203.0	203.0	35.0
LP38693SDX-1.8/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693SDX-2.5/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38693SDX-3.3/NOPB	WSON	NGG	6	4500	346.0	346.0	35.0
LP38693SDX-5.0/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

NDP0003B

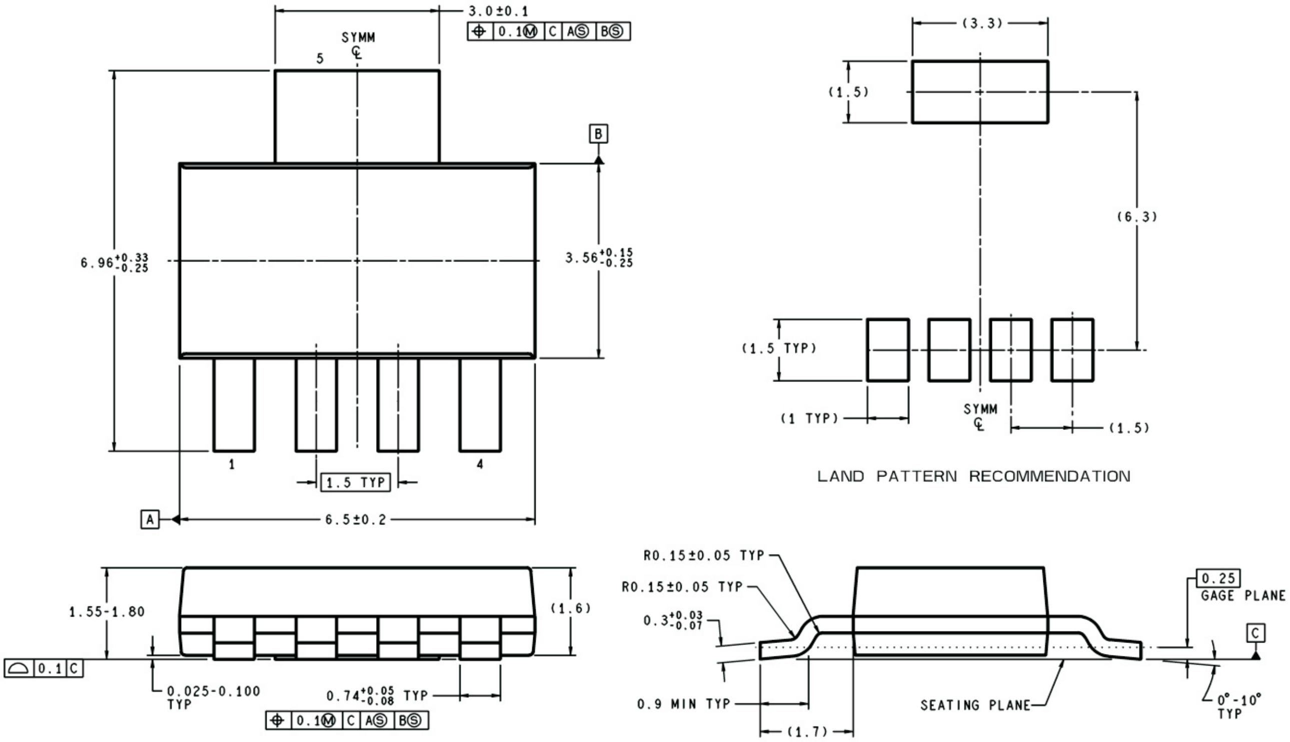


LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



TD03B (Rev F)



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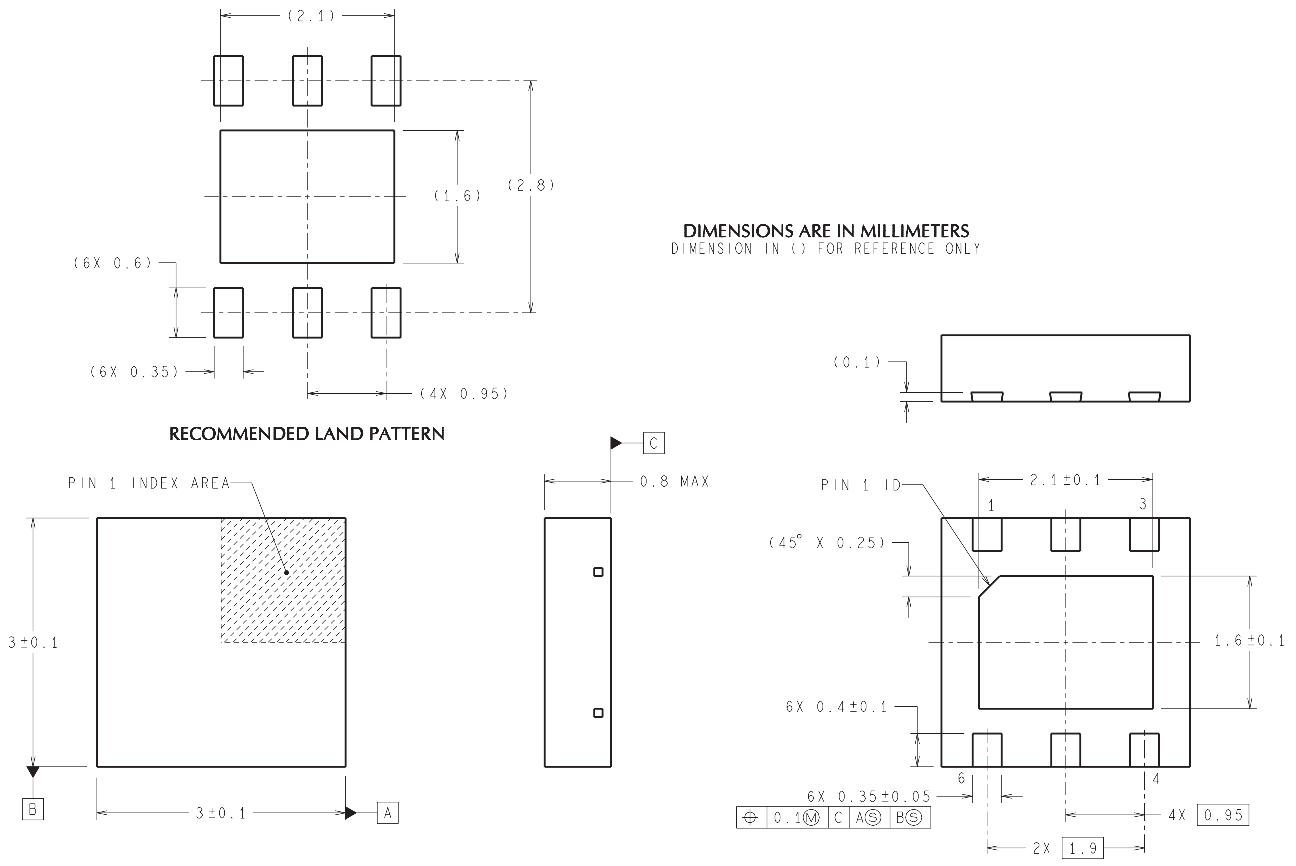
MP05A (Rev A)


(2.1)
(1.6)
(2.8)
(6X 0.6)
(6X 0.35)
(4X 0.95)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN () FOR REFERENCE ONLY
(0.1)
C
0.8 MAX
PIN 1 INDEX AREA
3±0.1
B
3±0.1
A
PIN 1 ID
2.1±0.1
1
3
(45° X 0.25)
1.6±0.1
6X 0.4±0.1
6
4
6X 0.35±0.05
⊕ 0.1Ⓜ C AⓈ BⓈ
4X 0.95
2X 1.9

SDE06A (Rev A)

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