TMS320C5515 Evaluation Module (EVM)

Technical Reference

2010 ***DSP Development Systems***

2.5.1 C5515 EVM Option Jumpers

The C5515 EVM's option jumpers fall into two categories; user selectable, and factory installed. The table below shows lists the user option jumpers and their function.

Table 18: C5515 EVM User Option Jumpers

Jumper #/ Schematic Page	Nomenclature	# of Positions	Setting	Function
JP2 / 12	nRESET Select	3	1 - 2 *	Use RESET from TPS65023
			2 - 3	Use RESET from SW1
JP3 / 17	UART_EN	2	Shorted *	UART transceiver enabled
			Open	UART transceiver disabled
JP5 / 2	WK_PU_PD_SEL	3	1 - 2	WAKEUP pin uses pull up
			2 - 3 *	WAKEUP pin uses pull down
JP6 / 10	LDO_EN	2	Shorted *	Enable internal DSP LDO
			Open	Disable internal DSP LDO
JP9 / 3	CLK_SEL	2	Shorted	CLK_SEL tied to VDD_IO1
			Open *	CLK_SEL tied to GND
JP12 / 10	MIC_BIAS	3	1 - 2	Use 3.3V
			2 - 3 *	Use AIC output
JP39 / 13	VIN Select	3	1 - 2	Power is from battery
			2 - 3 *	Power is from external 5v supply

* Factory default

The factory installed jumpers are pre-configured with a zero (0) ohm resistor at the factory and are **not** meant to be changed by users. These jumpers are not populated with a jumper header. The table below lists the factory installed option jumpers and their function.

Table 19: C5515 EVM Factory Installed Power Domain Configuration

Jumper #/ Schematic Page	Nomenclature	# of Positions	Setting	Function
JP1 / 11	CPU VDDC Select	3	1 - 2 ***+**	Internal DSP-LDO used
			2 - 3	DSP will use external 1.3 volt
JP4 / 3	RTC	3	1 - 2 *****	CVDDRTC tied to V1.3
			2 - 3	Do Not Use
JP11 / 10	LDOI Select	3	1 - 2 *	LDO_IN tied to V1.8
			2 - 3	LDO_IN tied to V3.3
JP15 / 11	USB_VDD_IN Select	3	1 - 2 ***z**	DSP will use internal USB LDO
			2 - 3	DSP will use external 1.3V
JP16 / 10	VDDA_ANA Select	3	1 - 2 *****	Internal Analog-LDO used
			2 - 3	DSP will use external 1.3V
JP18 / 10	VDDA_PLL Select	3	1 - 2 *	Internal Analog-LDO used
			2 - 3	DSP will use external 1.3V

* Default
\+ JP6 must be installed
Z USB LDO must be enabled in software

2.5.1.1 JP2, nRESET Source Select

Jumper JP2 is a three position jumper that allows the user to the select the source of the nRESET signal to the C5515 processor. This jumper is pre-configured at the factory with a jumper in the 2-3 position (*****).The table below shows the positions and their function.

Table 20: JP2, nRESET Source Select

Jumper Position	Function
1-2 *	PWR_RSTn is the source of the nRESET signal to the C5515 Processor
2-3	SW1 is the source of the nRESET signal to the C5515 Processor

Shown below is a top view of the JP2.

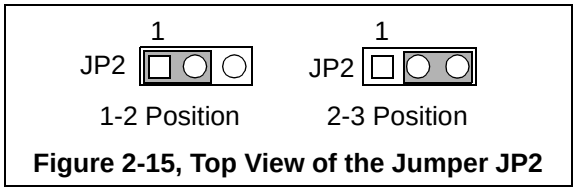

Figure 2-15, Top View of the Jumper JP2

2.5.1.2 JP3, UART_EN Select

Jumper JP3 is a two position populated jumper that enables/disables the UART driver on the EVM. This jumper is pre-configured at the factory with a jumper in place (*****). The table below shows the positions and their function.

Table 21: JP3, UART Enable Jumper

Jumper Position	Function
Open	$\overline{\text{EN_L}}$ pulled to GND thereby disabling the MAX3222 line driver
Shorted *	$\overline{\text{EN_L}}$ pulled to +3.3 thereby enabling the MAX3222 line driver

Shown below is a top view of the JP3.

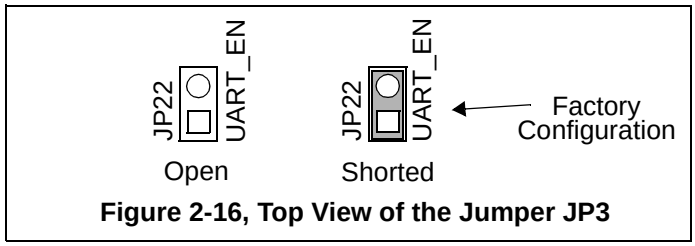

Figure 2-16, Top View of the Jumper JP3

2.5.1.3 JP5, WAKEUP Source Select

Jumper JP5 is a three position jumper that allows the user to the select the a pull up or pull down WAKEUP signal to the C5515 processor (U13-E8). This jumper is pre-configured at the factory with a jumper in the 2-3 position (*****). The 1-2 position allows the switch, SW2, to wake up the processor. The table below shows the positions and their function.

Table 22: JP5, WAKEUP Source Select

Jumper Position	Function
1-2	Depressing switch SW2 wakes up the C5515 Processor (uses pull up)
2-3 *	WAKEUP pin uses Pull Down

Shown below is a top view of the JP5.

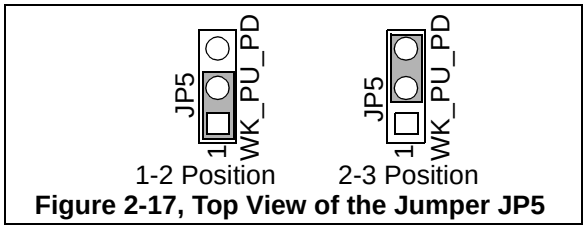

Figure 2-17, Top View of the Jumper JP5

2.5.1.4 JP6, LDO_EN Source Select

Jumper JP6 is a two position jumper located on the top side of the circuit board that selects the level of the LDO_EN signal. When the jumper is shorted, LDO_EN is pulled to GND enabling on-chip LDO's. If the jumper is open, LDO_EN is pulled high disabling on-chip LDO's. This jumper **must** be installed. The table below shows the positions and their function.

Table 23: JP6, LDO_EN Select

Jumper Position	Function
Open	LDO_EN, is pulled high, LDO's enabled
Shorted *	LDO_EN is low, the internal LDO is enabled

* Default

Shown below is a top view of the JP6.

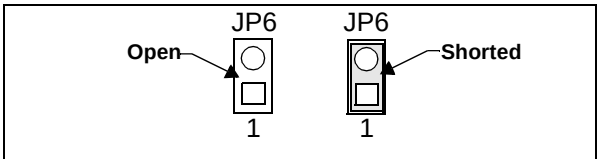

Figure 2-18, Top View of the Jumper JP6

2.5.1.5 JP9, CLK_SEL Source Select

Jumper JP9 is a two position jumper that determines if the DSP uses an external or internal oscillator. The shorted state allows an external oscillator to be used when an oscillator is populated in the 8 pin OSC1 socket. An open jumper means the DSP will use an internal oscillator. The jumper is pre-configured at the factory in the open state. The table below shows the positions and their function.

Table 24: JP9, CLK_SEL Select

Jumper Position	Function
Open *	Use internal oscillator for DSP clock
Shorted	Use external oscillator for DSP clock

* Default

Shown below is a top view of the JP9.

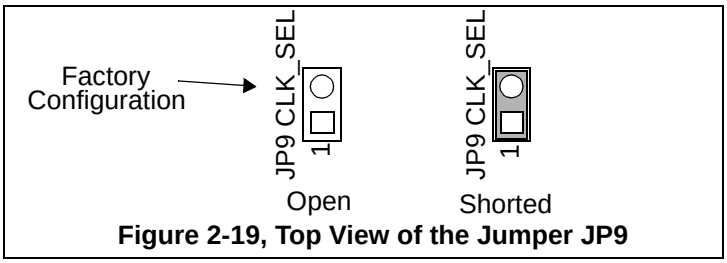

Figure 2-19, Top View of the Jumper JP9

2.5.1.6 JP12, MIC_BIAS Source Select

Jumper JP12 is a three position populated jumper that selects the source of the microphone bias used for AIC MIC1L and AIC MIC1R on the TLV320AIC3204. The table below shows the positions and their function.

Table 25: JP12, Microphone Bias Select

Jumper Position	Function
1-2	When R209 is installed bias is 3.3 volts
2-3 *	Bias from TLV320AIC3204 MICBIAS pin

* Default

Shown below is a top view of the JP12.

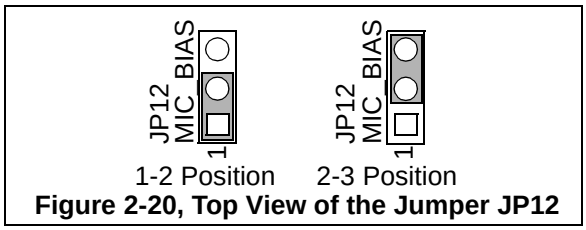

Figure 2-20, Top View of the Jumper JP12

2.5.1.7 JP39, VIN Source Select

Jumper JP39 is a three position populated jumper located on the top side of the circuit board that selects the source of the incoming +5 volts. The table below shows the positions and their function.

Table 26: JP39, VIN Source Select

Jumper Position	Function
1 - 2	Battery is selected as source for +5 volts input
2 - 3 *	External power supply is selected as source for +5 volts input, J16

* default

Shown below is a top view of the JP39 with silkscreen markings.

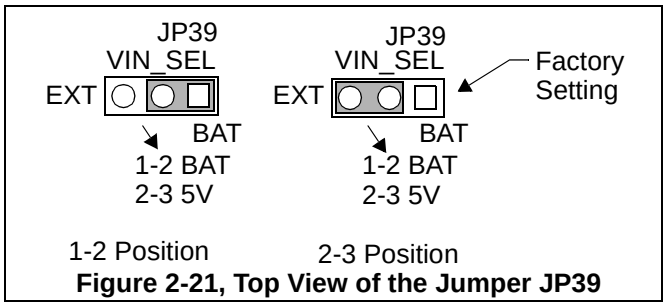

Figure 2-21, Top View of the Jumper JP39

2.5.2 C5515 EVM Power Domain Probe Points

The C5515 EVM has pre-designed probe points in the circuitry which could be used to observe power domains. Several of the power domains have INA219 power monitors and these domains have a 1 ohm resistor shunted on the EVM. The probe points with power monitors are shown in the table below.

Table 27: C5515 EVM Power Probe Points With Power Monitors

Jumper #/ Schematic Page	Signal	# of Positions	1 Ohm Shunt Resistor Installed at factory
JP8 / 11	TPS65023_VCC_1V8	2	Monitor
JP17 / 11	C5515 VDD_IO1	2	Monitor
JP20 / 15	V1.8	2	Monitor
JP22 / 13	VIN_EVM	2	Monitor
JP23 / 15	VDD_IO2	2	Monitor - 0
JP25 / 15	V3.3	2	Monitor
JP37 / 11	VDDC	2	Monitor
JP38 / 11	USB_VDD_IN	2	Monitor

Shown below is a diagram of a typical Power Domain Probe Point with a one (1) ohm resistor.

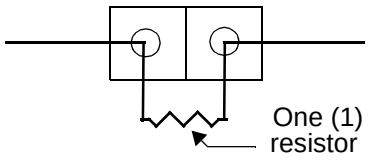

Figure 2-22, Diagram of a typical jumper

The remaining pre-configured power probe points are shunted with zero (0) ohm resistors as shown below.

Table 28: C5515 EVM Power Probe Points With 0 Ohm Resistors

Jumper #/ Schematic Page	Signal	# of Positions	0 Ohm Shunt Resistor Installed at factory
JP7 / 19	AIC HPVDD	2	Yes
JP13 / 2	C5515 VDDIO4	2	Yes
JP14 / 19	AIC IOVDD	2	Yes
JP19 / 10	USB_VDDA3P3	2	Yes
JP21 / 15	V1.3	2	Yes
JP24 / 15	VDD_IO1	2	Yes
JP26 / 15	CPU_VCC_CORE	2	Yes
JP40 / 19	AIC AVDD	2	Yes

Shown below is a diagram of a typical Power Domain Probe Point with a zero (0) ohm resistor.

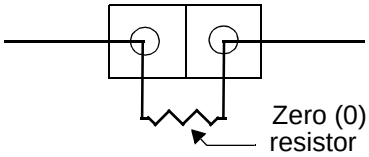

Figure 2-23, Diagram of a typical jumper

2.6 Test Points

The C5515 EVM has forty-one (41) test points. The position of these test points on the top side of the C5515 EVM are shown in the figures below.

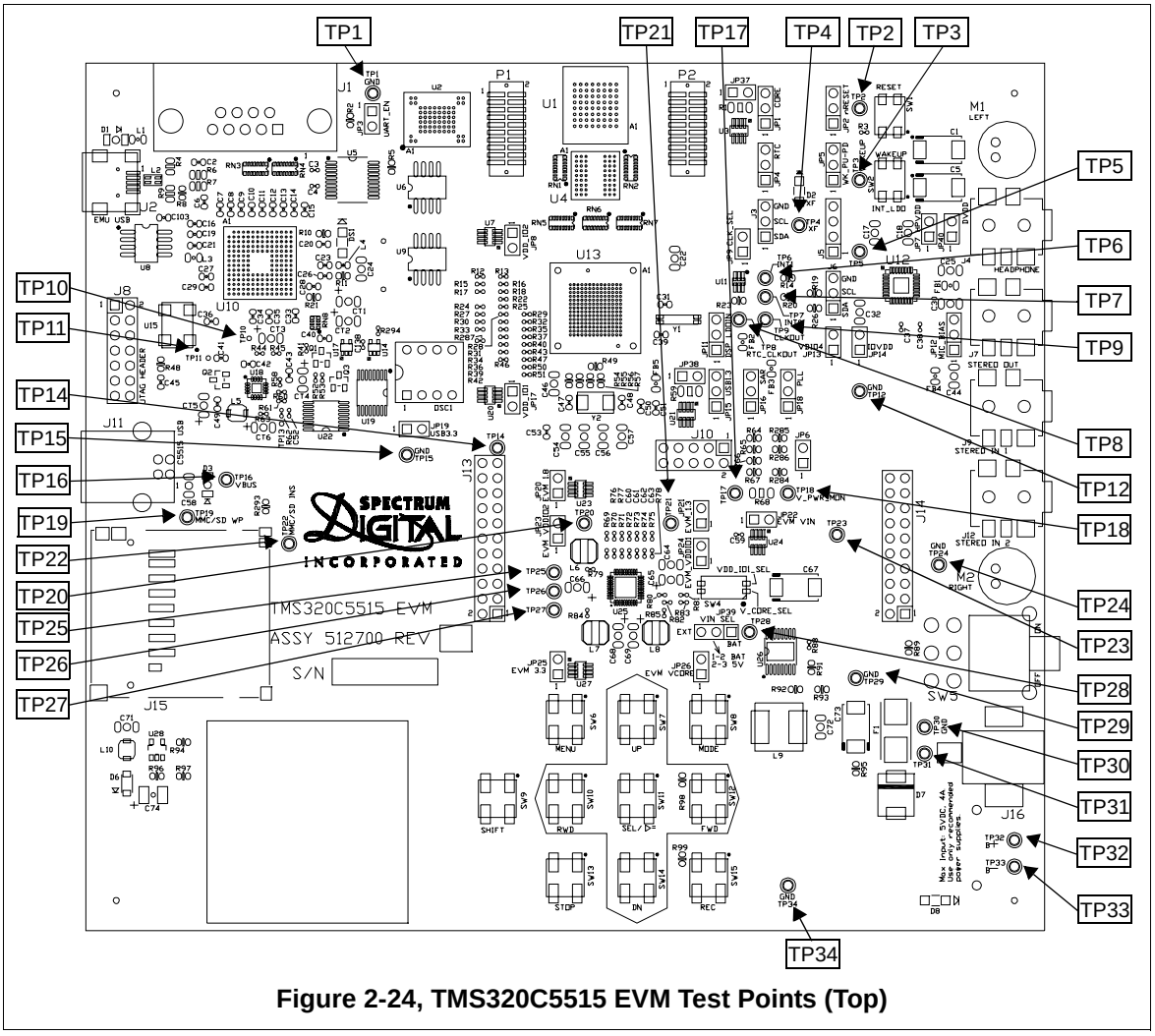

Figure 2-24, TMS320C5515 EVM Test Points (Top)

Figure below shows the location of test points on the bottom side of the C5515 EVM.

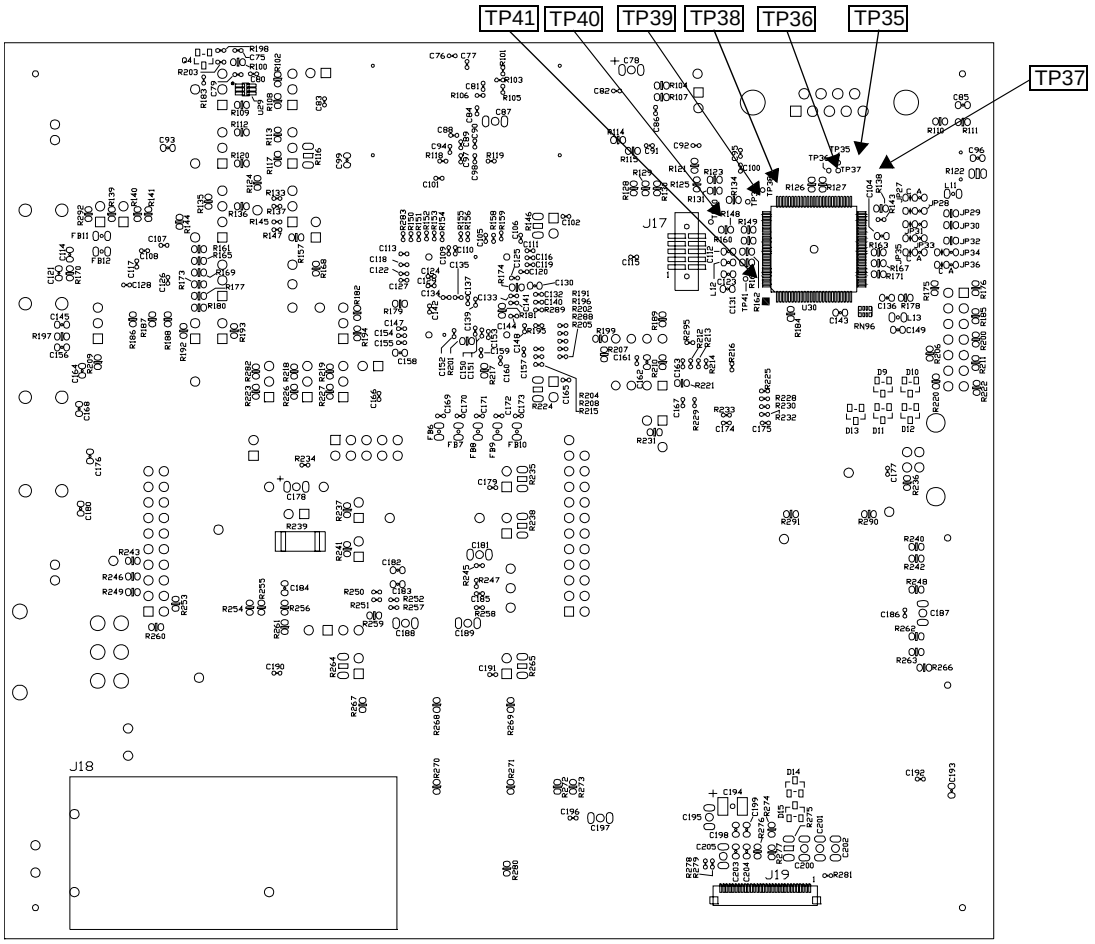

Figure 2-25, TMS320C5515 EVM Test Points (Bottom)

The table below shows the signals present on each user test point.

Table 29: C5515 EVM User Test Points

Test Point #	Signal	Schematic Page #
TP1	GND	11
TP2	nRESET	12
TP3	WAKUP	2
TP4	XF	2
TP5	AIC_GPIO	19
TP6	INT1	2
TP7	INT0	2
TP8	RTC_CLKOUT	2
TP9	CLKOUT	3
TP12	GND	15
TP13	USB_3.3V	27
TP14	GPIO5	18
TP15	GND	19
TP16	VBUS	3
TP17	TPS65023_VCC_3V3	15
TP18	V_PWR_MON	15
TP19	MMC0.WP	16
TP20	INTn	14
TP21	LOWBATn	14
TP22	MMC0.INS	16
TP23	VPWR_IN	13
TP24	GND	17
TP25	PWRFAILn	14
TP26	PWRFAIL_SNS	14
TP27	LOWBAT_SNS	14
TP28	VBATOUT	13
TP29	GND	18
TP30	GND	13
TP31	+5V Input	13
TP32	Battery +	13
TP33	Battery -	13
TP34	GND	3

The table below shows the signals present on each test point used exclusively by the factory.

Table 30: C5515 EVM Factory Test Points

Test Point #	Signal	Schematic Page #
TP10	USB_1.6V	27
TP11	USB_3.3V	27
TP35	GPIO_1	24
TP36	GPIO_0	24
TP37	CLKOUT	23
TP38	ODEMU1n	24
TP39	ODEMU0n	24
TP40	TCKR	24
TP41	USB_2.5V	27

Appendix A

Schematics

This appendix contains the schematics for the TMS320C5515 EVM. Board components with designators over 200 (e.g. DS210, R211) are part of Spectrum Digital's embedded JTAG emulator and are not included in these schematics.

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED:
4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic for layout	10/15/2009	RRP
B	Update TPS65023 Enable Logic	12/15/2009	RRP

Schematic Contents

01 - TITLE PAGE
02 - TMS320C5515 GPIO / MMC / SPI / I2C
03 - TMS320C5515 CLOCKS / JTAG / USB
04 - EMULATION - JTAG
05 - CC Board Interface
06 - TMS320C5515 EMIF
07 - Mobile DRAM Interface
08 - NAND Flash Interface
09 - NOR Flash Interface
10 - TMS320C5515 Power
11 - CPU Decoupling Caps
12 - RESET
13 - Power Input
14 - TPS65023 Power Management
15 - POWER Router
16- MMC / SD
17 - UART / EEPROMs
18 - SAR Resistor Network
19 - CODEC
20 - COLOR LCD INTERFACE

REVISION STATUS OF SHEETS

REV																				
SHEET																				
REV																				
SHEET																				
REV	A	B	A	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	11	12	13	14	15	16	17	18	19	20										
REV	B	A	A	A	A	A	A	A	A	A										
SHEET	1	2	3	4	5	6	7	8	9	10										

DWN	R.R.P.	10/15/2009	DATE
CHK	T.W.K.	10/15/2009	DATE
ENGR	R.R.P.	10/15/2009	DATE
SYSENGR	R.R.P.	10/15/2009	DATE
QA	C.M.D.	10/15/2009	DATE
QTY	R.R.P.	10/15/2009	DATE
RLSD	R.R.P.	10/15/2009	DATE

NEXT ASSY	USED ON
APPLICATION	

SPECTRUM DIGITAL INCORPORATED

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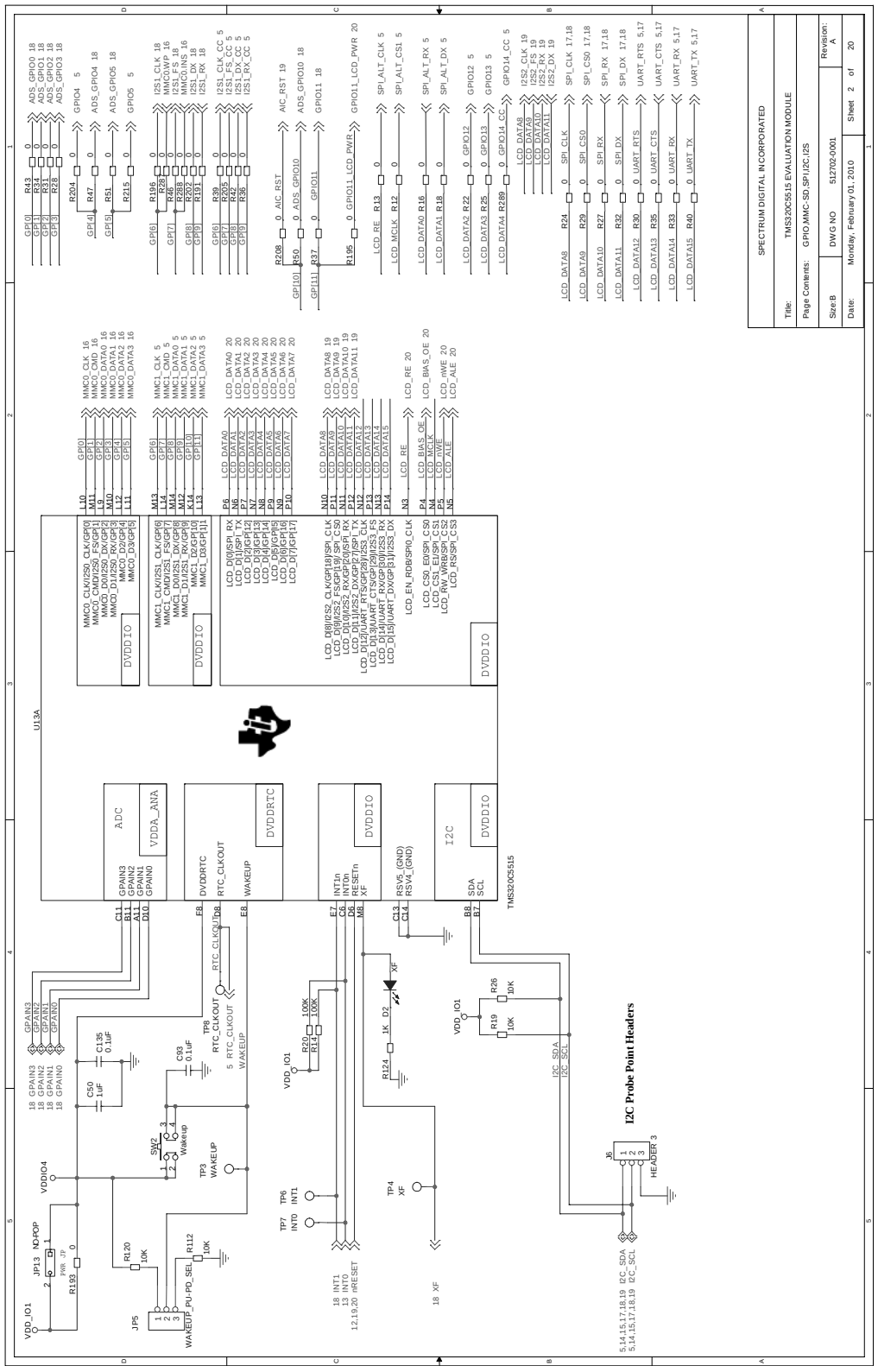
Date:	Monday, February 01, 2010 Sheet 1 of 20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Size:B DWG NO 512702-0001 Revision: A
Date: Monday, February 01, 2010 Sheet 2 of 20
I2C Probe Point Headers
U13A
TMS320C5515
ADC
VDDA_ANA
DVDDRTC
DVDDIO
I2C
JP13 NOPOP
JP5
SW2
Wakeup
TP3 WAKEUP
TP4 XF
TP6 INT1
TP7 INT0
TP8 RTC_CLKOUT
JP6
HEADER 3
WAKEUP_PU-PD_SEL
I2C_SDA
I2C_SCL
VDD_IO1
VDDIO4
ADS_GPIO0 18
ADS_GPIO1 18
ADS_GPIO2 18
ADS_GPIO3 18
GPIO4 5
ADS_GPIO4 18
ADS_GPIO5 18
GPIO5 5
I2S1_CLK 18
MMC0WP 16
I2S1_FS 18
MMC0CMD 16
I2S1_DX 18
I2S1_RX 18
I2S1_CLK_CC 5
I2S1_FS_CC 5
I2S1_DX_CC 5
I2S1_RX_CC 5
AIC_RST 19
ADS_GPIO10 18
GPIO11 18
GPIO11_LCD_PWR 20
SPI_ALT_CLK 5
SPI_ALT_CS1 5
SPI_ALT_RX 5
SPI_ALT_DX 5
GPIO12 5
GPIO13 5
GPIO14_CC 5
I2S2_CLK 19
I2S2_FS 19
I2S2_RX 19
I2S2_DX 19
SPI_CLK 17,18
SPI_CS0 17,18
SPI_RX 17,18
SPI_DX 17,18
UART_RTS 5,17
UART_CTS 5,17
UART_RX 5,17
UART_TX 5,17
MMC0_CLK 16
MMC0_CMD 16
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MMC0_DATA1 16
MMC0_DATA2 16
MMC0_DATA3 16
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MMC1_DATA1 5
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LCD_DATA7 20
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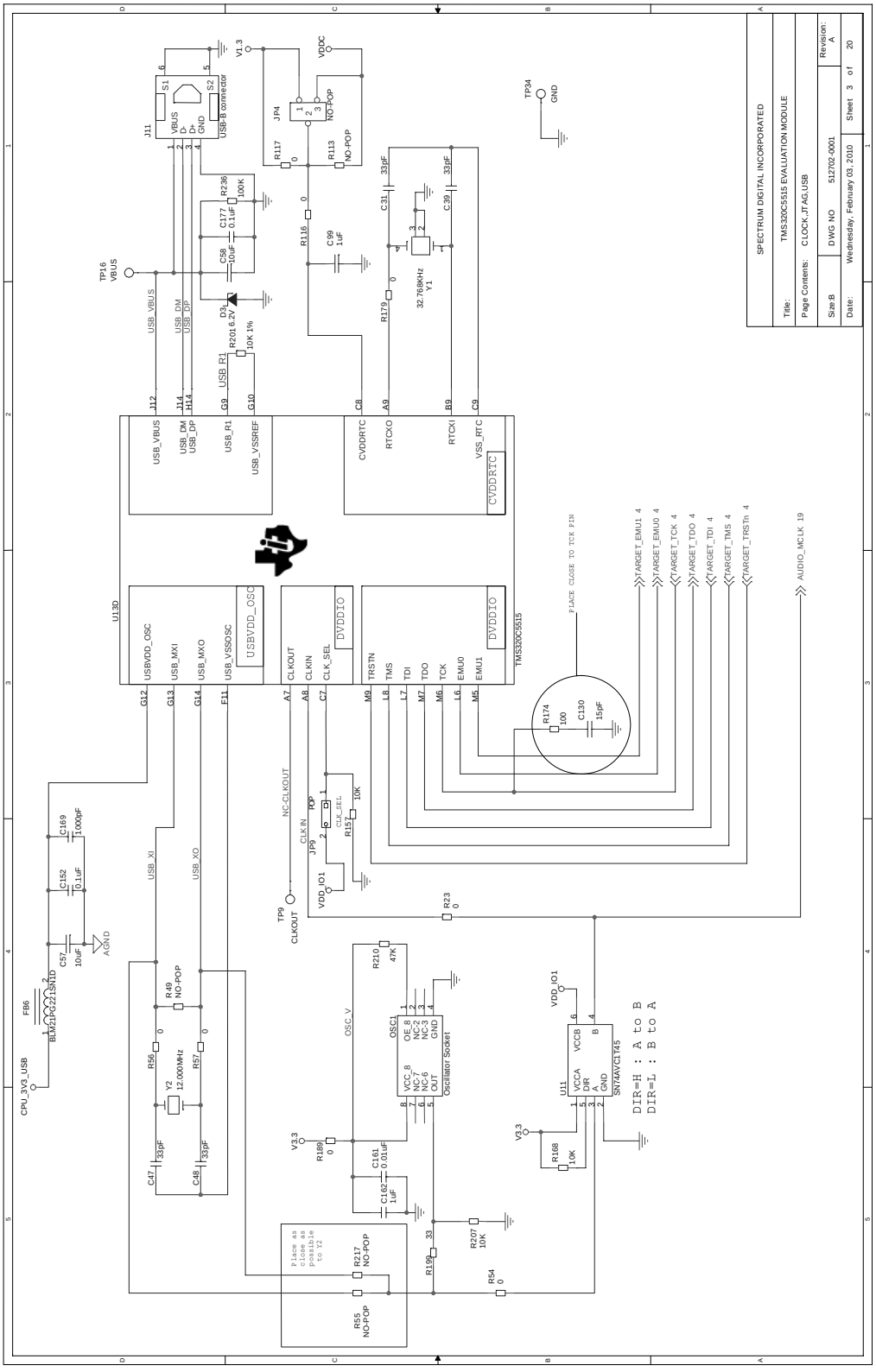
LCD_DATA9 19
LCD_DATA10 19
LCD_DATA11 19
LCD_DATA12 19
LCD_DATA13 19
LCD_DATA14 19
LCD_DATA15 19
LCD_RE 20
LCD_BIAS_OE 20
LCD_nWE 20
LCD_ALE 20
LCD_RE R13 0
LCD_MCLK R12 0
LCD_DATA0 R16 0
LCD_DATA1 R18 0
LCD_DATA2 R22 0
LCD_DATA3 R25 0
LCD_DATA4 R289 0
LCD_DATA8 R24 0
LCD_DATA9 R29 0
LCD_DATA10 R27 0
LCD_DATA11 R32 0
LCD_DATA12 R30 0
LCD_DATA13 R35 0
LCD_DATA14 R33 0
LCD_DATA15 R40 0
R208 0 AIC_RST
R50 0 ADS_GPIO10
R37 0 GPIO11
R195 0 GPIO11_LCD_PWR
R43 0
R44 0
R31 0
R28 0
R204 0
R47 0
R51 0
R215 0
R196 0
R28 0
R46 0
R288 0
R202 0
R191 0
R39 0
R205 0
R42 0
R36 0
C50 1uF
C135 0.1uF
C93 0.1uF
R193 0
R120 10K
R112 10K
R20 10K
R14 10K
R124 1K
D2
XF
R26 10K
R19 10K
C13
C14
RSV5_(GND)
RSV4_(GND)
18 INT1
13 INT0
12,19,20 nRESET
18 XF
5,14,15,17,18,19 I2C_SDA
5,14,15,17,18,19 I2C_SCL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Date: Wednesday, February 03, 2010
Sheet 3 of 20
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USB_DM
USB_DP
USB_R1
USB_VSSREF
CVDDRTC
RTCXO
RTCXI
VSS_RTC
USBVDD_OSC
USB_MXI
USB_MXO
USB_VSSOSC
CLKOUT
CLKIN
CLK_SEL
TRSTN
TMS
TDI
TDO
TCK
EMU0
EMU1
DVDDIO
USBVDD_OSC
CVDDRTC
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TARGET_EMU0 4
TARGET_TCK 4
TARGET_TDO 4
TARGET_TDI 4
TARGET_TMS 4
TARGET_TRSTn 4
AUDIO_MCLK 19
USB-B connector
32.768KHz
12.000MHz
SN74AVC1T45
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DIR=L : B to A
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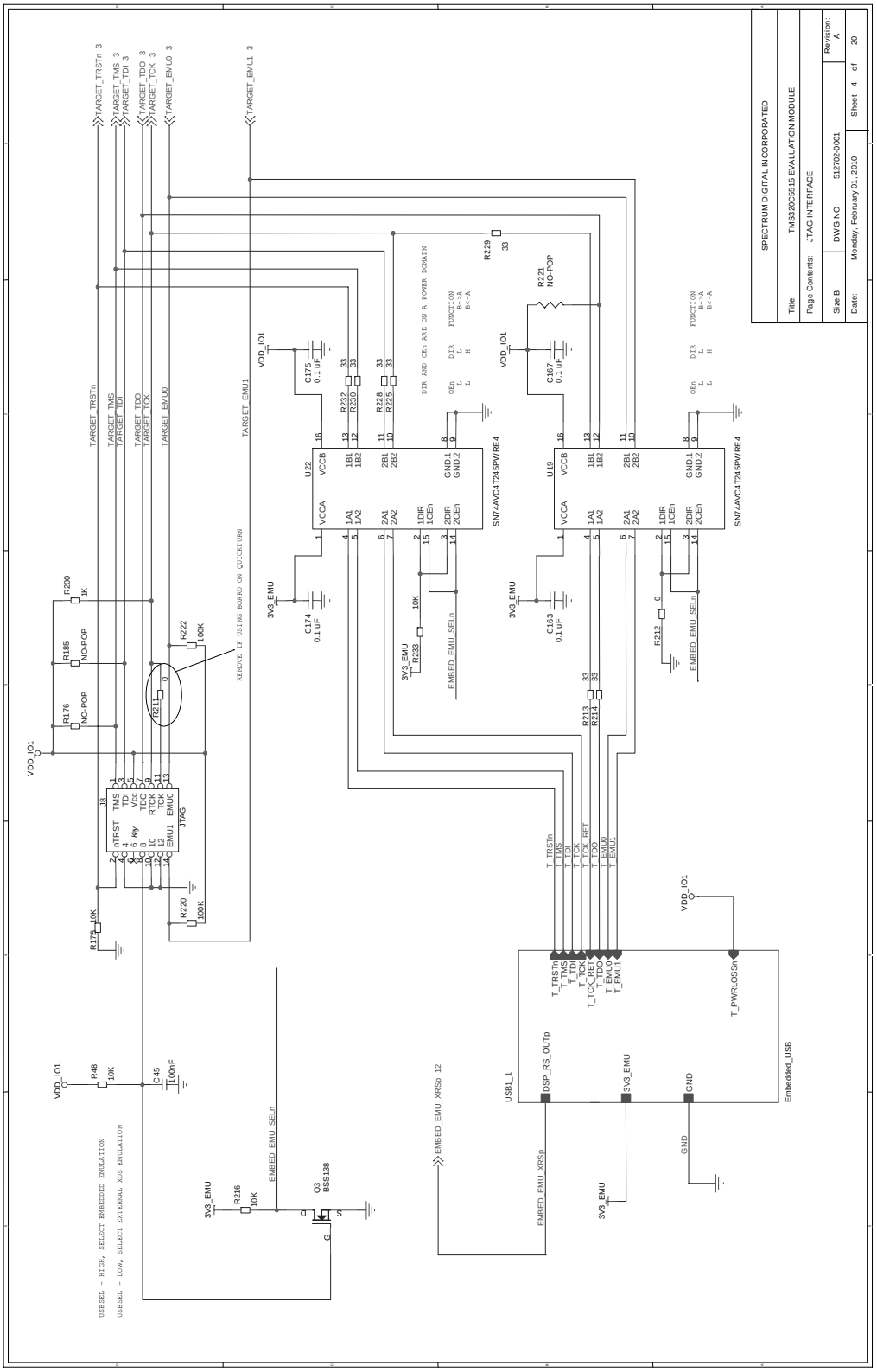
CPU_3V3_USB
AGND
CLKOUT
VDD_IO1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Revision: A
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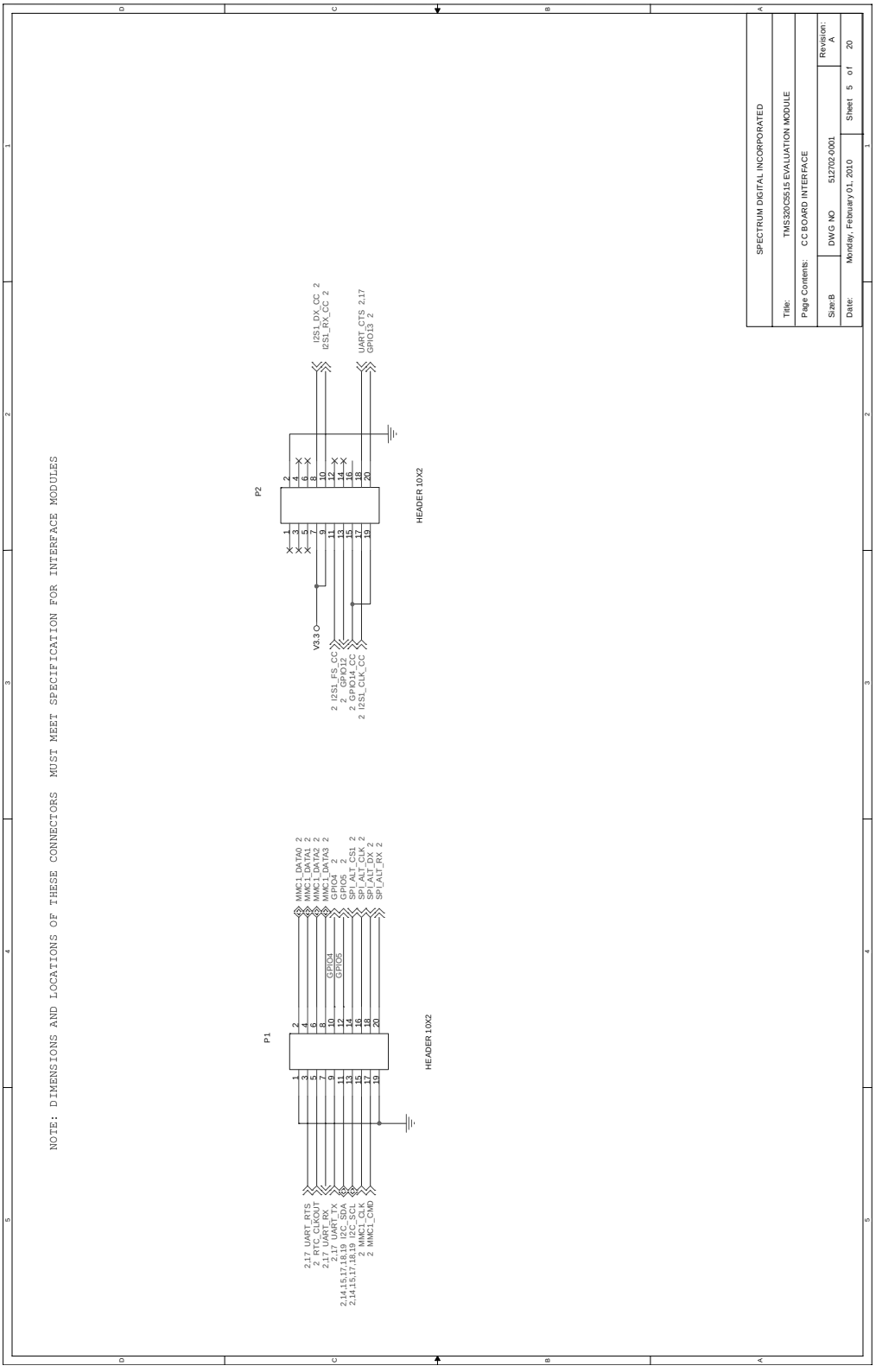
TARGET_TMS 3
TARGET_TDI 3
TARGET_TDO 3
TARGET_TCK 3
TARGET_EMU0 3
TARGET_EMU1 3
JTAG
SN74AVC4T245PWRE4
DIR AND OEn ARE ON A POWER DOMAIN
REMOVE IF USING BOARD ON QUICTURN
USB1_1
Embedded_USB
EMBED_EMU_SELn
EMBED_EMU_XRSp
USB.SEL - HIGH, SELECT EMBEDDED EMULATION
USB.SEL - LOW, SELECT EXTERNAL XDS EMULATION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Sheet 5 of 20
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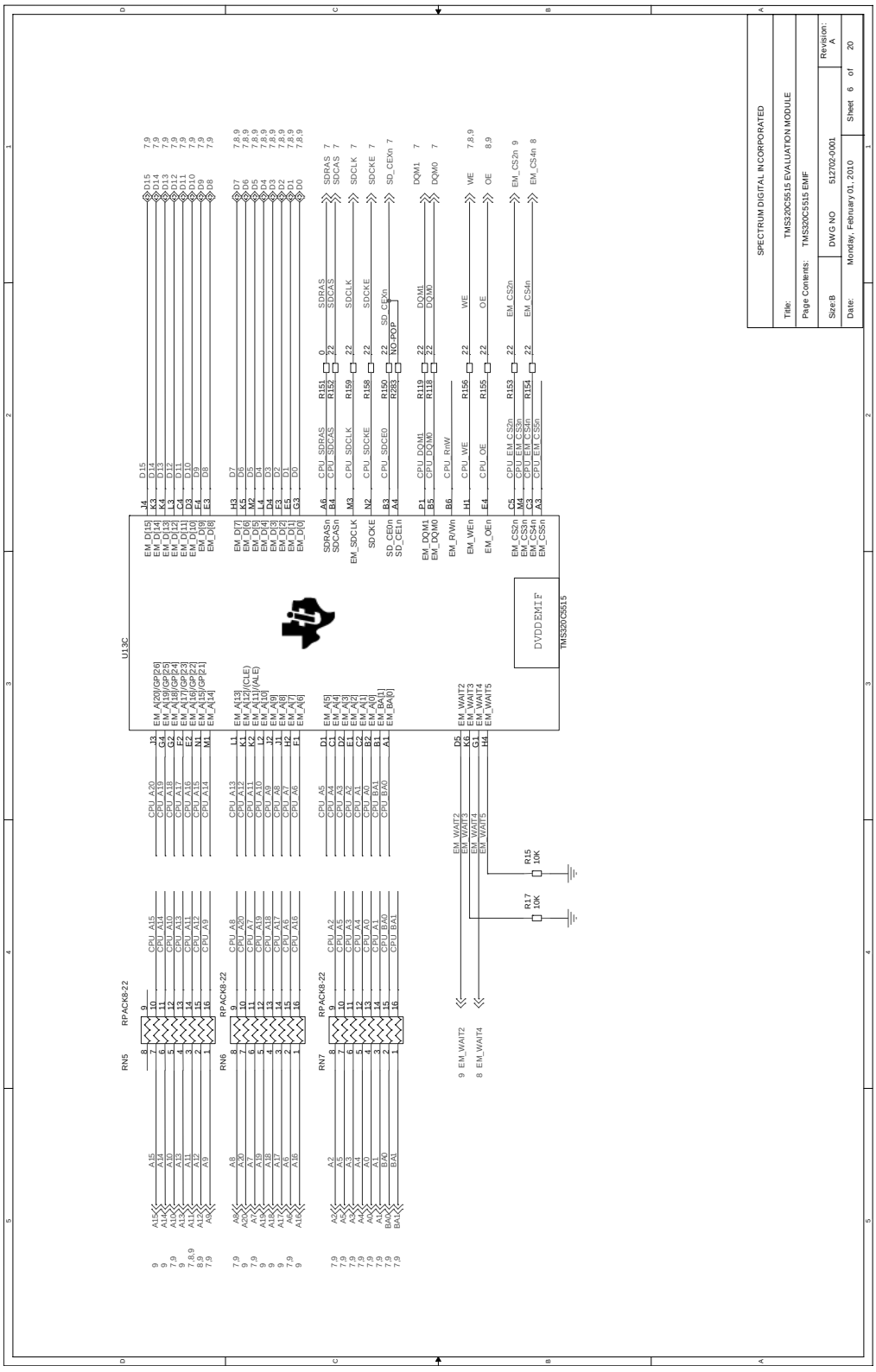
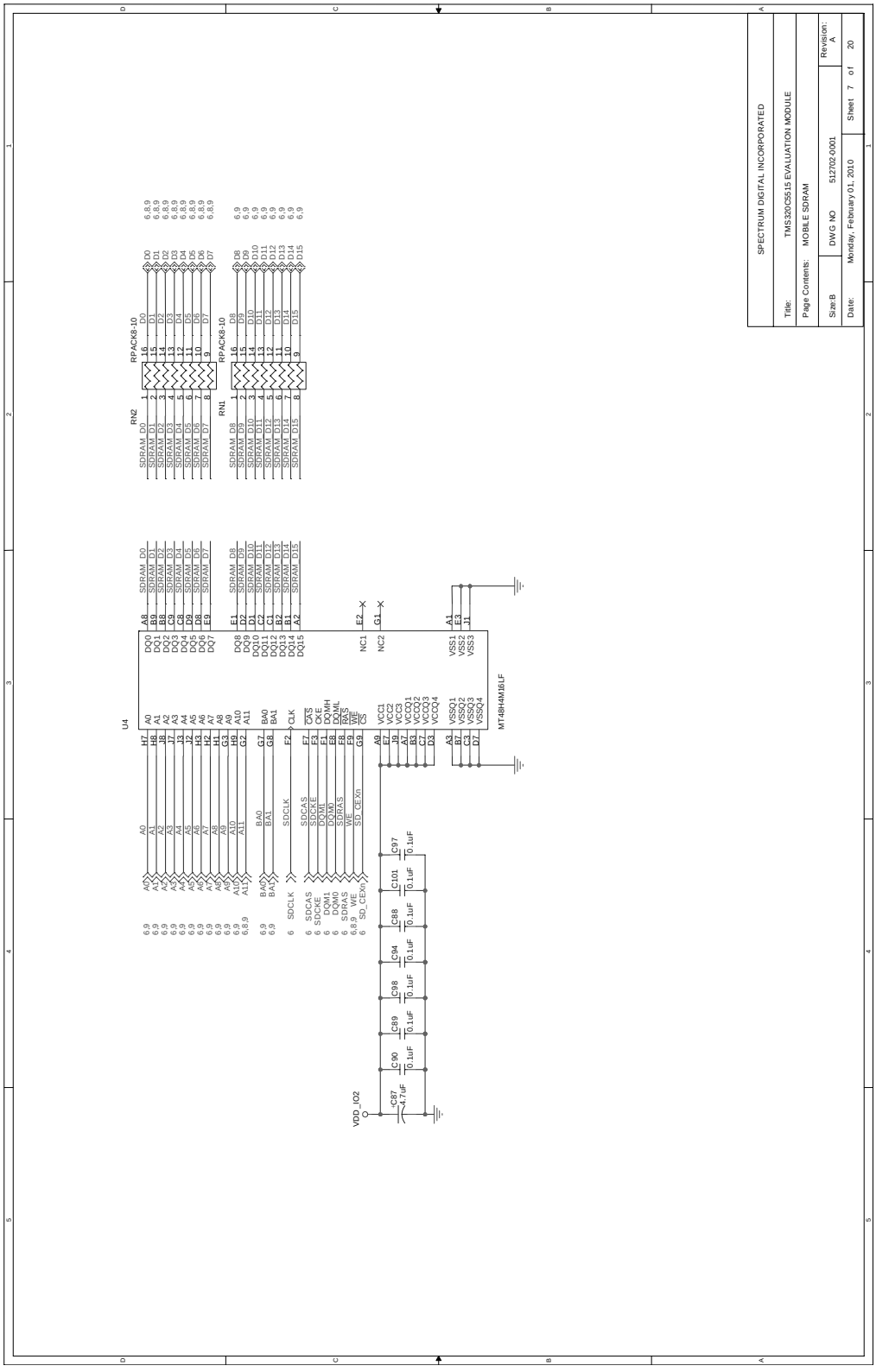
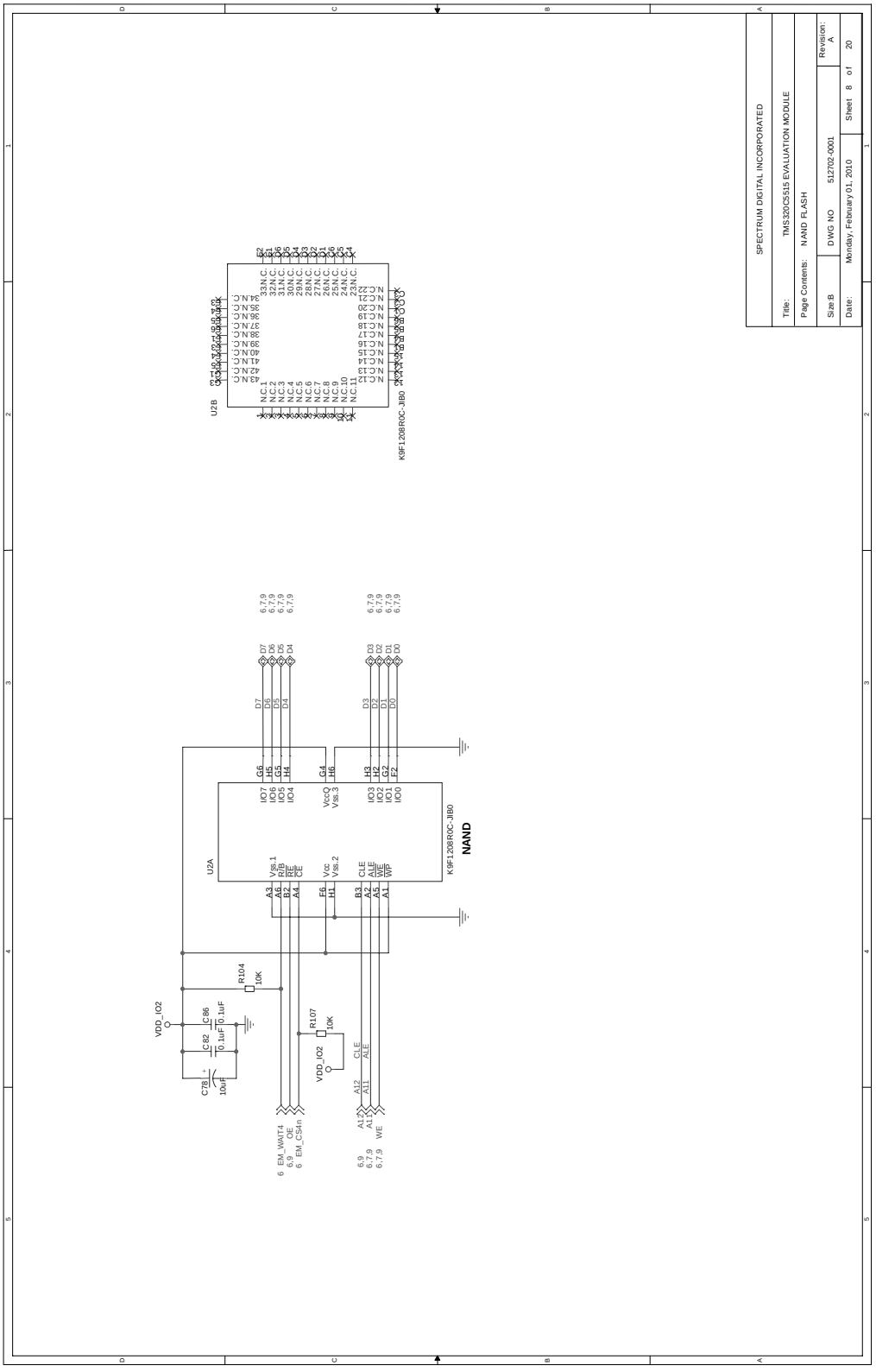
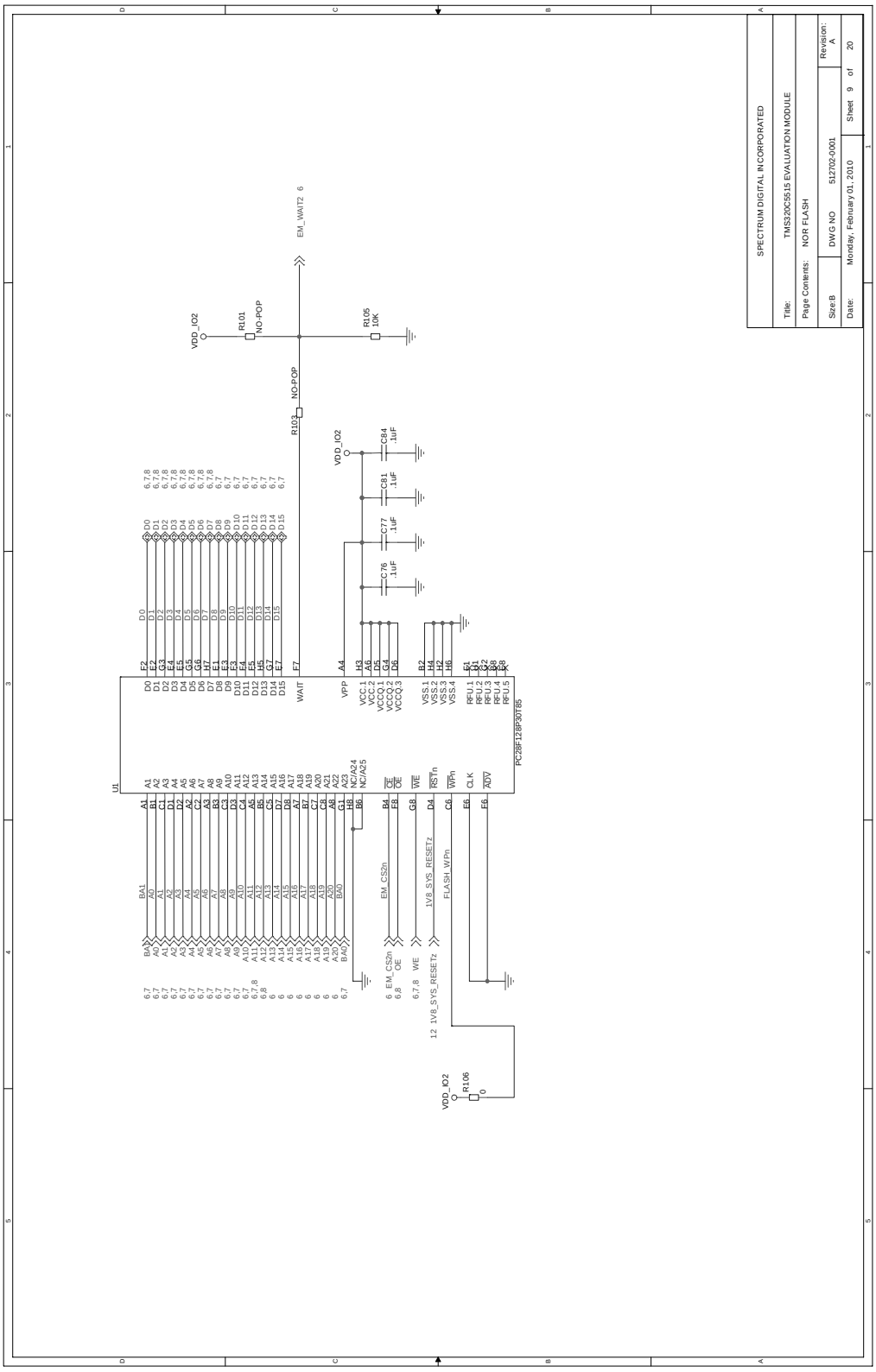
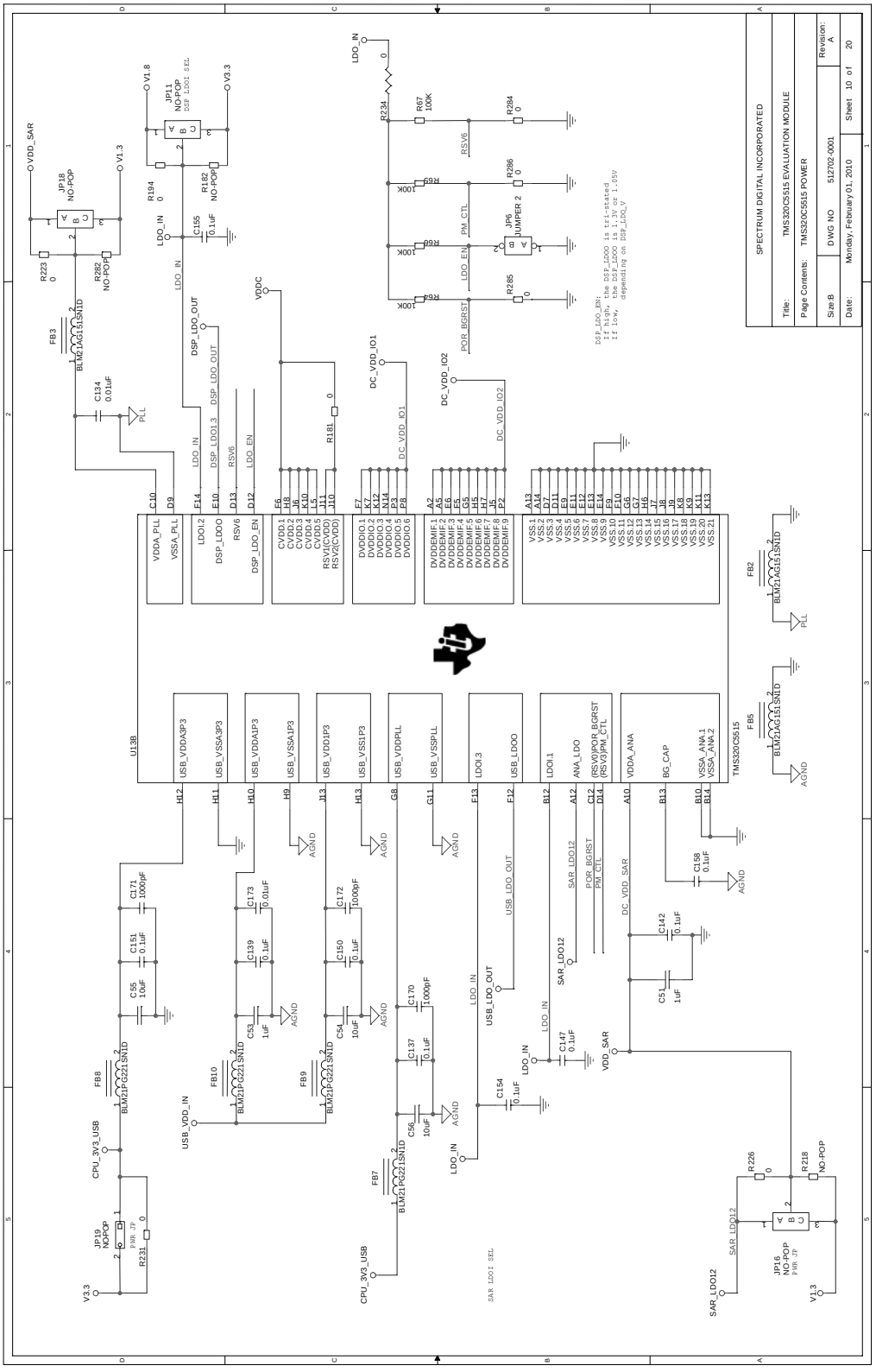
HEADER 10X2
P2
HEADER 10X2
MMC1_DATA0 2
MMC1_DATA1 2
MMC1_DATA2 2
MMC1_DATA3 2
GPIO4 2
GPIO5 2
SPI_ALT_CS1 2
SPI_ALT_CLK 2
SPI_ALT_DX 2
SPI_ALT_RX 2
2.17 UART_RTS
2 RTC_CLKOUT
2.17 UART_RX
2.17 UART_TX
2,14,15,17,18,19 I2C_SDA
2,14,15,17,18,19 I2C_SCL
2 MMC1_CLK
2 MMC1_CMD
I2S1_DX_CC 2
I2S1_RX_CC 2
UART_CTS 2,17
GPIO13 2
V3.3
2 I2S1_FS_CC
2 GPIO12
2 GPIO14_CC
2 I2S1_CLK_CC

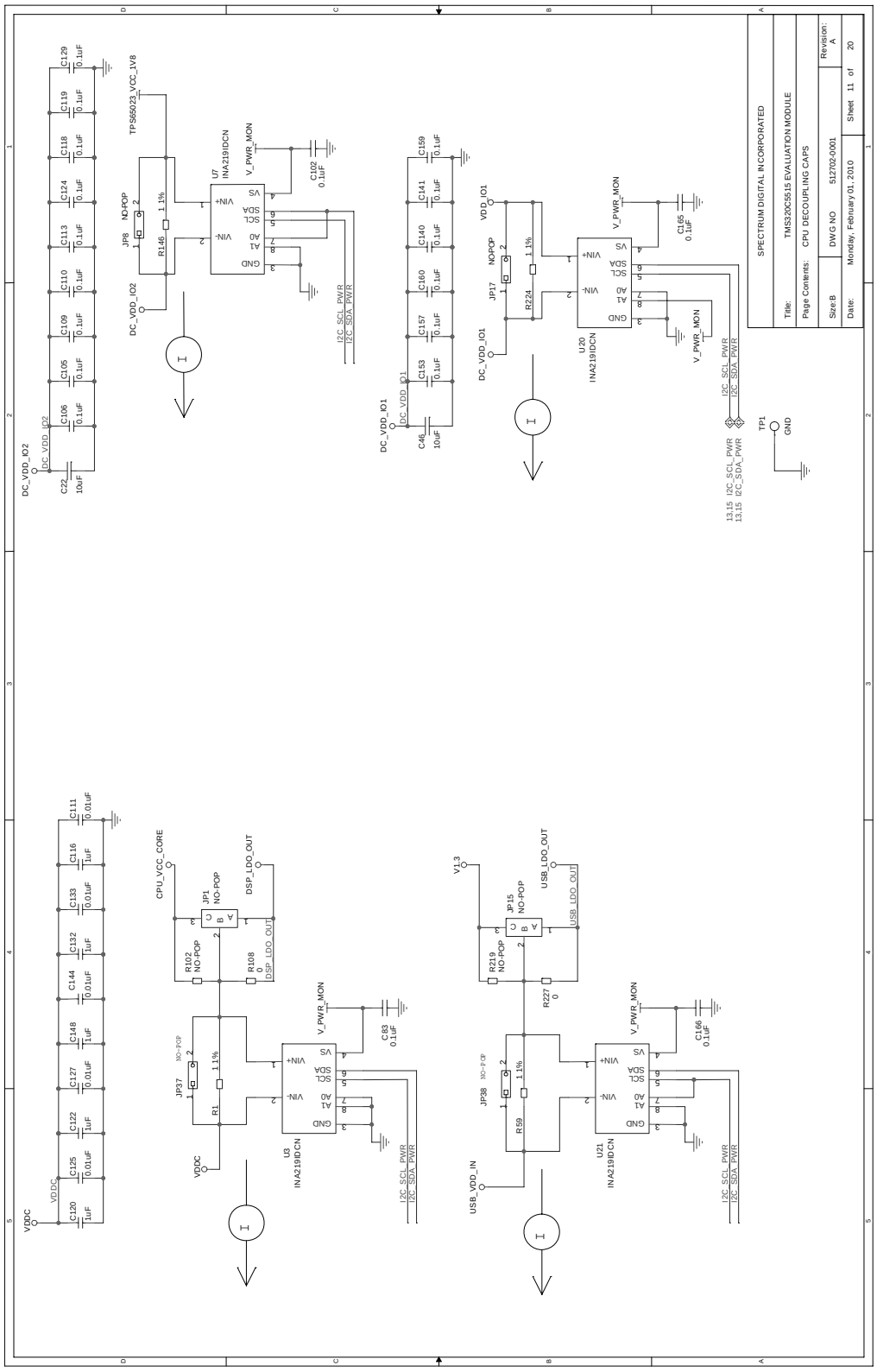

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: TMS320C5515 EMIF
Size:B
DWG NO 512702-0001
Revision: A
Date: Monday, February 01, 2010
Sheet 6 of 20
U13C
TMS320C5515
DVDDEMIF
RN5 RPACK8-22
RN6 RPACK8-22
RN7 RPACK8-22
R15 10K
R17 10K
EM_WAIT2
EM_WAIT3
EM_WAIT4
EM_WAIT5
EM_D[15]
EM_D[14]
EM_D[13]
EM_D[12]
EM_D[11]
EM_D[10]
EM_D[9]
EM_D[8]
EM_D[7]
EM_D[6]
EM_D[5]
EM_D[4]
EM_D[3]
EM_D[2]
EM_D[1]
EM_D[0]
SDRAS
SDCAS
SDCLK
SDCKE
SD_CEXn
DQM1
DQM0
EM_R/Wn
WE
OE
EM_CS2n
EM_CS3n
EM_CS4n
EM_CS5n
CPU_SDRAS
CPU_SDCAS
CPU_SDCLK
CPU_SDCKE
CPU_SDCE0
CPU_DQM1
CPU_DQM0
CPU_R/nW
CPU_WE
CPU_OE
CPU_EM_CS2n
CPU_EM_CS3n
CPU_EM_CS4n
CPU_EM_CS5n
NO-POP

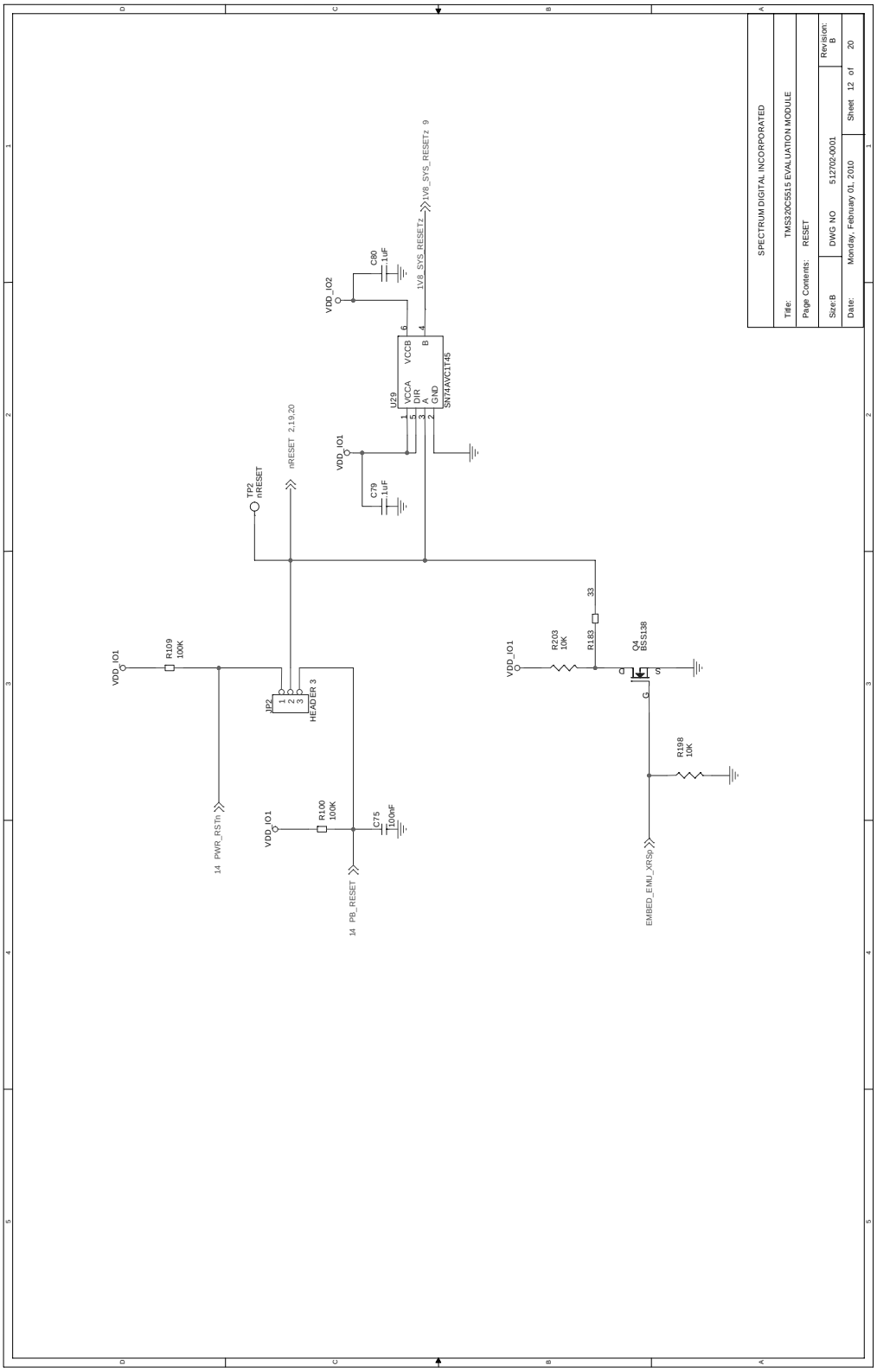

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: MOBILE SDRAM
Size:B
DWG NO 512702-0001
Revision: A
Date: Monday, February 01, 2010
Sheet 7 of 20
U4
MT48H4M16LF
RN1
RN2
RPACK8-10
C87 4.7uF
C89 0.1uF
C90 0.1uF
C94 0.1uF
C98 0.1uF
C88 0.1uF
C101 0.1uF
C97 0.1uF
VDD_IO2
SDRAM_D0
SDRAM_D1
SDRAM_D2
SDRAM_D3
SDRAM_D4
SDRAM_D5
SDRAM_D6
SDRAM_D7
SDRAM_D8
SDRAM_D9
SDRAM_D10
SDRAM_D11
SDRAM_D12
SDRAM_D13
SDRAM_D14
SDRAM_D15
SDCLK
SDCAS
SDCKE
DQM1
DQM0
SDRAS
WE
SD_CEn

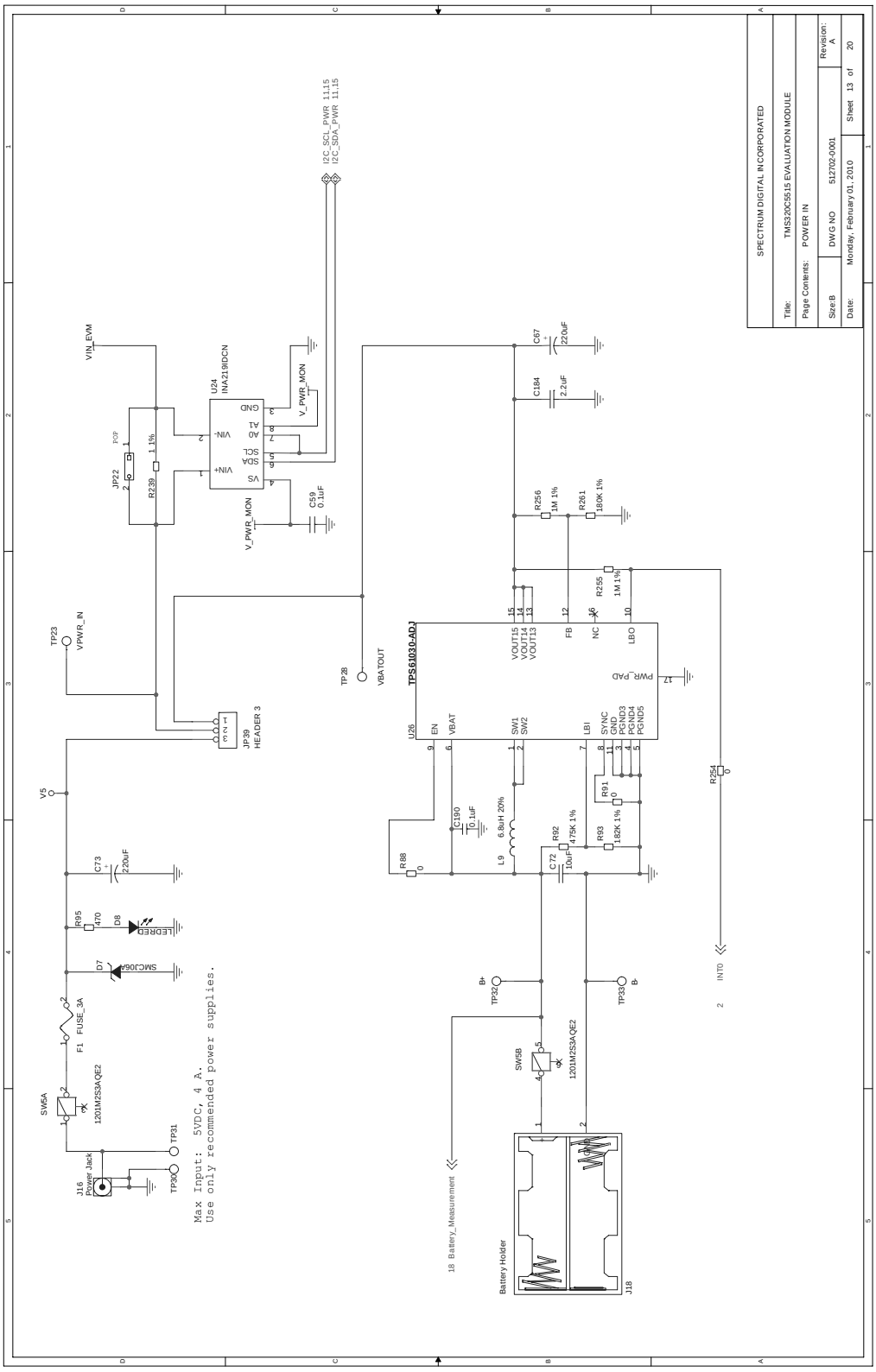

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: NAND FLASH
Size:B
DWG NO 5127702-0001
Revision: A
Date: Monday, February 01, 2010
Sheet 8 of 20
U2B
K9F1208R0C-JIB0
U2A
NAND
R104
10K
R107
10K
C86
0.1uF
C82
0.1uF
C78
10uF
VDD_IO2
CLE
ALE
WE
EM_WAIT4
EM_CS4n

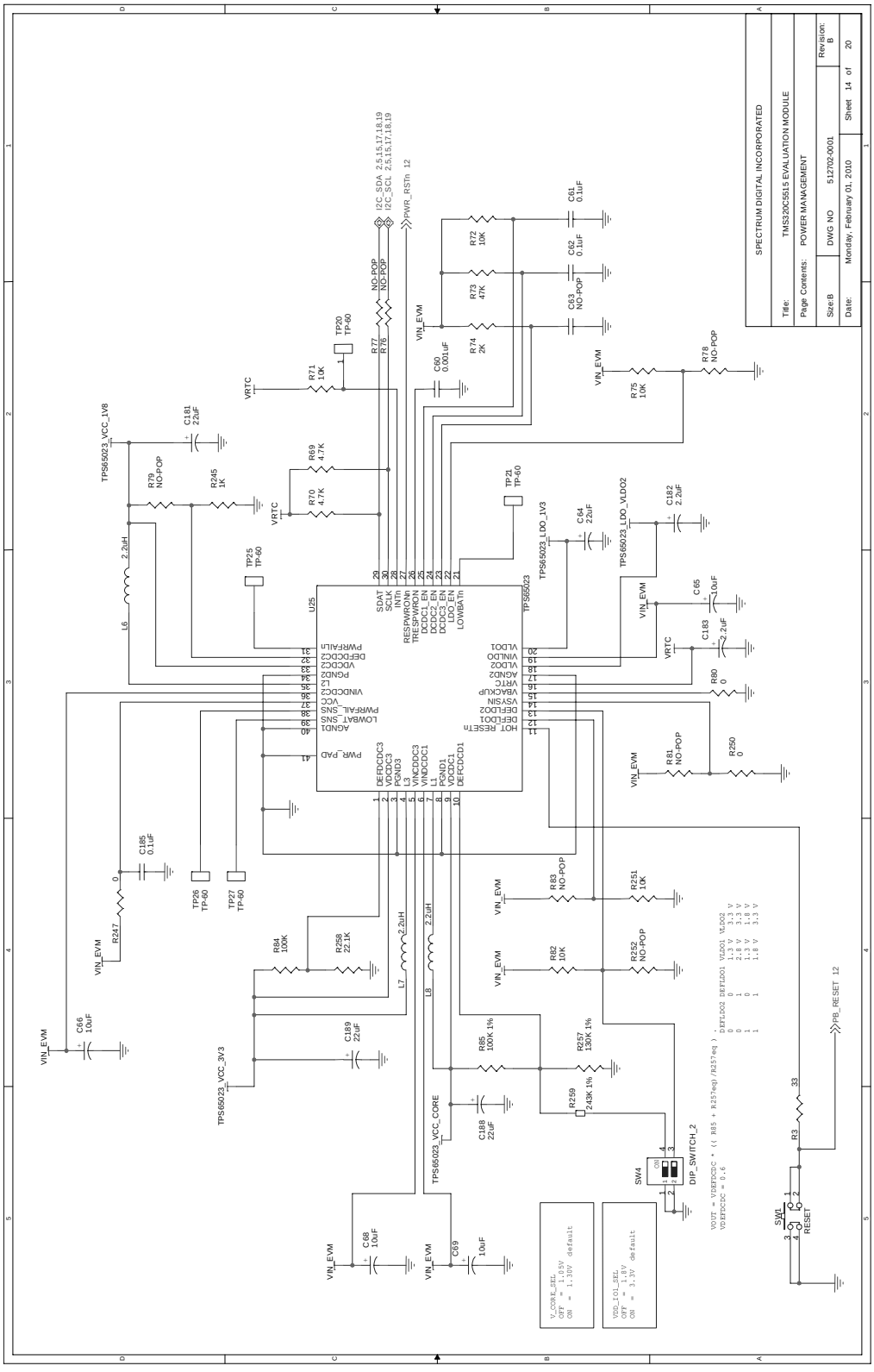

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: NOR FLASH
Size:B DWG NO 512702-0001 Revision: A
Date: Monday, February 01, 2010 Sheet 9 of 20
U1
PC28F128P30T85
R101 NO-POP
R103 NO-POP
R105 10K
R106 0
C76 .1uF
C77 .1uF
C81 .1uF
C84 .1uF
VDD_IO2
EM_WAIT2
EM_CS2n
OE
WE
1V8_SYS_RESETz
FLASH_WPn
CLK
ADV

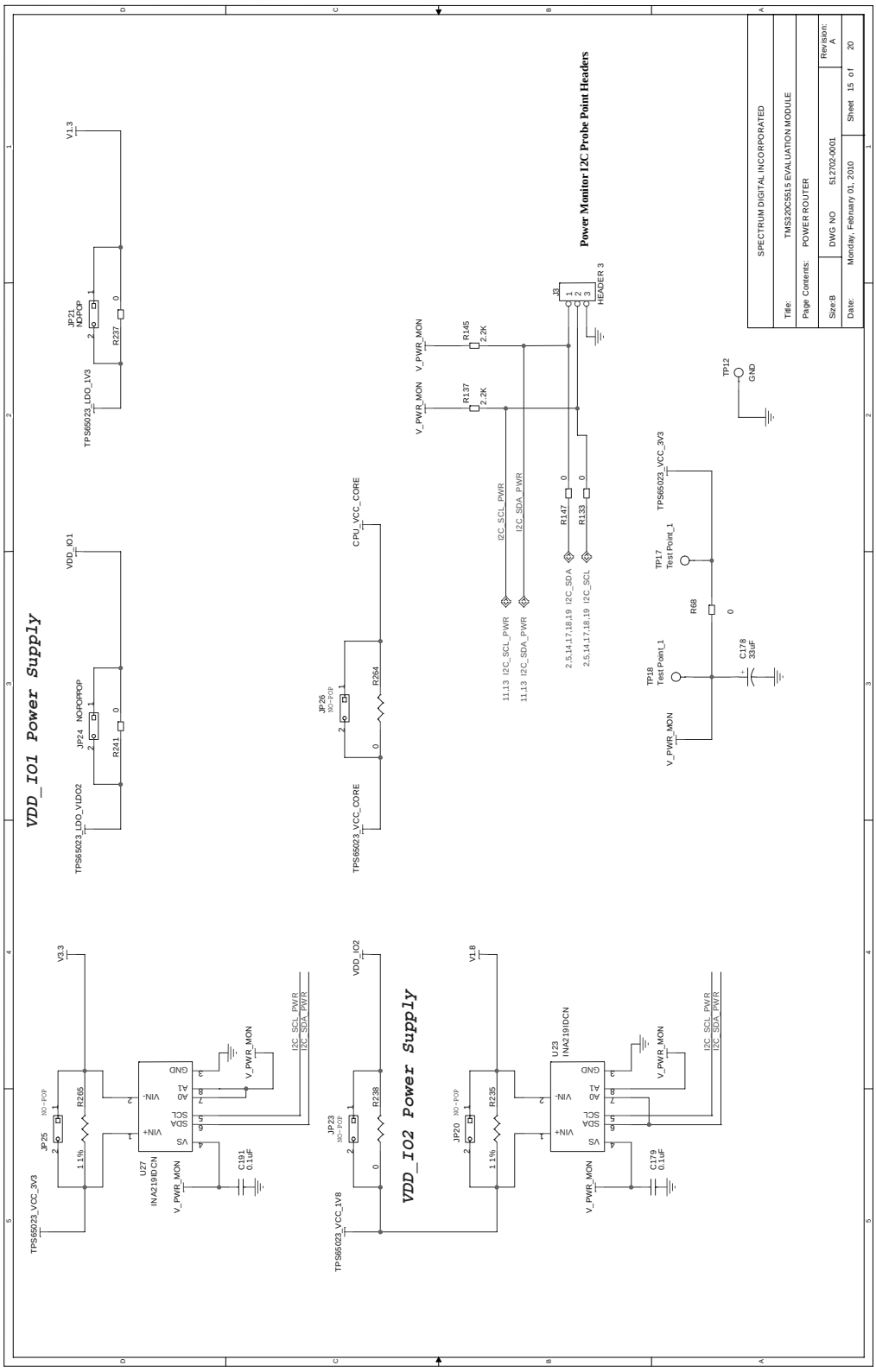

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: TMS320C5515 POWER
Size:B DWG NO 512702-0001 Revision: A
Date: Monday, February 01, 2010 Sheet 10 of 20
TMS320C5515
U13B
VDD_SAR
V1.3
V1.8
V3.3
LDO_IN
DSP_LDO_OUT
VDDC
DC_VDD_IO1
DC_VDD_IO2
POR_BGRST
PM_CTL
LDO_EN
RSV6
USB_VDD_IN
CPU_3V3_USB
SAR_LDO12
USB_LDO_OUT
VDD_SAR
DC_VDD_SAR
SAR LDO1 SEL
DSP LDO1 SEL
JP18 NO-POP
JP11 NO-POP
JP19 NO-POP
JP16 NO-POP
JP6 JUMPER 2
R234 R67 100K
R223 R282 R194 R182 R155 R181 R147 R154 R218 R226 R231
C134 C171 C151 C55 C173 C139 C53 C172 C150 C54 C170 C137 C56 C142 C51 C158
FB1 FB2 FB3 FB5 FB7 FB8 FB9 FB10
BLM21AG151SN1D
BLM21PG221SN1D
AGND
PLL

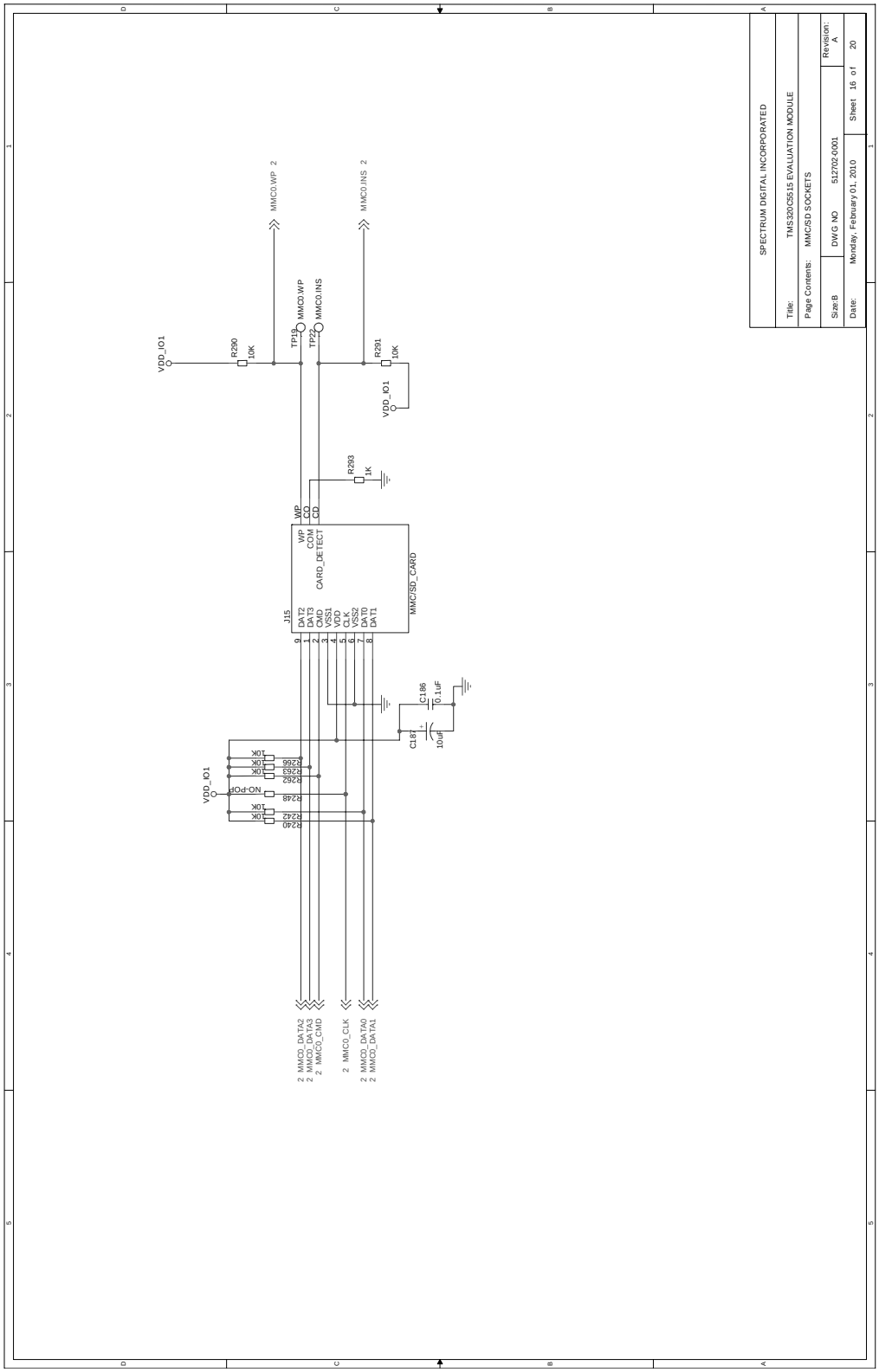

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: CPU DECOUPLING CAPS
Size: B
DWG NO 512702-0001
Revision: A
Date: Monday, February 01, 2010
Sheet 11 of 20
DC_VDD_IO2
DC_VDD_IO1
V_PWR_MON
I2C_SCL_PWR
I2C_SDA_PWR
CPU_VCC_CORE
DSP_LDO_OUT
USB_LDO_OUT
VDDC
USB_VDD_IN
GND

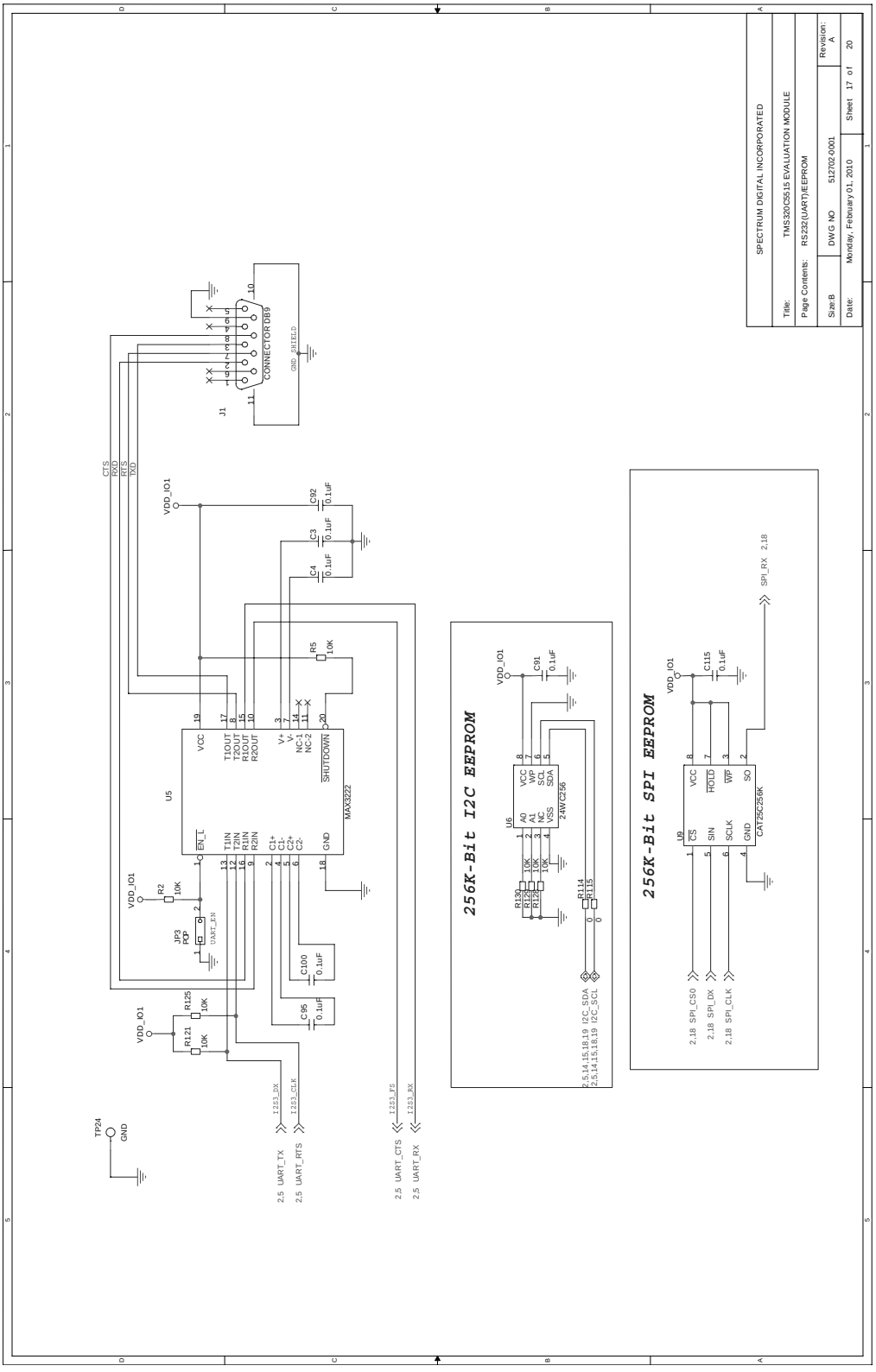

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: RESET
Size:B DWG NO 512702-0001 Revision: B
Date: Monday, February 01, 2010 Sheet 12 of 20
1V8_SYS_RESETz 9
C80 1uF
VDD_IO2
U29 SN74AVC1T45
VCCA DIR A GND VCCB B
C79 1uF
VDD_IO1
nRESET 2,19,20
TP2 nRESET
R109 100K
JP2 HEADER 3
R100 100K
C75 100nF
14 PWR_RSTn
14 PB_RESET
33
R183
R2103 10K
Q4 BSS138
R198 10K
EMBED_EMU_XRSn

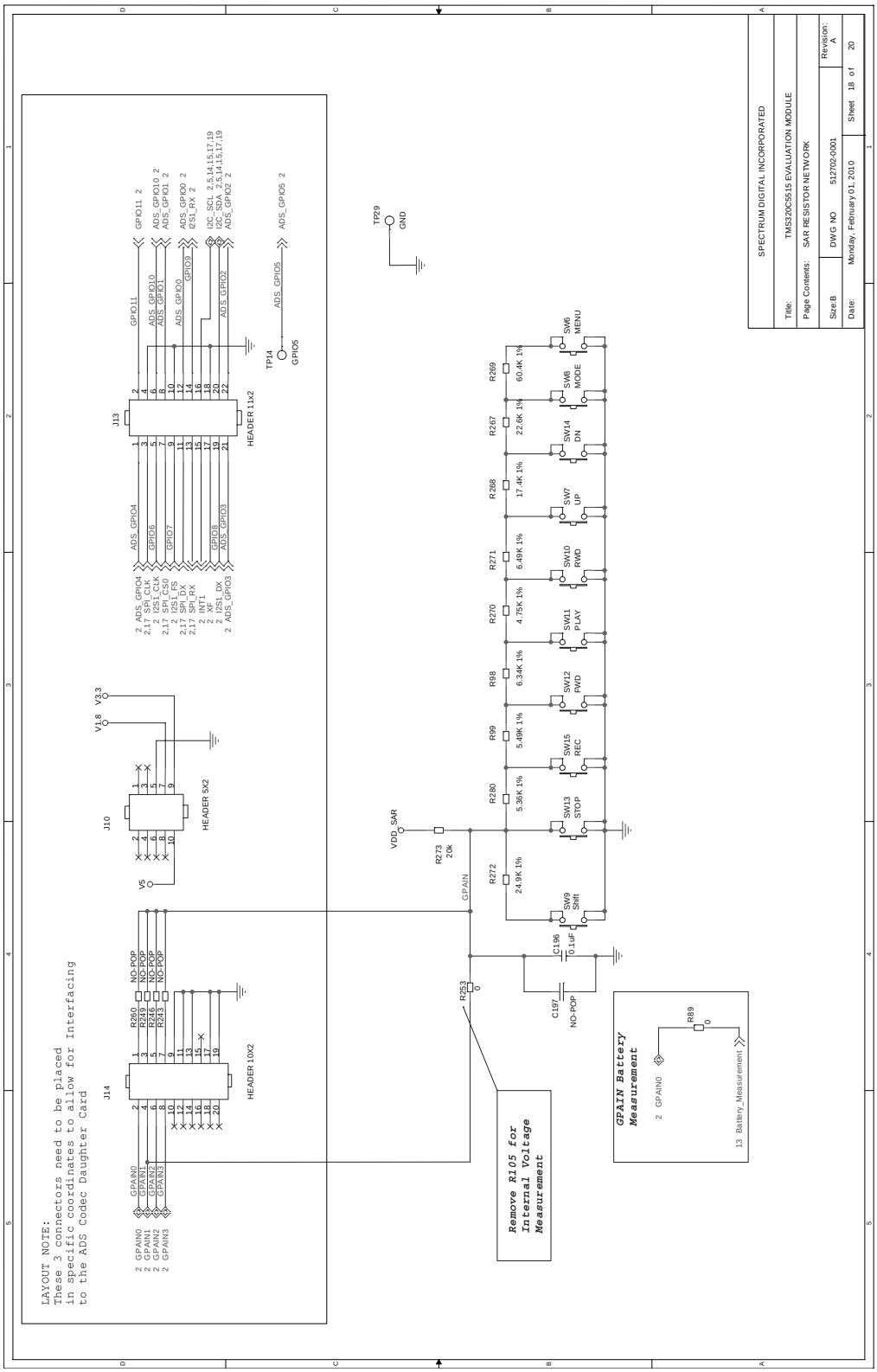

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: POWER IN
Size:B
DWG NO 512702-0001
Revision: A
Date: Monday, February 01, 2010
Sheet 13 of 20
I2C_SCL_PWR 11,15
I2C_SDA_PWR 11,15
VIN_EVM
U24 INA219IDCN
V_PWR_MON
JP22
R239 1.1%
C59 0.1uF
C67 220uF
C184 2.2uF
R256 1M 1%
R261 180K 1%
R255 1M 1%
TP23
VPWR_IN
JP39 HEADER 3
TP28
VBATOUT
U26 TPS61030-ADJ
VOUT15
VOUT14
VOUT13
FB
NC
LBO
PWR_PAD
EN
VBAT
SW1
SW2
LBI
SYNC
GND
PGND3
PGND4
PGND5
C190 0.1uF
L9 6.8uH 20%
R88 0
R91 0
R92 475K 1%
R93 182K 1%
C72 10uF
R254 0
C73 220uF
R95 470
D8 LEDRED
D7 SMCJ06A
F1 FUSE_3A
SW5A 1201M2S3AQE2
SW5B 1201M2S3AQE2
TP31
TP30
J16 Power Jack
TP32
TP33
B+
B-
18 Battery_Measurement
Battery Holder
J18
2 INT0
Max Input: 5VDC, 4 A.
Use only recommended power supplies.

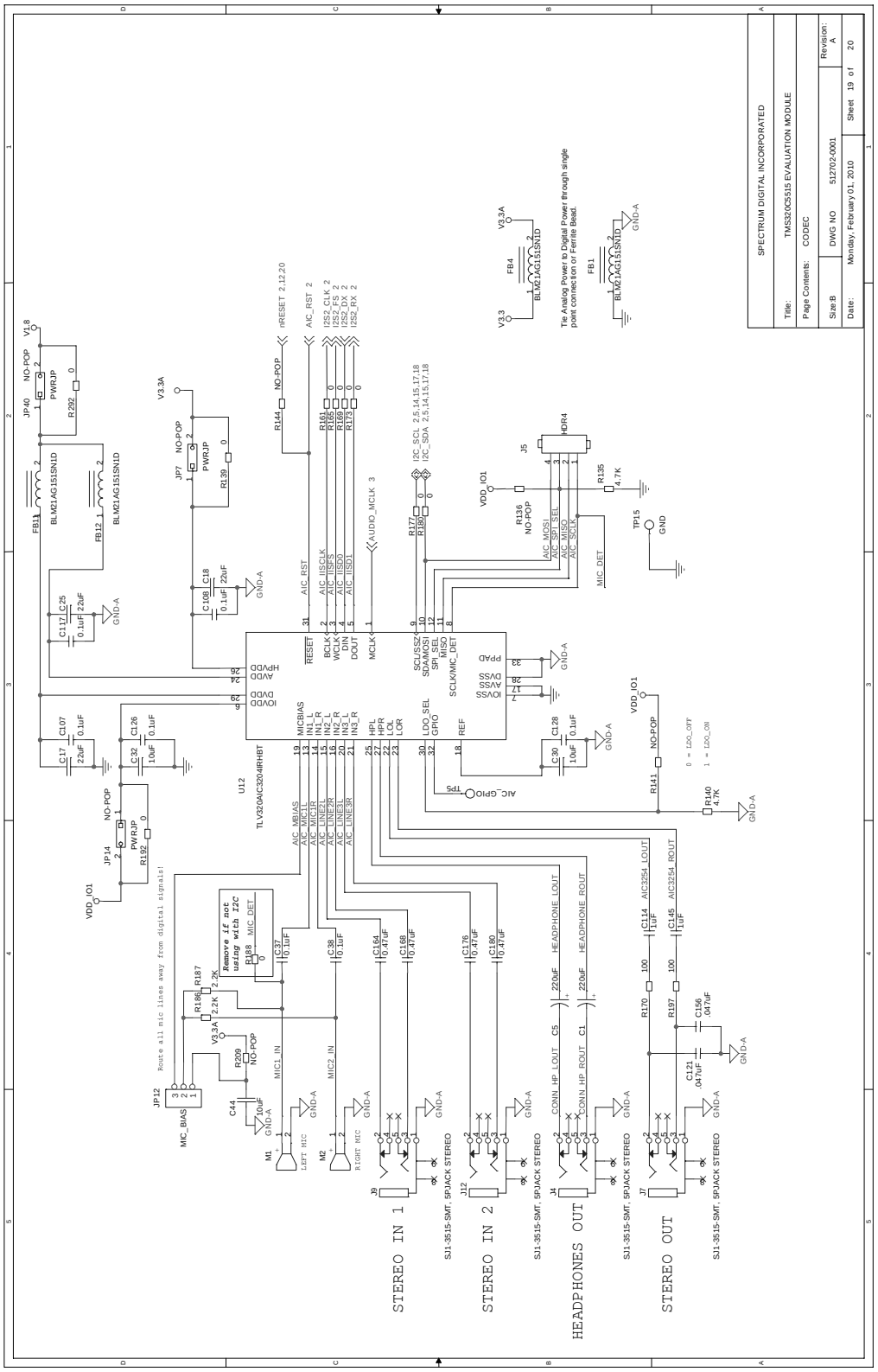

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: POWER MANAGEMENT
Size:B
DWG NO 512702-0001
Revision: B
Date: Monday, February 01, 2010
Sheet 14 of 20
TPS65023_VCC_1V8
TPS65023_VCC_3V3
TPS65023_VCC_CORE
TPS65023_LDO_1V3
TPS65023_LDO_VLDO2
VIN_EVM
VRTC
I2C_SDA 2,5,15,17,18,19
I2C_SCL 2,5,15,17,18,19
PWR_RSTn 12
PB_RESET 12
U25
TPS65023
DIP_SWITCH_2
SW4
SW1
RESET
V_CORE_SEL
OFF = 1.05V
ON = 1.30V default
VDD_IO1_SEL
OFF = 1.8V
ON = 3.3V default
VOUT = VDEFDCDC * ((R85 + R257eq)/R257eq) ,
VDEFDCDC = 0.6
DEFLDO2 DEFLDO1 VLDO1 VLDO2
0 0 1.3 V 3.3 V
0 1 2.8 V 3.3 V
1 0 1.3 V 1.8 V
1 1 1.8 V 3.3 V

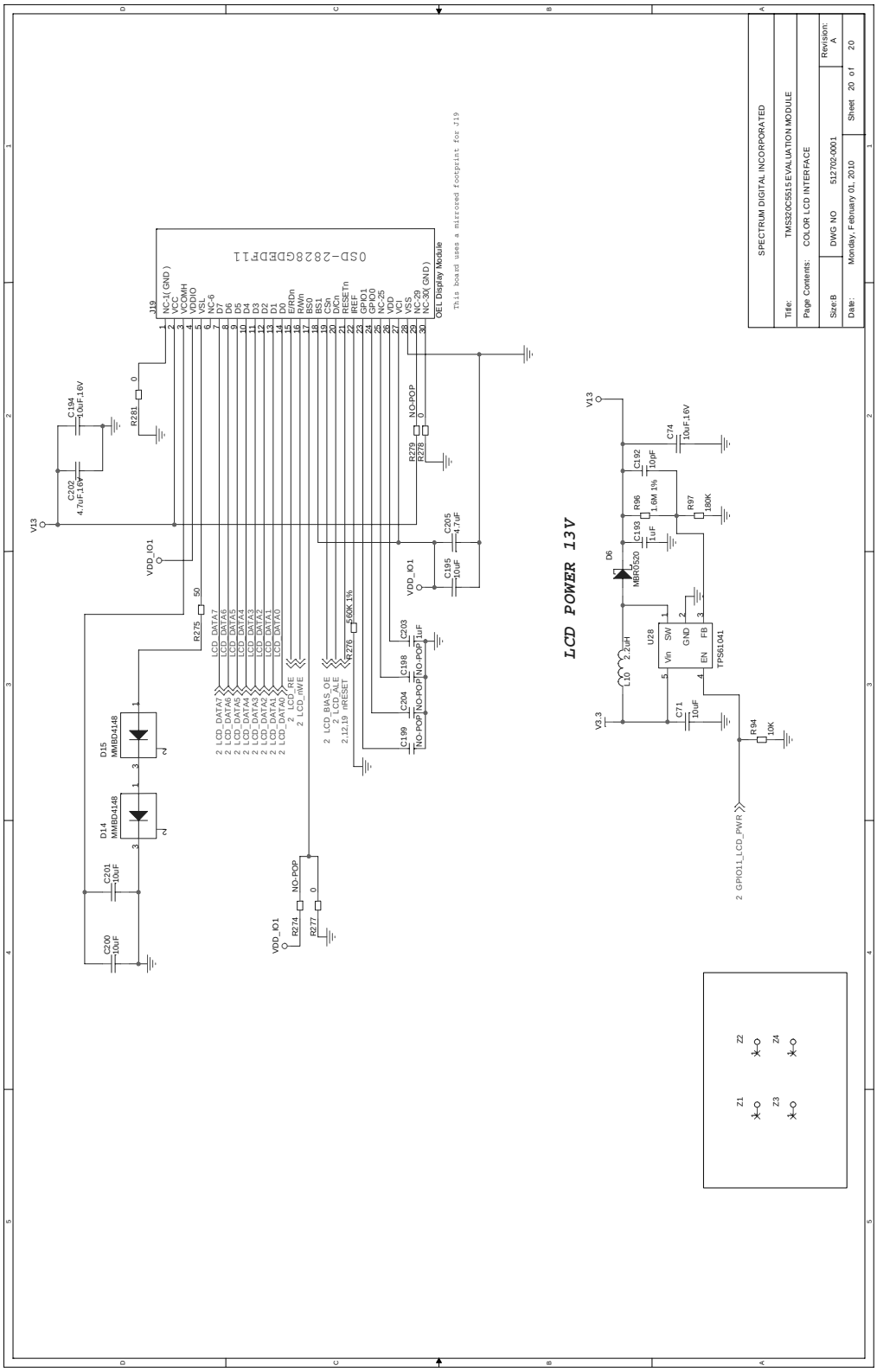

VDD_IO1 Power Supply
VDD_IO2 Power Supply
Power Monitor I2C Probe Point Headers
SPECTRUM DIGITAL INCORPORATED
TMS320C5515 EVALUATION MODULE
POWER ROUTER
DWG NO 5127702-0001
Monday, February 01, 2010
TPS65023_LDO_1V3
TPS65023_LDO_VUDO2
TPS65023_VCC_CORE
TPS65023_VCC_3V3
TPS65023_VCC_1V8
CPU_VCC_CORE
V_PWR_MON
I2C_SCL_PWR
I2C_SDA_PWR
HEADER 3
INA219IDCN
GND
VIN+
VIN-
VS
SDA
SCL
A0
A1
GND
TP12
GND
TP17
Test Point_1
TP18
Test Point_1


SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: MMC/SD SOCKETS
Size:B DWG NO 5127020001 Revision: A
Date: Monday, February 01, 2010 Sheet 16 of 20
MMC0.WP 2
MMC0.INS 2
VDD_IO1
R290 10K
TP19 MMC0.WP
TP20 MMC0.INS
R291 10K
R293 1K
J15
MMC/SD_CARD
CARD_DETECT
DAT2
DAT3
CMD
VSS1
VDD
CLK
VSS2
DAT0
DAT1
C186 0.1uF
C187 10uF
R262 10K
R263 10K
R266 10K
R248 NO-POP
R240 10K
R242 10K
2 MMC0_DATA2
2 MMC0_DATA3
2 MMC0_CMD
2 MMC0_CLK
2 MMC0_DATA0
2 MMC0_DATA1


SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: RS232(UART)/EEPROM
Size: B
DWG NO 512702-0001
Revision: A
Date: Monday, February 01, 2010
Sheet 17 of 20
256K-Bit I2C EEPROM
256K-Bit SPI EEPROM
CONNECTOR DB9
MAX3222
24WC256
CAT25C256K
VDD_IO1
UART_EN
2,5 UART_TX
2,5 UART_RTS
2,5 UART_CTS
2,5 UART_RX
2,5,14,15,18,19 I2C_SDA
2,5,14,15,18,19 I2C_SCL
2,18 SPI_CS0
2,18 SPI_DX
2,18 SPI_CLK
2,18 SPI_RX


LAYOUT NOTE:
These 3 connectors need to be placed
in specific coordinates to allow for Interfacing
to the ADS Codec Daughter Card
SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: SAR RESISTOR NETWORK
Size: B
DWG NO 512702-0001
Revision: A
Date: Monday, February 01, 2010
Sheet 18 of 20
HEADER 10X2
HEADER 11x2
HEADER SX2
Remove R105 for Internal Voltage Measurement
GPAIN Battery Measurement
VDD_SAR
R273 20k
GPAIN
C196 0.1uF
C197 NO-POP
R253 0
R89 0
R272 24.9K 1%
R280 5.36K 1%
R99 5.49K 1%
R98 6.34K 1%
R270 4.75K 1%
R271 6.49K 1%
R268 17.4K 1%
R267 22.6K 1%
R269 60.4K 1%
SW9 Shift
SW13 STOP
SW15 REC
SW12 FWD
SW11 PLAY
SW10 RWD
SW7 UP
SW14 DN
SW8 MODE
SW6 MENU
TP29 GND
TP14 GPIO5
V3.3
V1.8
V5

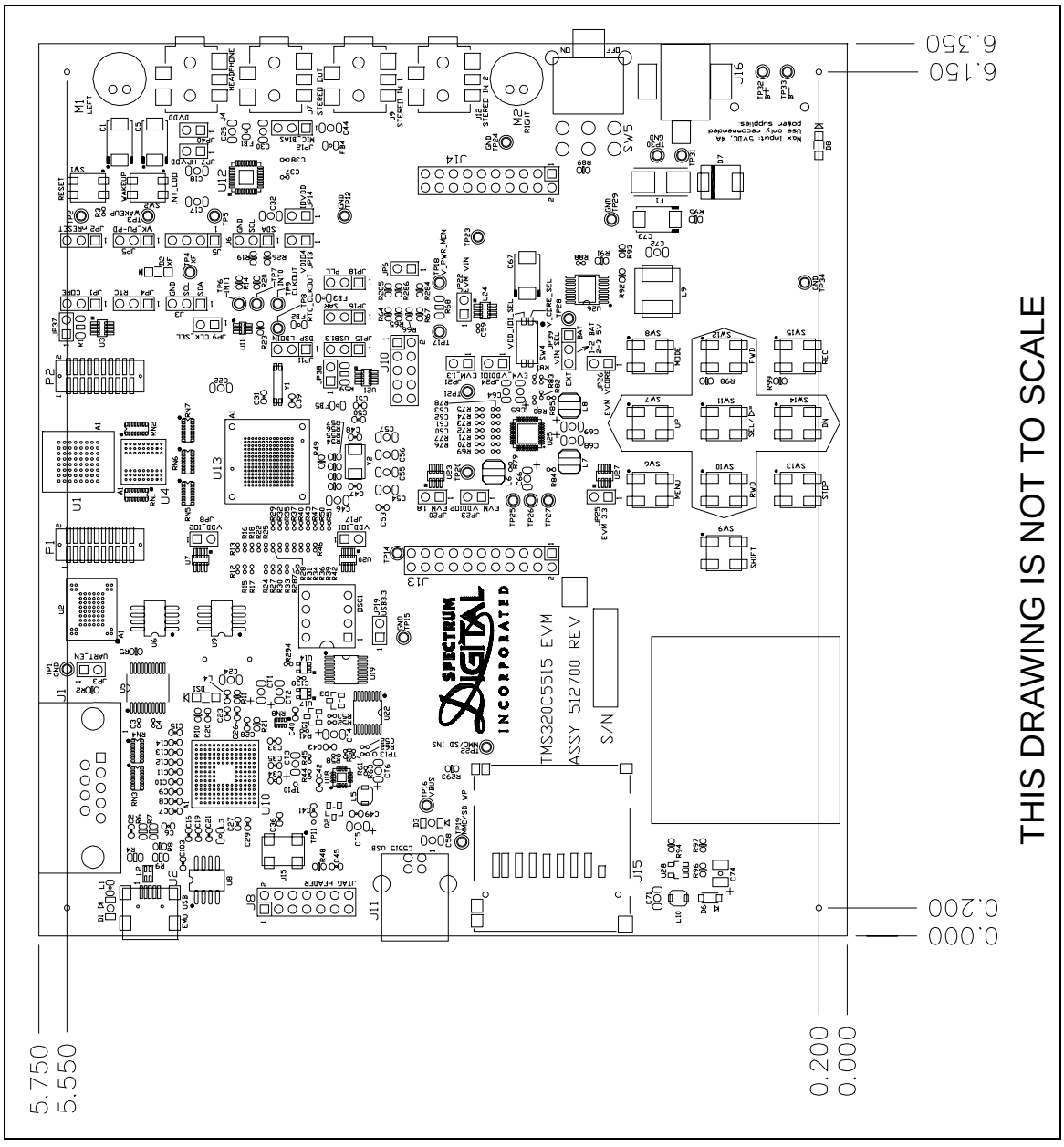

SPECTRUM DIGITAL INCORPORATED
Title: TMS320C5515 EVALUATION MODULE
Page Contents: CODEC
Size:B DWG NO 512702-0001 Revision: A
Date: Monday, February 01, 2010 Sheet 19 of 20
U12
TLV320AIC3204RHBT
STEREO IN 1
STEREO IN 2
HEADPHONES OUT
STEREO OUT
SJ1-3515-SMT, 5PJACK STEREO
Route all mic lines away from digital signals!
Remove if not using with I2C
Tie Analog Power to Digital Power through single point connection or Ferrite Bead.
0 = LDO_OFF
1 = LDO_ON


LCD POWER 13V
OSD-2828GDEDF11
SPECTRUM DIGITAL INCORPORATED
TMS320C5515 EVALUATION MODULE
COLOR LCD INTERFACE
512702-0001
Monday, February 01, 2010

Appendix B

Mechanical Information

This appendix contains the mechanical information about the TMS320C5515 EVM produced by Spectrum Digital.


THIS DRAWING IS NOT TO SCALE
6.350
6.150
0.200
0.000
5.750
5.550
0.200
0.000
TMS320C5515 EVM
ASSY 512700 REV
S/N

[redacted]

SPECTRUM DIGITAL INCORPORATED

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512705-0001 Rev. A