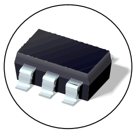


Low Quiescent Current, Programmable-Delay Supervisory Circuit

FEATURES

- **Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s**
- **Very Low Quiescent Current: 2.4μA typ**
- **High Threshold Accuracy: 0.5% typ**
- **Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V Are Available**
- **Manual Reset ($\overline{\text{MR}}$) Input**
- **Open-Drain $\overline{\text{RESET}}$ Output**
- **Temperature Range: -40°C to 125°C**
- **Small SOT23 Package**

APPLICATIONS

- **DSP or Microcontroller Applications**
- **Notebook/Desktop Computers**
- **PDAs/Hand-Held Products**
- **Portable/Battery-Powered Products**
- **FPGA/ASIC Applications**

DESCRIPTION

The TPS3808xxx family of microprocessor supervisory circuits monitor system voltages from 0.4V to 5.0V, asserting an open drain $\overline{\text{RESET}}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{\text{MR}}$) pin drops to a logic low. The $\overline{\text{RESET}}$ output remains low for the user adjustable delay time after the SENSE voltage and manual reset ($\overline{\text{MR}}$) return above their thresholds.

The TPS3808 uses a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3V$. The reset delay time can be set to 20ms by disconnecting the CT pin, 300ms by connecting the CT pin to V_{DD} using a resistor, or can be user-adjusted between 1.25ms and 10s by connecting the CT pin to an external capacitor. The TPS3808 has a very low typical quiescent current of 2.4μA so it is well-suited to battery-powered applications. It is available in a small SOT23 package and is fully specified over a temperature range of -40°C to +125°C.

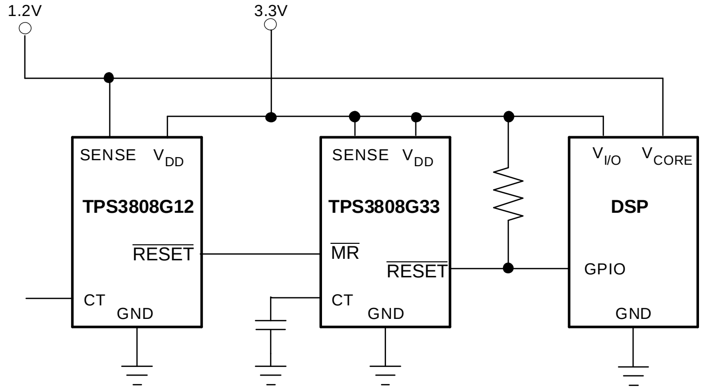
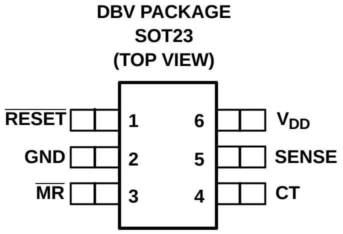


Figure 1. Typical Application Circuit



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	NOMINAL SUPPLY VOLTAGE(1)	THRESHOLD VOLTAGE (V_{IT})	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS380G801	Adjustable	0.405V	-40°C to +125°C	AVW	TPS3808G01DBVT	Tape and Reel, 250
					TPS3808G01DBVR	Tape and Reel, 3000
TPS3808G09	0.9V	0.84V	-40°C to +125°C	AVV	TPS3808G09DBVT	Tape and Reel, 250
					TPS3808G09DBVR	Tape and Reel, 3000
TPS3808G12	1.2V	1.12V	-40°C to +125°C	AVY	TPS3808G12DBVT	Tape and Reel, 250
					TPS3808G12DBVR	Tape and Reel, 3000
TPS3808G15	1.5V	1.40V	-40°C to +125°C	AVS	TPS3808G15DBVT	Tape and Reel, 250
					TPS3808G15DBVR	Tape and Reel, 3000
TPS3808G18	1.8V	1.67V	-40°C to +125°C	AVR	TPS3808G18DBVT	Tape and Reel, 250
					TPS3808G18DBVR	Tape and Reel, 3000
TPS3808G25	2.5V	2.33V	-40°C to +125°C	AVQ	TPS3808G25DBVT	Tape and Reel, 250
					TPS3808G25DBVR	Tape and Reel, 3000
TPS3808G30	3.0V	2.79V	-40°C to +125°C	AVP	TPS3808G30DBVT	Tape and Reel, 250
					TPS3808G30DBVR	Tape and Reel, 3000
TPS3808G33	3.3V	3.07V	-40°C to +125°C	AVO	TPS3808G33DBVT	Tape and Reel, 250
					TPS3808G33DBVR	Tape and Reel, 3000
TPS3808G50	5.0V	4.65V	-40°C to +125°C	AVN	TPS3808G50DBVT	Tape and Reel, 250
					TPS3808G50DBVR	Tape and Reel, 3000

(1) Custom threshold voltages from 0.82V to 3.3V, 4.4V to 5.0V are available on a quick-turn basis for fast prototyping. Minimum order quantities apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range (unless otherwise noted)(1)

	TPS3808	UNIT
Input voltage range, V_{DD}	-0.3 to 7.0	V
CT voltage range, V_{CT}	-0.3 to V_{DD} + 0.3	V
Other voltage ranges: V_{RESET}, V_{MR}, V_{SENSE}	-0.3 to 7	V
$\overline{\text{RESET}}$ pin current	5	mA
Operating junction temperature range, T_J(2)	-40 to +150	°C
Storage temperature range, T_{STG}	-65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) Due to the low dissipated power in this device, it is assumed that $T_J = T_A$.

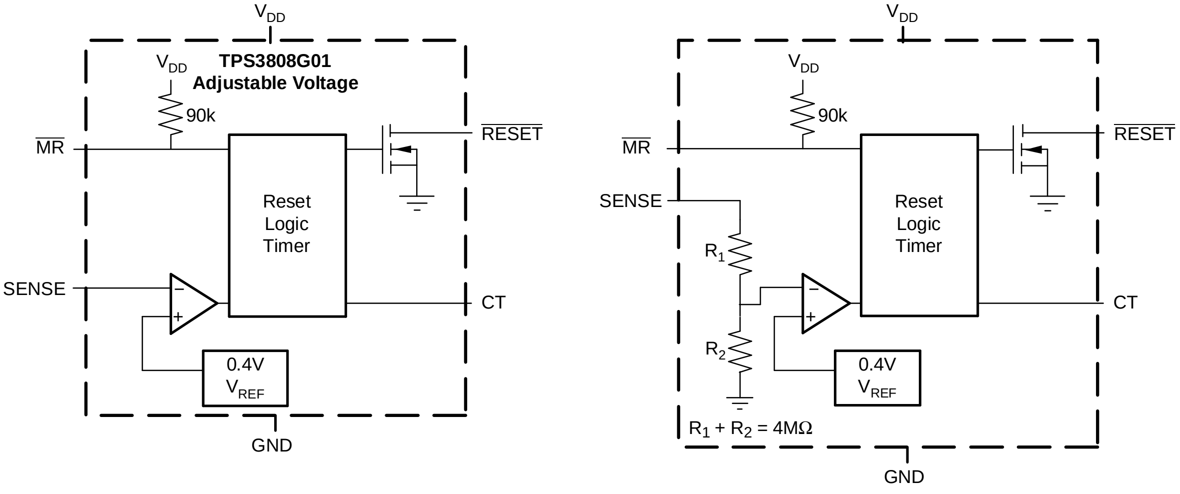
ELECTRICAL CHARACTERISTICS

$1.8V \le V_{DD} \le 6.5V$, $R_{LRESET} = 100k\Omega$, $C_{LRESET} = 50pF$, over operating temperature range (T_J = -40°C to +125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.8		6.5	V
I_{DD}	Supply current (current into V_{DD} pin)		V_{DD} = 3.3V, $\overline{\text{RESET}}$ not asserted $\overline{\text{MR}}$, $\overline{\text{RESET}}$, CT open		2.4	5.0	µA
			V_{DD} = 6.5V, $\overline{\text{RESET}}$ not asserted $\overline{\text{MR}}$, $\overline{\text{RESET}}$, CT open		2.7	6.0	µA
V_{OL}	Low-level output voltage		$1.3V \le V_{DD} < 1.8V$, I_{OL} = 0.4mA			0.3	V
			$1.8V \le V_{DD} \le 6.5V$, I_{OL} = 1.0mA			0.4	V
	Power-up reset voltage(1)		V_{OL} (max) = 0.2V, $I_{\overline{RESET}}$ = 15µA			0.8	V
V_{IT}	Negative-going input threshold accuracy	TPS3808G01		-2.0	±1.0	+2.0	%
		$V_{IT} \le 3.3V$		-1.5	±0.5	+1.5	
		$3.3V < V_{IT} \le 5.0V$		-2.0	±1.0	+2.0	
		$V_{IT} \le 3.3V$	-40°C < T_J < +85°C	-1.25	±0.5	+1.25	
		$3.3V < V_{IT} \le 5.0V$	-40°C < T_J < +85°C	-1.5	±0.5	+1.5	
V_{hys}	Hysteresis on V_{IT} pin	TPS3808G01			1.5	3.0	$\%V_{IT}$
		Fixed versions			1.0	2.5	
$R_{\overline{MR}}$	$\overline{\text{MR}}$ Internal pull-up resistance			70	90		kΩ
I_{SENSE}	Input current at SENSE pin	TPS3808G01	$V_{SENSE} = V_{IT}$	-25		25	nA
		Fixed versions	V_{SENSE} = 6.5V		1.7		µA
I_{OH}	$\overline{\text{RESET}}$ leakage current		$V_{\overline{RESET}}$ = 6.5V, $\overline{\text{RESET}}$ not asserted			300	nA
C_{IN}	Input capacitance, any pin	CT pin	V_{IN} = 0V to V_{DD}		5		pF
		Other pins	V_{IN} = 0V to 6.5V		5		
V_{IL}	$\overline{\text{MR}}$ logic low input			0.3 V_{DD}			V
V_{IH}	$\overline{\text{MR}}$ logic high input					0.7 V_{DD}	
t_w	Maximum transient duration	SENSE	$V_{IH} = 1.05V_{IT}$, $V_{IL} = 0.95V_{IT}$		20		µs
		$\overline{\text{MR}}$	$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$		0.001		
t_d	$\overline{\text{RESET}}$ delay time	CT = Open	See timing diagram	12	20	28	ms
		CT = V_{DD}		180	300	420	ms
		CT = 100pF		0.75	1.25	1.75	ms
		CT = 180nF		0.7	1.2	1.7	s
t_{pHL}	Propagation delay	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$	$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$		150		ns
	High to low level $\overline{\text{RESET}}$ delay	SENSE to $\overline{\text{RESET}}$	$V_{IH} = 1.05V_{IT}$, $V_{IL} = 0.95V_{IT}$		20		µs
θ_{JA}	Thermal resistance, junction-to-ambient				290		°C/W

(1) The lowest supply voltage (V_{DD}) at which $\overline{\text{RESET}}$ becomes active. $T_{rise(VDD)} \ge 15µs/V$.

FUNCTIONAL BLOCK DIAGRAMS



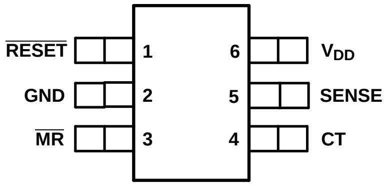
Adjustable Voltage Version

Fixed Voltage Version

Figure 2. Adjustable and Fixed Voltage Versions

PIN ASSIGNMENTS

DBV PACKAGE
SOT23
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	SOT23 (DBV) PIN NO.	
$\overline{\text{RESET}}$	1	$\overline{\text{RESET}}$ is an open drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{\text{MR}}$ pin is set to a logic low). $\overline{\text{RESET}}$ will remain low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{\text{MR}}$ is set to a logic high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD}.
GND	2	Ground
$\overline{\text{MR}}$	3	Driving the manual reset pin ($\overline{\text{MR}}$) low asserts $\overline{\text{RESET}}$. $\overline{\text{MR}}$ is internally tied to V_{DD} by a 90kΩ pull-up resistor.
CT	4	Reset period programming pin. Connecting this pin to V_{DD} through a 40kΩ to 200kΩ resistor or leaving it open results in fixed delay times (see ***Electrical Characteristics***). Connecting this pin to a ground referenced capacitor ≥ 100pF gives a user-programmable delay time. See *Selecting The Reset Delay Time* in the **Device Operation** section for more information.
SENSE	5	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT}, then $\overline{\text{RESET}}$ is asserted.
V_{DD}	6	Supply voltage. It is good analog design practice to place a 0.1µF ceramic capacitor close to this pin.

TIMING DIAGRAM

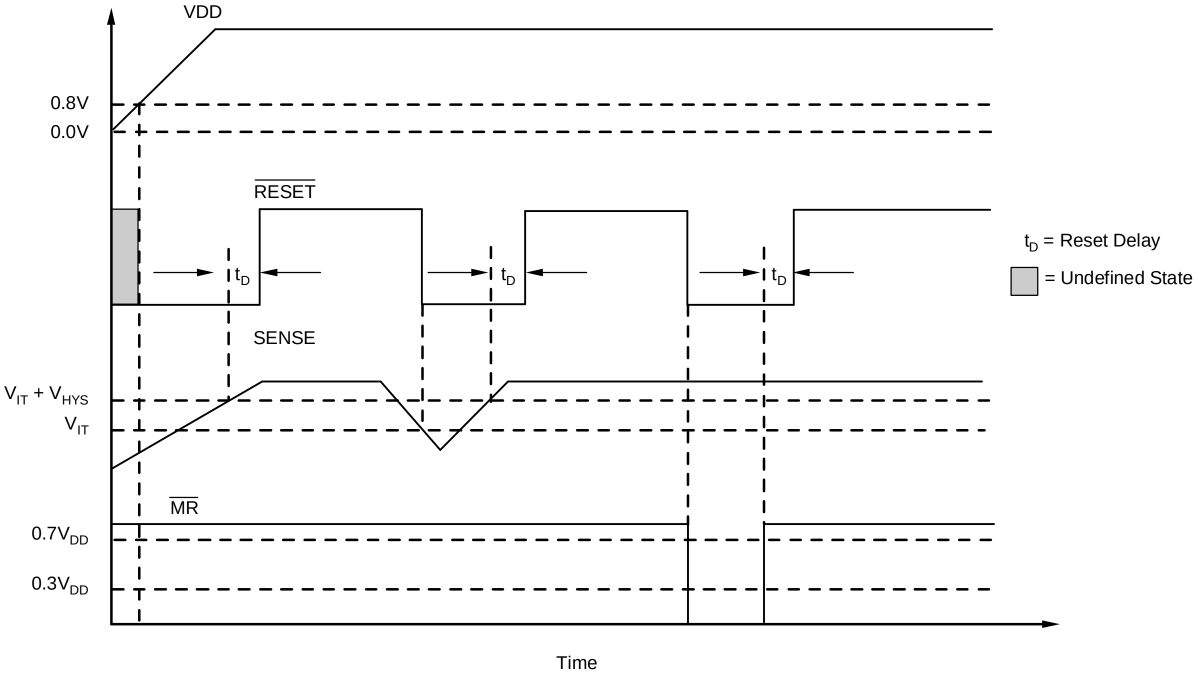


Figure 3. TPS3808 Timing Diagram Showing $\overline{\text{MR}}$ and SENSE Reset Timing

TRUTH TABLE

$\overline{\text{MR}}$	SENSE > V_{IT}	$\overline{\text{RESET}}$
L	0	L
L	1	L
H	0	L
H	1	H

TYPICAL CHARACTERISTICS

V_{DD} = 3.3V, T_J = 25°C, R_{LRESET} = 100kΩ, C_{LRESET} = 50pF

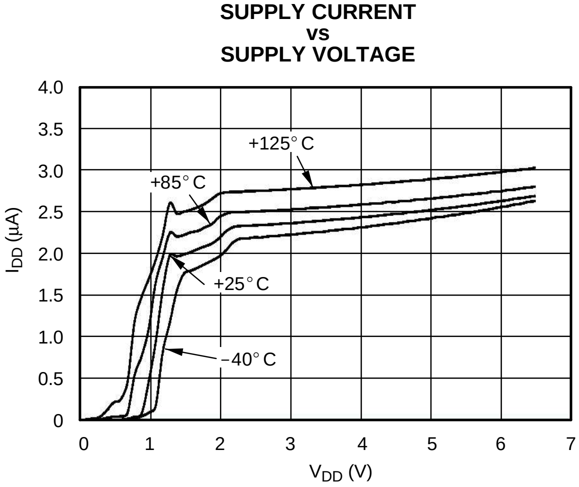


Figure 4.

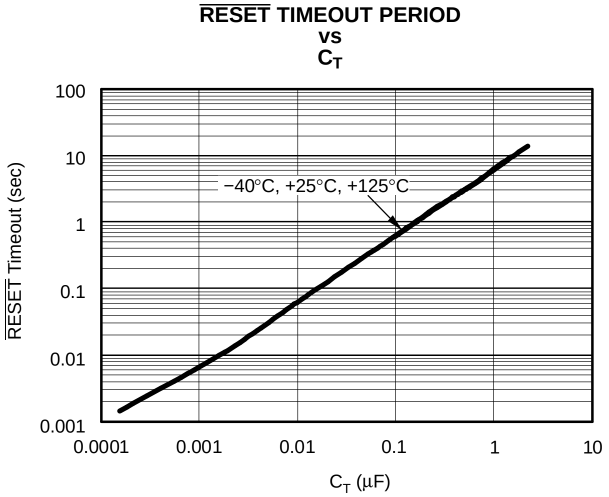


Figure 5.

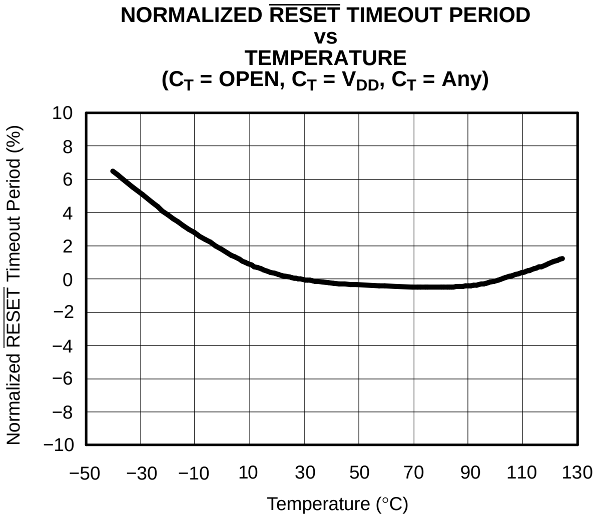


Figure 6.

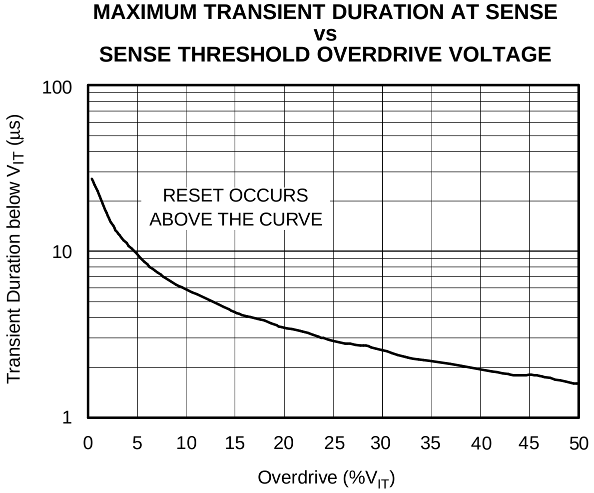


Figure 7.

TYPICAL CHARACTERISTICS (continued)

V_{DD} = 3.3V, T_J = 25°C, R_{LRESET} = 100kΩ, C_{LRESET} = 50pF

NORMALIZED SENSE THRESHOLD VOLTAGE (V_{IT})
vs
TEMPERATURE

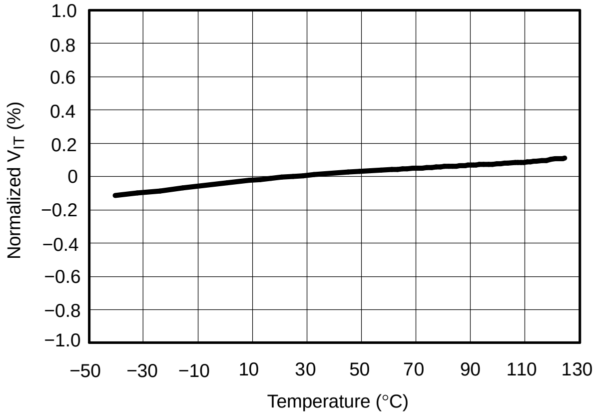


Figure 8.

LOW-LEVEL $\overline{\text{RESET}}$ VOLTAGE
vs
$\overline{\text{RESET}}$ CURRENT

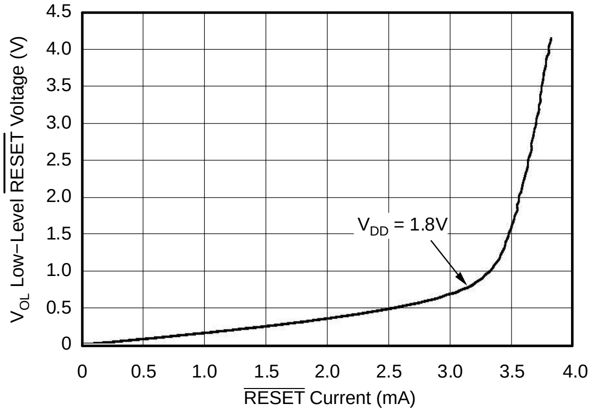


Figure 9.

LOW-LEVEL $\overline{\text{RESET}}$ VOLTAGE
vs
$\overline{\text{RESET}}$ CURRENT

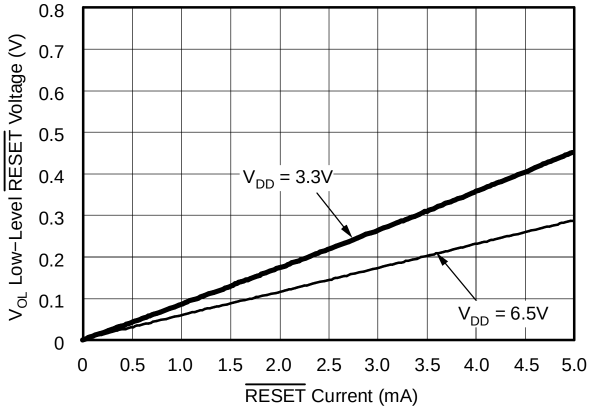


Figure 10.

DEVICE OPERATION

The TPS3808 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{IT} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above their thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the TPS3808G01 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the CT pin to V_{DD} results in a 300ms reset delay, while leaving the CT pin open yields a 20ms reset delay. In addition, connecting a capacitor between CT and GND allows the designer to select any reset delay period from 1.25ms to 10s.

RESET OUTPUT

A typical application of the TPS3808G25 used with the OMAP1510 processor is shown in Figure 11. The open drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pull-up resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below 0.8V, but this is normally not a problem since most microprocessors do not function below this voltage. $\overline{\text{RESET}}$ remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset ($\overline{\text{MR}}$) is logic high. If either SENSE falls below V_{IT} or $\overline{\text{MR}}$ is driven low, $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

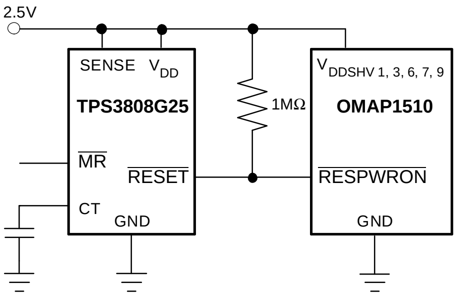


Figure 11. Typical Application of the TPS3808 with an OMAP Processor

Once $\overline{\text{MR}}$ is again logic high and SENSE is above V_{IT} + V_{hys} (the threshold hysteresis), a delay circuit is enabled which holds $\overline{\text{RESET}}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{\text{RESET}}$ pin goes to a high impedance state. The pull-up resistor from the open drain $\overline{\text{RESET}}$ to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6.5V). The pull-up resistor should be no smaller than 10kΩ as a result of the finite impedance of the $\overline{\text{RESET}}$ line.

SENSE INPUT

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808G01 can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure 12.

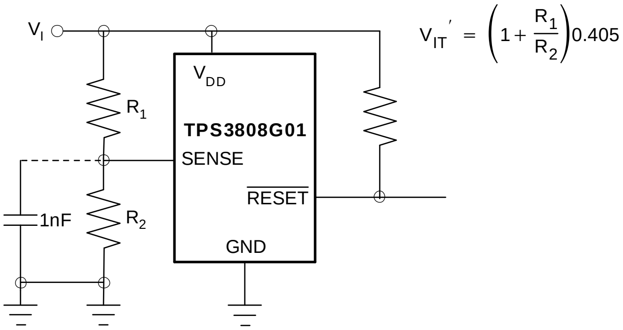


Figure 12. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage

MANUAL RESET ($\overline{\text{MR}}$) INPUT

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low ($0.3V_{DD}$) on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above its reset threshold, $\overline{\text{RESET}}$ is de-asserted after the user defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to V_{DD} using a 90k resistor so this pin can be left unconnected if $\overline{\text{MR}}$ will not be used.

Figure 13 shows how $\overline{\text{MR}}$ can be used to monitor multiple system voltages. Note that if the logic signal driving $\overline{\text{MR}}$ does not go fully to V_{DD}, there will be some additional current draw into V_{DD} as a result of the internal pull-up resistor on $\overline{\text{MR}}$. To minimize current draw, a logic-level FET can be used as shown in Figure 14.

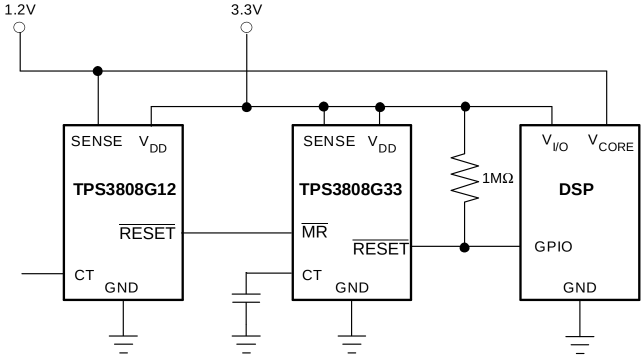


Figure 13. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages

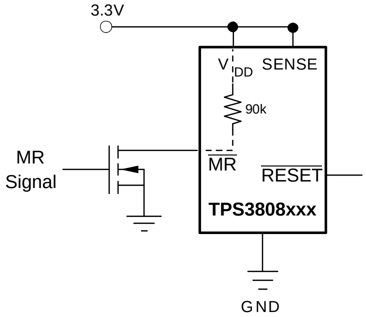


Figure 14. Using an External MOSFET to Minimize I_{DD} When $\overline{\text{MR}}$ Signal Does Not Go to V_{DD}

SELECTING THE RESET DELAY TIME

The TPS3808 has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure 15. Figure 15a shows the configuration for a fixed 300ms typical delay time by tying CT to V_{DD}; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected by the choice of resistor. Figure 15b shows a fixed 20ms delay time by leaving the CT pin open. Figure 15c shows a ground referenced capacitor connected to CT for a user-defined program time between 1.25ms and 10s.

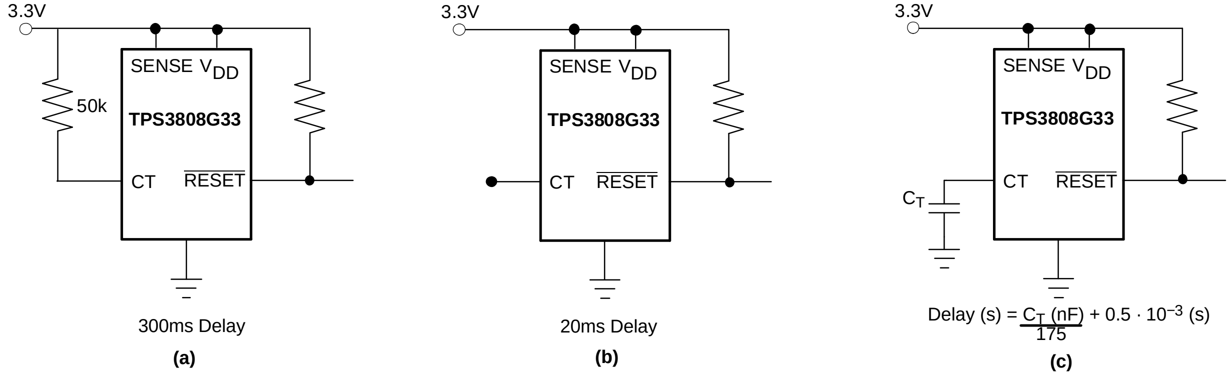
The capacitor CT should be ≥ 100pF nominal value in order for the TPS3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:

$$C_T\,(\text{nF}) = \left[t_D\,(\text{s}) - 0.5 \cdot 10^{-3}\,(\text{s})\right] \cdot 175 \qquad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a $\overline{\text{RESET}}$ is asserted the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V, $\overline{\text{RESET}}$ is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The TPS3808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph in the Typical Characteristics section.



300ms Delay
(a)

20ms Delay
(b)

$\text{Delay (s)} = \frac{C_T\,(\text{nF})}{175} + 0.5 \cdot 10^{-3}\,(\text{s})$
(c)

Figure 15. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time

PACKAGE OPTION ADDENDUM

26-Apr-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3808G01DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G09DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G09DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G09DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

PACKAGE OPTION ADDENDUM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS3808G30DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G50DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G50DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G50DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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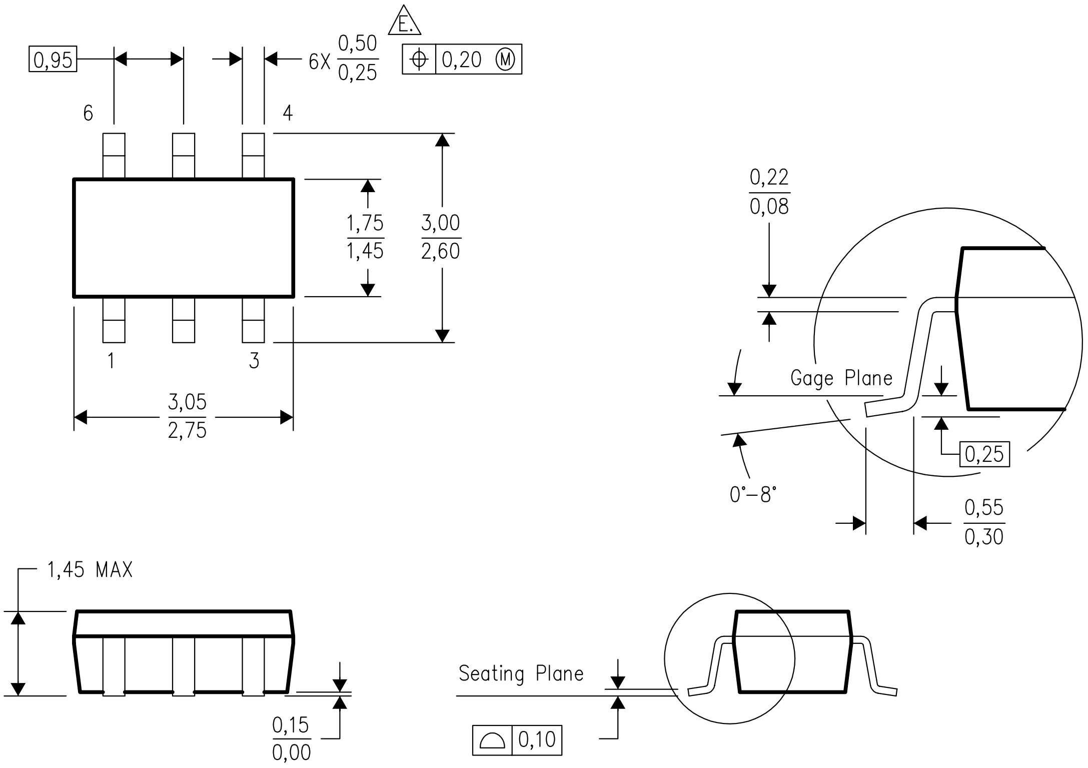
DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

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