

DS26C32AT/DS26C32AM Quad Differential Line Receiver

Check for Samples: [DS26C32AM](#), [DS26C32AT](#)

FEATURES

- **CMOS Design for Low Power**
- **$\pm 0.2\text{V}$ Sensitivity over Input Common Mode Voltage Range**
- **Typical Propagation Delays: 19 ns**
- **Typical Input hysteresis: 60 mV**
- **Inputs Won't Load Line When $V_{CC} = 0\text{V}$**
- **Meets the Requirements of EIA Standard RS-422**
- **TRI-STATE Outputs for Connection to System Buses**
- **Available in Surface Mount**
- **Mil-Std-883C Compliant**

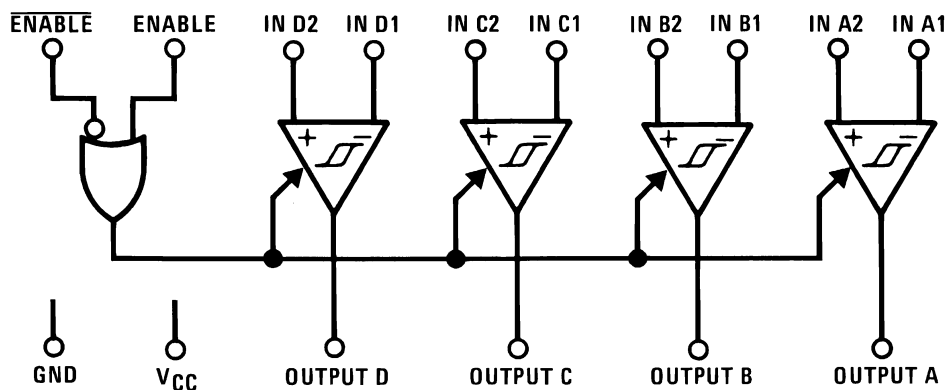
DESCRIPTION

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of $\pm 7\text{V}$. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers. It also features TRI-STATE outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

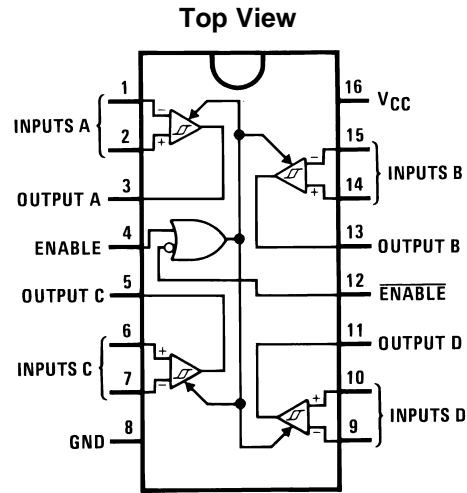
Logic Diagram



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Connection Diagrams



For Complete Military Product Specifications, refer to the appropriate SMD or MDS.

Figure 1. PDIP Package
 See Package Number D0016A or NFG0016E
 See Package Number NAJ0020A, NFE0016A or NAD0016A

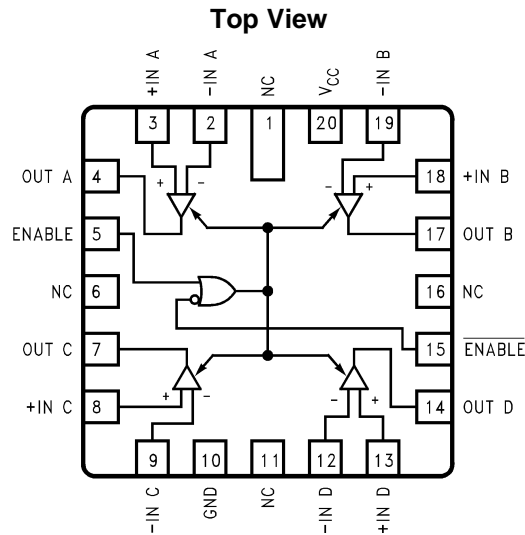


Figure 2. 20-Lead Ceramic Leadless Chip Carrier LCCC Package



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	$\pm 14V$
Differential Input Voltage (V_{DIFF})	$\pm 14V$
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering 4 sec.)	$260^{\circ}C$
Maximum Power Dissipation at $25^{\circ}C$ ⁽⁴⁾	
Ceramic NFE0016A Package	2308 mW
Plastic NFG0016E Package	1645 mW
SOIC D0016A Package	1190 mW
Ceramic NAJ0020A Package	2108 mW
Ceramic NAD0016A Package	1215 mW
Maximum Current Per Output	± 25 mA
This device does not meet 2000V ESD rating. ⁽⁵⁾	

- (1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
- (2) Unless otherwise specified, all voltages are referenced to ground.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications
- (4) Ratings apply to ambient temperature at $25^{\circ}C$. Above this temperature derate N Package 13.16 mW/ $^{\circ}C$, J Package 15.38 mW/ $^{\circ}C$, M Package 9.52 mW/ $^{\circ}C$, E Package 12.04 mW/ $^{\circ}C$, and W package 6.94 mW/ $^{\circ}C$.
- (5) ESD Rating: HBM (1.5 k Ω , 100 pF) Inputs $\geq 2000V$ All other pins $\geq 1000V$ EIAJ (0 Ω , 200 pF) $\geq 350V$

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS26C32AT	-40	+85	$^{\circ}C$
DS26C32AM	-55	+125	$^{\circ}C$
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics
 $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)⁽¹⁾

Parameter		Test Conditions	Min	Typ	Max	Units	
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	-200	35	+200	mV	
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	DS26C32AT	5.0	6.8	10	k Ω
			DS26C32AM	4.5	6.8	11	k Ω
I_{IN}	Input Current	$V_{IN} = +10V,$ Other Input = GND	DS26C32AT	+1.1	+1.5	mA	
			DS26C32AM	+1.1	+1.8	mA	
		$V_{IN} = -10V,$ Other Input = GND	DS26C32AT	-2.0	-2.5	mA	
			DS26C32AM	-2.0	-2.7	mA	
V_{OH}	Minimum High Level Output Voltage	$V_{CC} = \text{Min}, V_{DIFF} = +1V$ $I_{OUT} = -6.0$ mA	3.8	4.2		V	
V_{OL}	Maximum Low Level Output Voltage	$V_{CC} = \text{Max}, V_{DIFF} = -1V$ $I_{OUT} = 6.0$ mA		0.2	0.3	V	
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V	
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V	

- (1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics (continued) $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)⁽¹⁾

Parameter		Test Conditions	Min	Typ	Max	Units
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{ENABLE} = V_{IL}$, $ENABLE = V_{IH}$		± 0.5	± 5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			± 1.0	μA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max}$,	DS26C32AT	16	23	mA
		$V_{DIF} = +1V$	DS26C32AM	16	25	mA
V_{HYST}	Input Hysteresis	$V_{CM} = 0V$		60		mV

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ ⁽¹⁾

Parameter	Test Conditions	Min	Typ	Max		Units	
				DS26C32AT	DS26C32AM		
t_{PLH} , t_{PHL}	Propagation Delay Input to Output	$C_L = 50 \text{ pF}$	10	19	30	35	ns
		$V_{DIFF} = 2.5V$					
		$V_{CM} = 0V$					
t_{RISE} , t_{FALL}	Output Rise and Fall Times	$C_L = 50 \text{ pF}$		4	9	9	ns
		$V_{DIFF} = 2.5V$					
		$V_{CM} = 0V$					
t_{PLZ} , t_{PHZ}	Propagation Delay ENABLE to Output	$C_L = 50 \text{ pF}$		13	22	29	ns
		$R_L = 1000\Omega$					
		$V_{DIFF} = 2.5V$					
t_{PZL} , t_{PZH}	Propagation Delay ENABLE to Output	$C_L = 50 \text{ pF}$		13	23	29	ns
		$R_L = 1000\Omega$					
		$V_{DIFF} = 2.5V$					

(1) Unless otherwise specified, Min/Max limits apply over recommended operating conditions. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ C$.

Comparison Table of Switching Characteristics into “LS-Type” Load(Figure 6, Figure 7, and Figure 8) ⁽¹⁾

Parameter	Test Conditions	DS26C32A	DS26LS32A	Units
		Typ	Typ	
t_{PLH}	Input to Output	17	23	ns
t_{PHL}				
t_{LZ}	ENABLE to Output	13	15	ns
t_{HZ}				
t_{ZL}	ENABLE to Output	13	14	ns
t_{ZH}				

(1) This table is provided for comparison purposes only. The values in this table for the DS26C32A reflect the performance of the device, but are not tested.

TEST AND SWITCHING WAVEFORMS

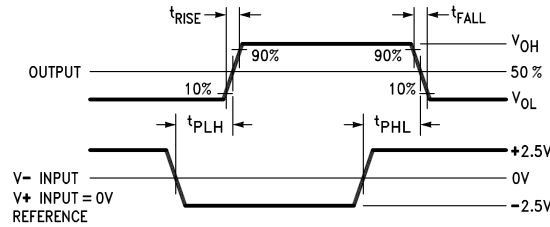
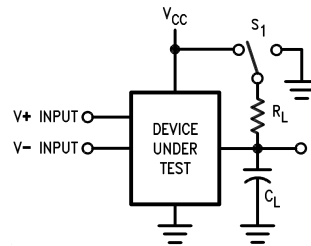


Figure 3. Propagation Delay



C_L includes load and test jig capacitance.
 S₁ = V_{CC} for t_{PZL} and t_{PLZ} measurements.
 S₁ = Gnd for t_{PZH} and t_{PHZ} measurements.

Figure 4. Test Circuit for TRI-STATE Output Tests

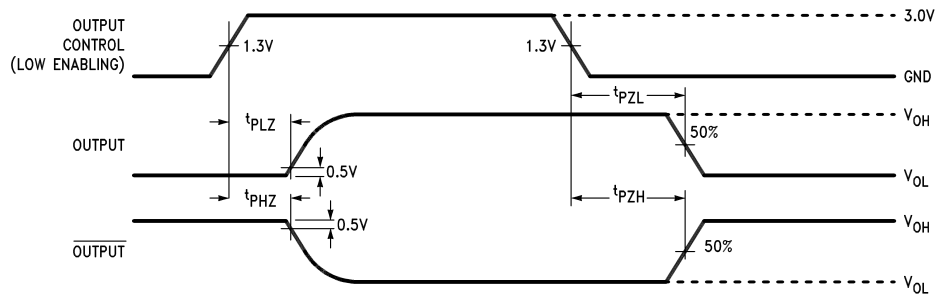


Figure 5. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuit and Switching Time Waveforms

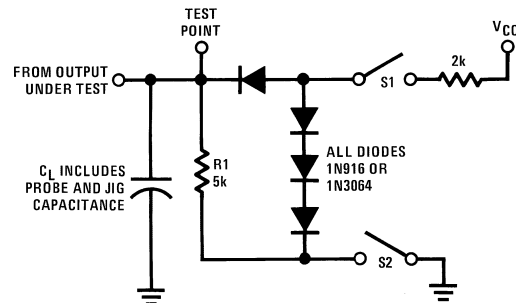


Figure 6. Load Test Circuit for TRI-STATE Outputs for "LS-Type" Load

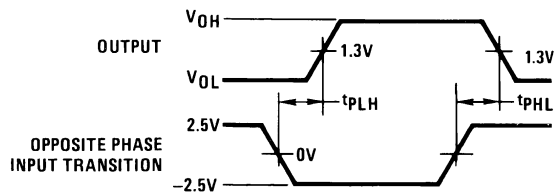
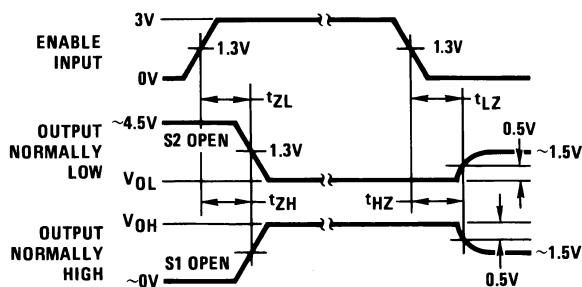


Figure 7. Propagation Delay for “LS-Type” Load



- (1) Diagram shown for $\overline{\text{ENABLE}}$ low.
- (2) S1 and S2 of load circuit are closed except where shown.
- (3) Pulse generator for all pulses: Rate ≤ 1.0 MHz; $Z_0 = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

Figure 8. Enable and Disable Times for “LS-Type” Load

Truth Table⁽¹⁾

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{TH} (\text{Max})$	H
		$V_{ID} \leq V_{TH} (\text{Min})$	L
		Open	H

(1) Z = TRI-STATE

TYPICAL APPLICATIONS

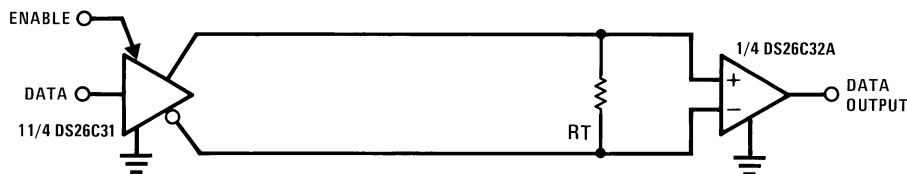


Figure 9. Two-Wire Balanced Systems, RS-422

Typical Performance Characteristics

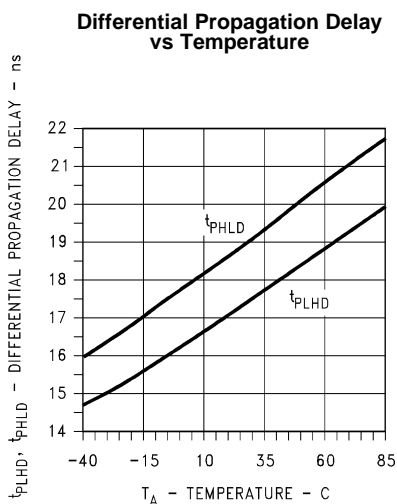


Figure 10.

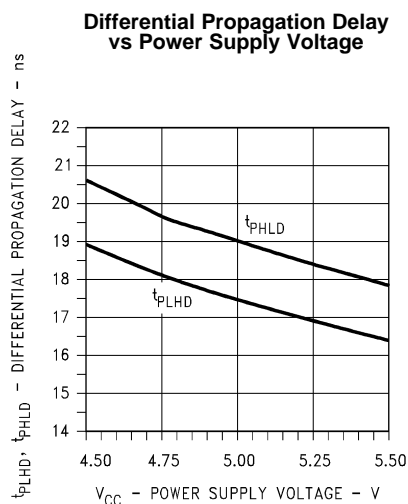


Figure 11.

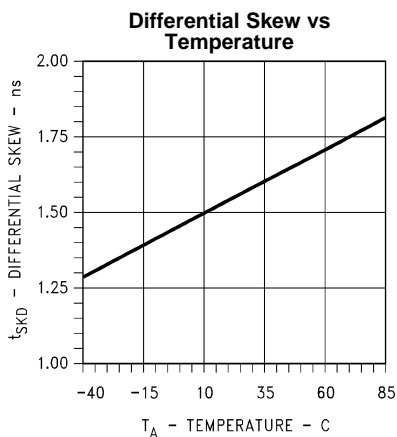


Figure 12.

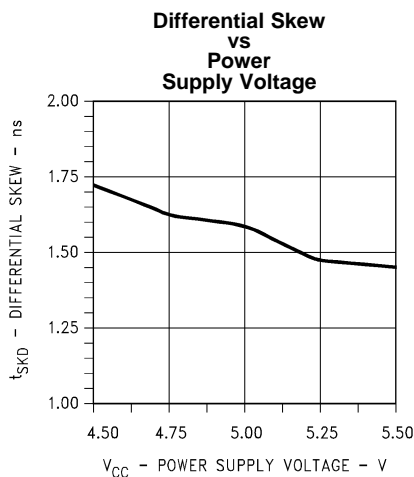


Figure 13.

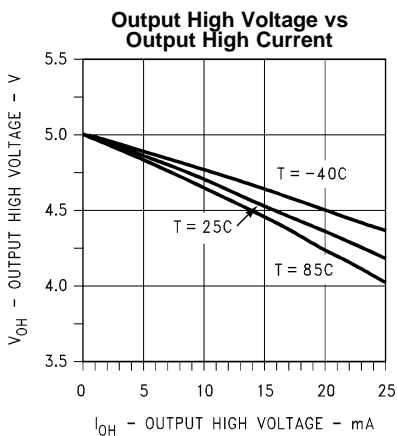


Figure 14.

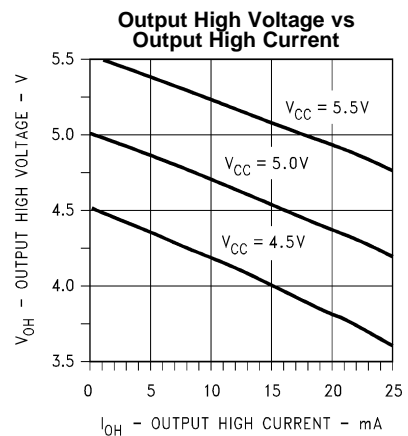


Figure 15.

Typical Performance Characteristics (continued)

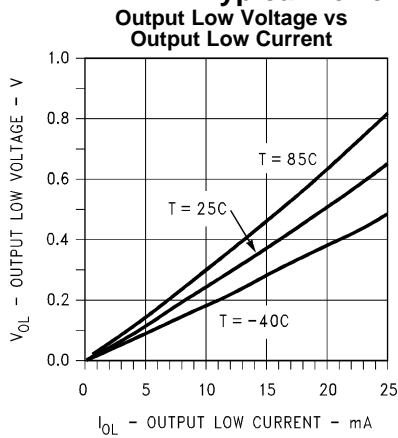


Figure 16.

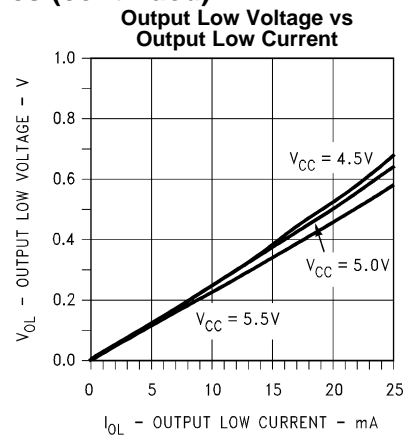


Figure 17.

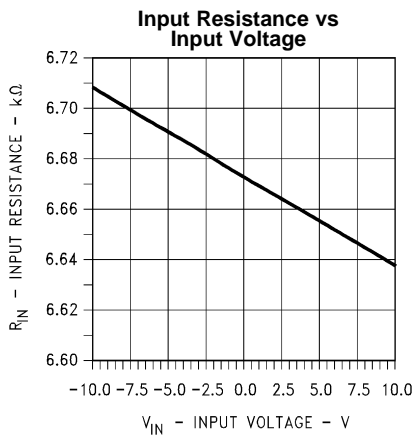


Figure 18.

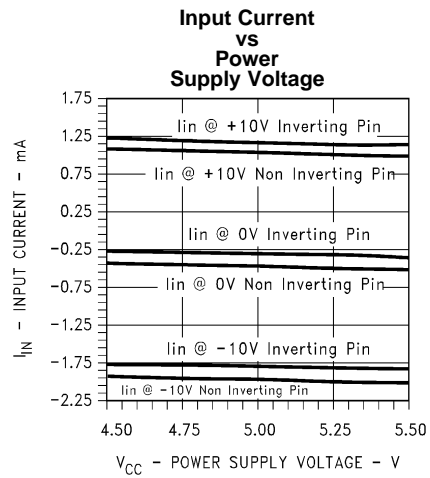


Figure 19.

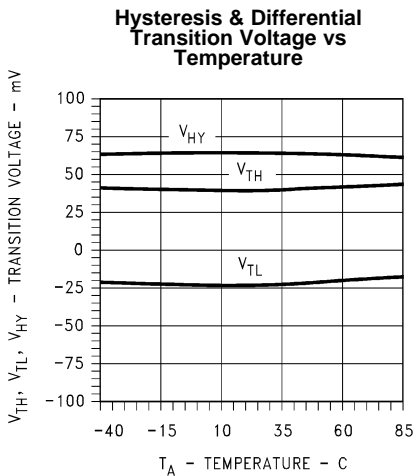


Figure 20.

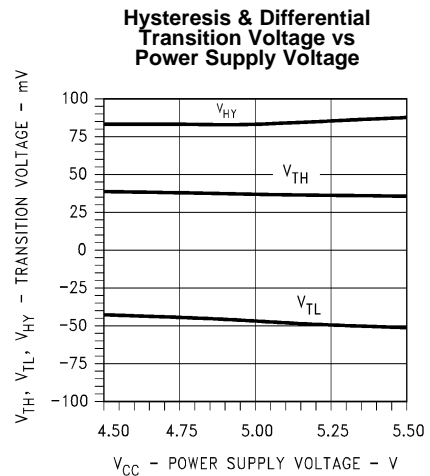


Figure 21.

Typical Performance Characteristics (continued)

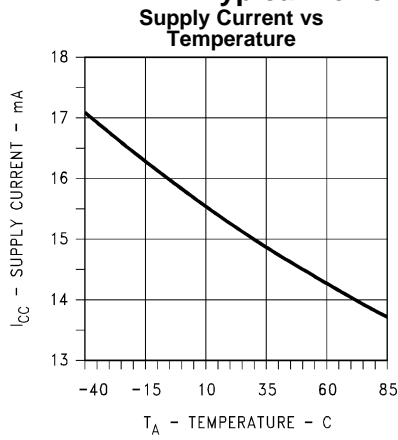


Figure 22.

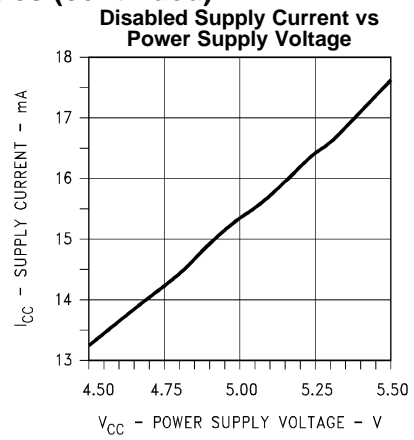


Figure 23.

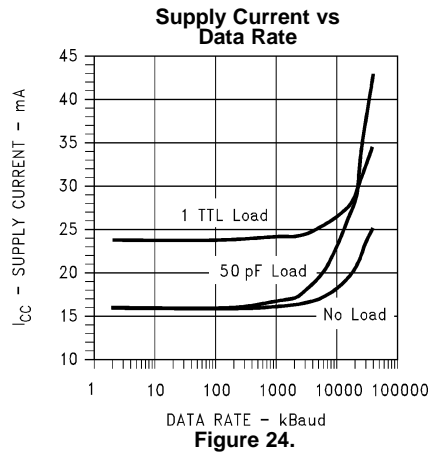


Figure 24.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26C32ATM	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS26C32ATM	Samples
DS26C32ATM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	SN CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C32ATM	Samples
DS26C32ATMX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS26C32ATM	Samples
DS26C32ATMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C32ATM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26C32ATMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS26C32ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26C32ATMX	SOIC	D	16	2500	367.0	367.0	35.0
DS26C32ATMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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