TPS62730 Stepdown Converter With Bypass Mode for Ultralow-Power Wireless Applications

This user's guide describes the TPS62730 evaluation module (EVM), how to perform a stand-alone evaluation or interface with a host or system. The converter is designed to deliver up to 100 mA of continuous current to the output. The converter can be switched into bypass mode by grounding the ON/BYP pin or automatically with the input voltage falling to the output regulation voltage.

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1 Introduction

The TPS62730 device is a high-frequency synchronous stepdown dc-dc converter optimized for ultralow-power wireless applications. The device is optimized to supply TI's low-power wireless sub-1-GHz and 2.4-GHz RF transceivers. The TPS62730 reduces the current consumption drawn from the battery during TX and RX modes by a highly efficient stepdown voltage conversion. It provides up to 100-mA output current and allows the use of tiny and low-cost chip inductors and capacitors. This device supports most Li-ion primary battery chemistries, with an input range of 1.9 V to 3.9 V dc.

The TPS62730 features an ultralow-power bypass mode with a typical 30 nA current consumption to support low-power modes of modern RF transceivers. In this bypass mode, the input is connected the VOUT pin via an internal 2-Ω bypass FET.

The device automatically enters bypass mode when the input (battery) voltage falls to the bypass transition threshold.

2 Considerations With Evaluating the TPS62730

This part has two modes of operation, the switching buck mode and the dc bypass mode. The IC automatically shuts down the switcher once the input voltage drops to the bypass threshold, which is a few millivolts above the regulation voltage, saving on bias power to the switcher.

Bypass mode can be implemented at higher input voltages by pulling the ON/BYP pin low. There may be some applications where the input voltage is too high for the system, and caution should be taken that this mode transfer is not performed for these cases. The ON/BYP pin should not be floated (open), or it is highly likely that the IC will be in an unknown state/mode and the output voltage could be anywhere between the input voltage and the regulation voltage.

The EVM has a pullup resistor on the ON/BYP pin to Vin so that it stays in the switching mode if the jumper is removed and only goes into the bypass mode if the shunt is moved to ground the ON/BYP pin.

This pullup resistor on the EVM causes the input to be loaded, when in bypass mode, by Vin/1 MΩ. In a typical application, a driver controls the ON/BYP pin and does not load the input; thus, this current should not be considered in the quiescent current when in bypass mode.

The pullup resistor for the status output on the EVM should also be considered (ignored) when calculating the efficiency of the converter. The EVM uses a *stiff* pullup, because it is not known what will be connected to the STAT pin, but when designing the system a much higher-value resistor may be appropriate.

3 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	UNIT
Input dc voltage, Vin	Recommended input voltage range	1.9		3.9	V
Reduced performance, Vin[(1)]	Input voltage too low to maintain output regulation	1.9		2.1	V

(1) As the output load increases from 0 mA to 100 mA, the input voltage should be > 2.2 V to avoid dropout and maintain regulation.

4 Test Summary

The TPS62730EVM-726 board requires an adjustable 5-V, ≥150-mA current-limited power source to provide input power and a resistive load between 100 Ω and 21 Ω. The test setup connections and jumper-setting selections are configured for a stand-alone evaluation, but can be changed to interface with external hardware such as a system load and microcontroller.

4.1 Equipment

- Adjustable dc power supply between 1.8 V and 4 V with adjustable current limit set to ~150 mA
- Load: system load or resistive load ≥ 21 Ω
- Three Fluke 75 DMMs (equivalent or better)
- Oscilloscope, model TDS222 (equivalent or better)

4.2 Equipment and EVM Setup

Table 1. Setup I/O Connections and Configuration for Evaluation of TPS62730 EVM

Jack/Component (Silk Screen)	Connect or Adjustment To:
J1-1/2 (Vin)	Power supply positive lead, preset to 3.3 VDC, 150-mA current limit
J2-1 (+ SNS); input	Positive lead of DMM #1
J2-2 (- SNS); input	Negative lead of DMM #1
J3-1/2 (GND)	Power supply negative lead (3.3 VDC supply)
J4-1/2 (Vout)	Positive lead to system load or load resistance
J5-1 (+ SNS); output	Positive lead of DMM #2
J5-2 (- SNS); output	Negative lead of DMM #2
J6-1/2 (GND)	Negative lead to system load or load resistance
J7-1 (STAT)	Positive lead of DMM meter #3
J7-2 (GND)	Negative lead of DMM meter #3
JP1-1/2 (ON)	Apply shunt to ON for converter operation
JP1-2/3 (Bypass)	Do not apply shunt until procedures calls for change.

Connect the meters, scope probes, output load, shunt, and input power supply as listed in Table 1 and set scope to 200 ns/div, positive trigger, dc-coupled on CH1, CH2: ac-coupled and 10 mV/div. Additional channels can be added or probes can be moved to view Vin, Vstat and Vbypass. The resistive load can be replaced with a system load or decade load box to vary the load between 1 kΩ and 21 Ω.

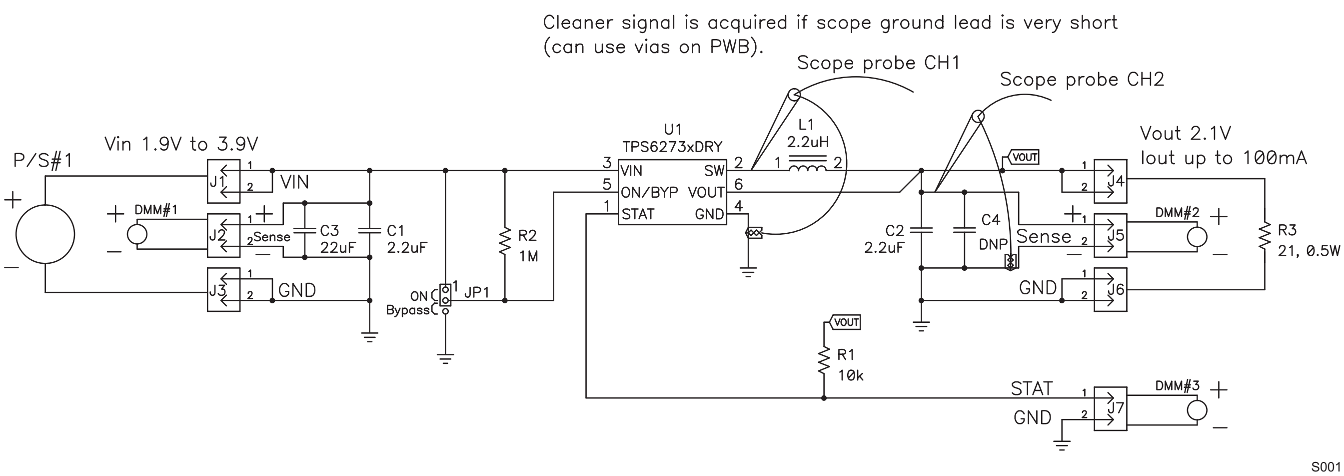

Figure 1. EVM Schematic and Evaluation Setup

4.3 Test Procedure Using a Single Cell Li-Ion Battery

1. Make sure that the EVM is set up according to Table 1 and Figure 1, and that the power supply is preset to 3.3 VDC at ~150 mA current limit.
2. Turn on the input supply and verify the input voltage is ~3.3 VDC (DMM#1) and the output voltage is at ~2.1 VDC (DMM#2).
3. Look at CH1 and CH2 and verify that the duty cycle is near 70% and the ripple is less than 10-mV ripple; see Figure 6 for typical waveforms.
4. Vary the load between 0 and 100 mA (1 kΩ to 21 Ω). Observe the change in the switching waveform from PFM with discontinuous ringing to PWM mode. It may be necessary to change the time scale on the scope to 1 µs/div for light loads. See Figure 7 and Figure 8 for various loads. Set the load back to approximately 21 Ω.
5. Vary the input voltage from 3.3 VDC to 3.9 VDC and back to 2.4 VDC to see the change in duty cycle.
6. Reduce the input voltage from 2.4 VDC to 1.9 VDC and verify that the switcher automatically goes into bypass mode, disabling the switcher and turning on the internal bypass FET. The output should be the input voltage minus the IR drop across the pass FET (~2 Ω). The STAT pin should go to the high-impedance state and be pulled to the output voltage. Figure 9 was captured by moving CH2 to the J7-STAT relative to ground, 1 V/div, dc-coupled, setting the time scale to 50 µs/div (a slower time scale may be required, depending on power-supply decay), single-sequence trigger on CH2, and removing input power. The phase node is shown going into PFM, then disabling switching, and then indicating bypass mode by the STAT pin being pulled up to the output voltage (~2.2 VDC).

CAUTION

The following step disables the buck converter and switches the input voltage to the output. Make sure the maximum system input voltage is not exceeded by this step or the later steps that place the JP1 shunt in the bypass position.

7. Move the shunt on jumper JP1 from the ON position to the Bypass position. Notice that the switcher is disabled and the input voltage is switched to the output via the bypass switch. The output should be the input voltage minus the IR drop across the pass FET (~2 ohms). The STAT pin should go to the high-impedance state and be pulled to the output voltage. Move the shunt on jumper JP1 to the ON position.
8. For steps 9 through 13, one can view the figure and determine how scope was set up.
9. See Figure 10 for the transition from converter switch mode to bypass mode by pulling the ON/BYP pin low.
10. Remove the bypass jumper to see transition from bypass mode to converter switch mode; see Figure 11.
11. See Figure 12 for typical hot-plug power up.
12. See Figure 13 for the transient output load step from 50 mA to 100 mA.
13. See Figure 14 for the transient output load step from 100 mA to 50 mA.

5 Schematic, Physical Layouts and Bill of Materials

5.1 Schematic

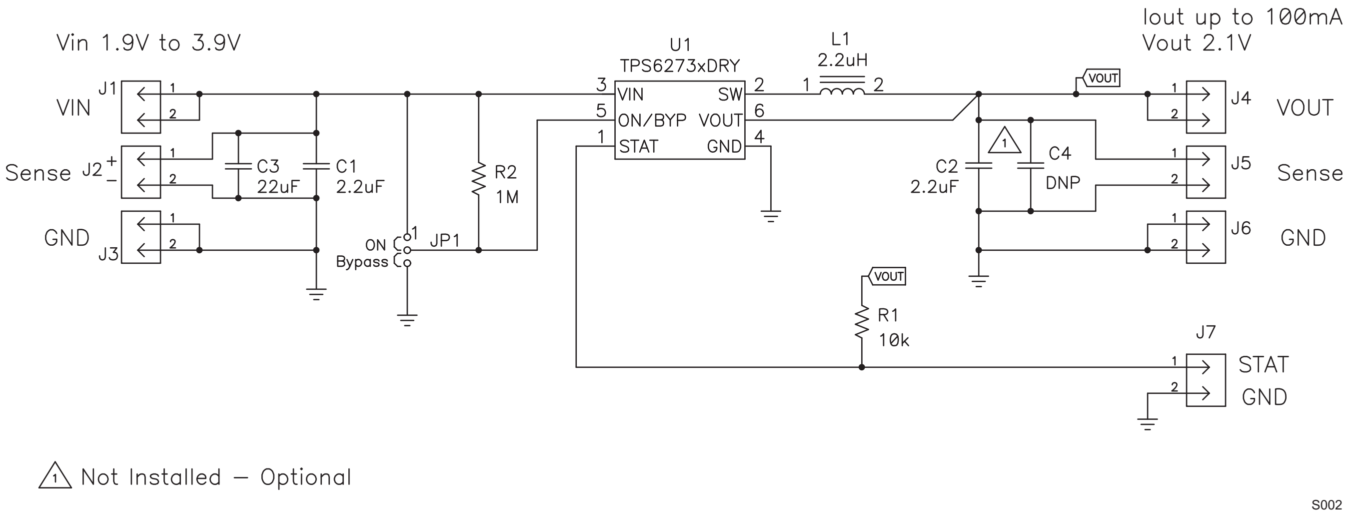

Figure 2. TPS62730 EVM Board Schematic

5.2 Physical Layouts

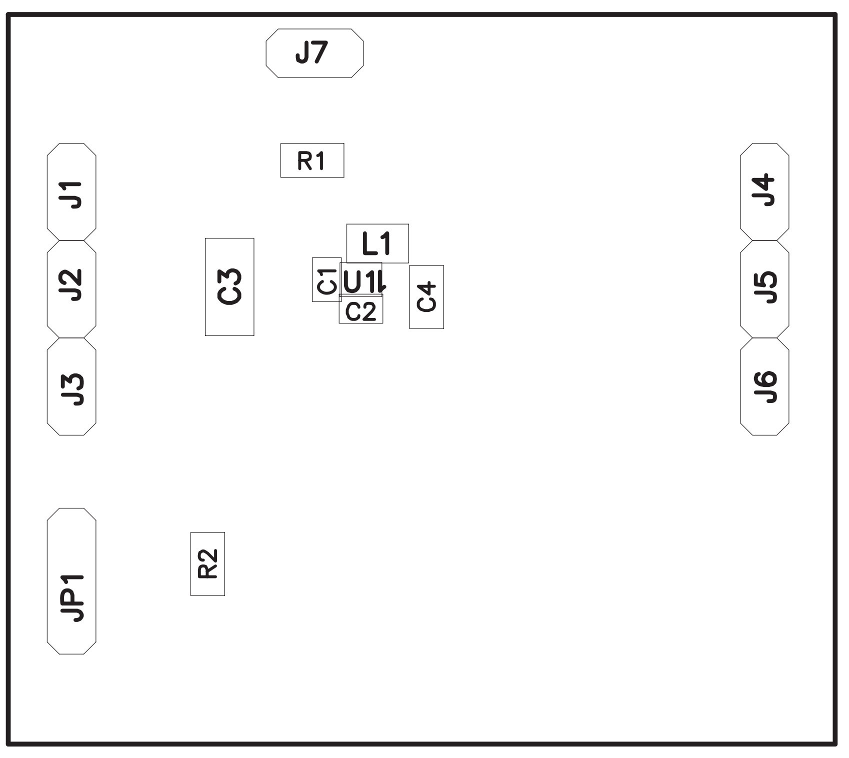

Figure 3. Assembly Layer

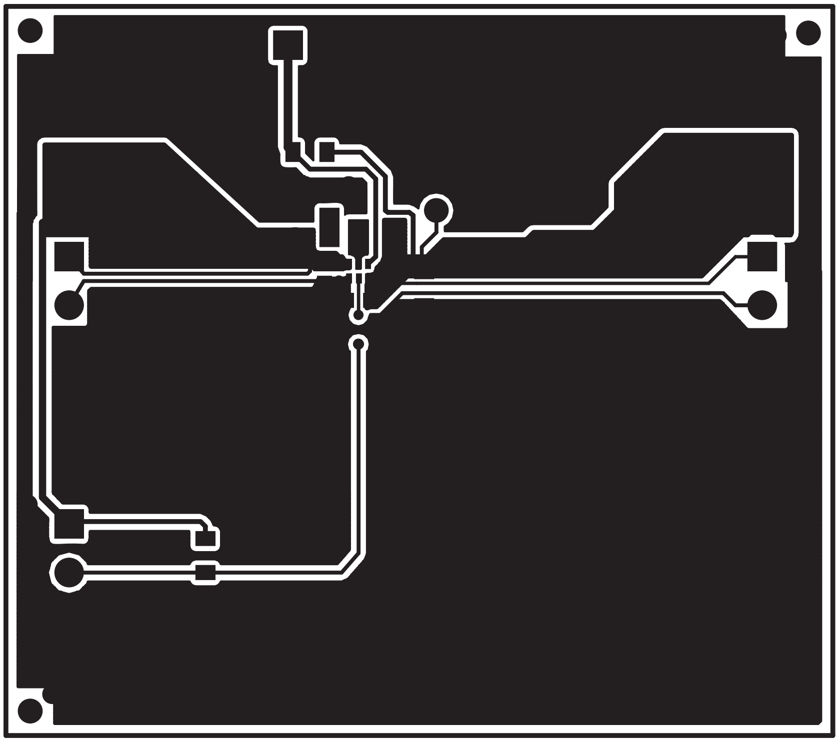

Figure 4. Top Layer

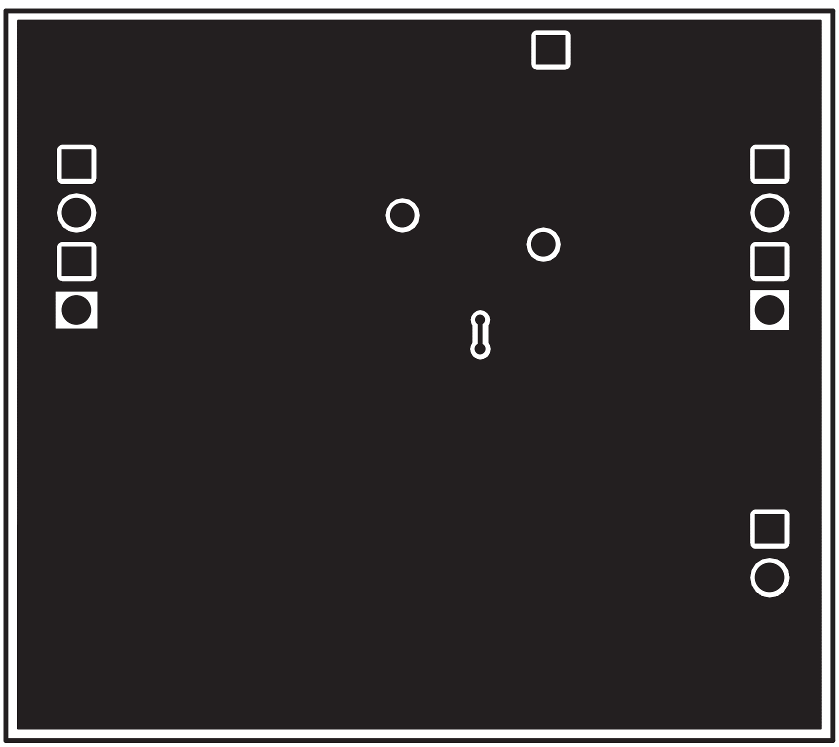

Figure 5. Bottom Layer

5.3 Bill of Materials

Table 2. HPA726A Bill of Materials

Count -001	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	2.2 µF	Capacitor, ceramic, 6.3-V, X5R, 20%	0402	GRM155R60J225ME15D	muRata
1	C3	22 µF	Capacitor, ceramic, 16-V, X5R, 10%	0603	ECJ-1VB1A225K	Panasonic
0	C4		Capacitor, ceramic, 6.3-V, X5R, 20%	0603	Std	Std
7	J1, J2, J3, J4, J5, J6, J7	PEC02SAAN	Header, male 2-pin, 100-mil (2,54-mm) spacing	0.100 inch (2,54-mm) × 2	PEC02SAAN	Sullins
1	JP1	PEC03SAAN	Header, 3-pin, 100-mil (2,54-mm) spacing	0.100 inch (2,54-mm) × 3	PEC02SAAN	Sullins
1	L1	2.2 µH	Inductor, SMT, 0.8-A, 0.23-Ω	0805	LQM21PN2R2NGC	muRata
1	R1	10.0 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R2	1.00 MΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS62730DRY	IC, step-down converter with bypass mode for low-power wireless	1,5 mm × 1 mm	TPS62730DRY	TI
1	–		PCB, 1.7 in. × 1.5 in. x 0.031 in. (4,32 cm × 3,81 cm × 0,787 mm)		HPA726	Any
1	Apply on: JP1-ON		Shunt, 100-mil (2,54-mm), black	0.1 in (2,54-mm)	929950-00	3M

6 Oscilloscope Traces

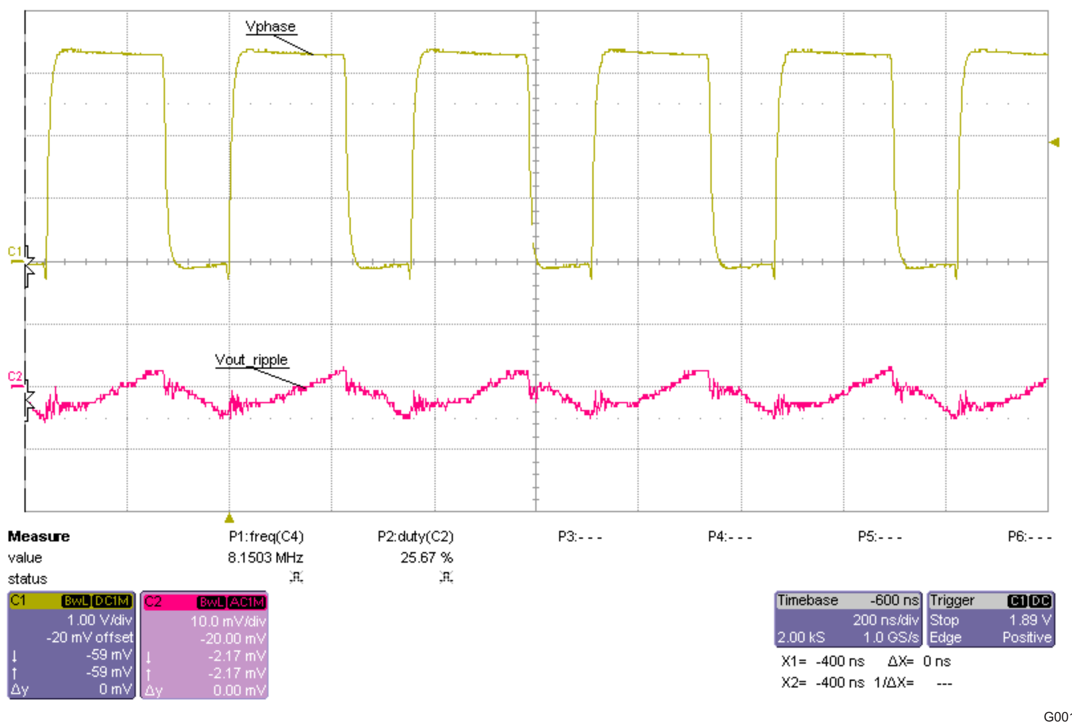

Figure 6. CH1: Phase; CH2: Output Ripple, Vin = 3.3 V, and 21-Ω Load

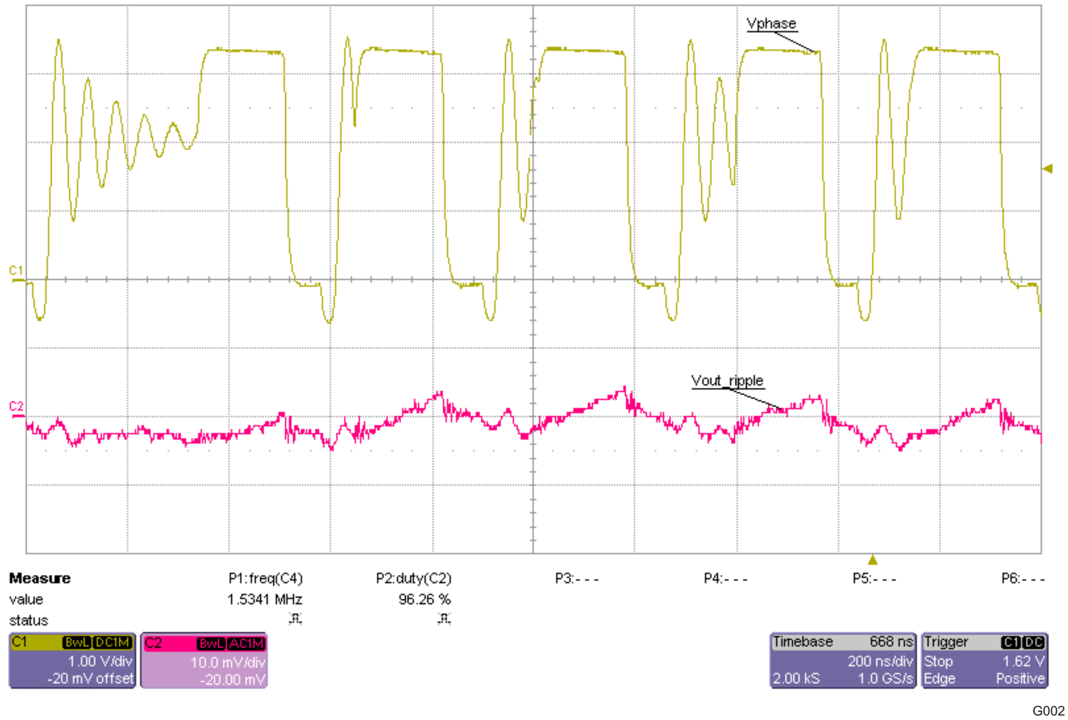

Figure 7. PFM Mode at Low Load, 40 mA – CH1: Phase; CH2: Output Ripple; 0.2 μs/div

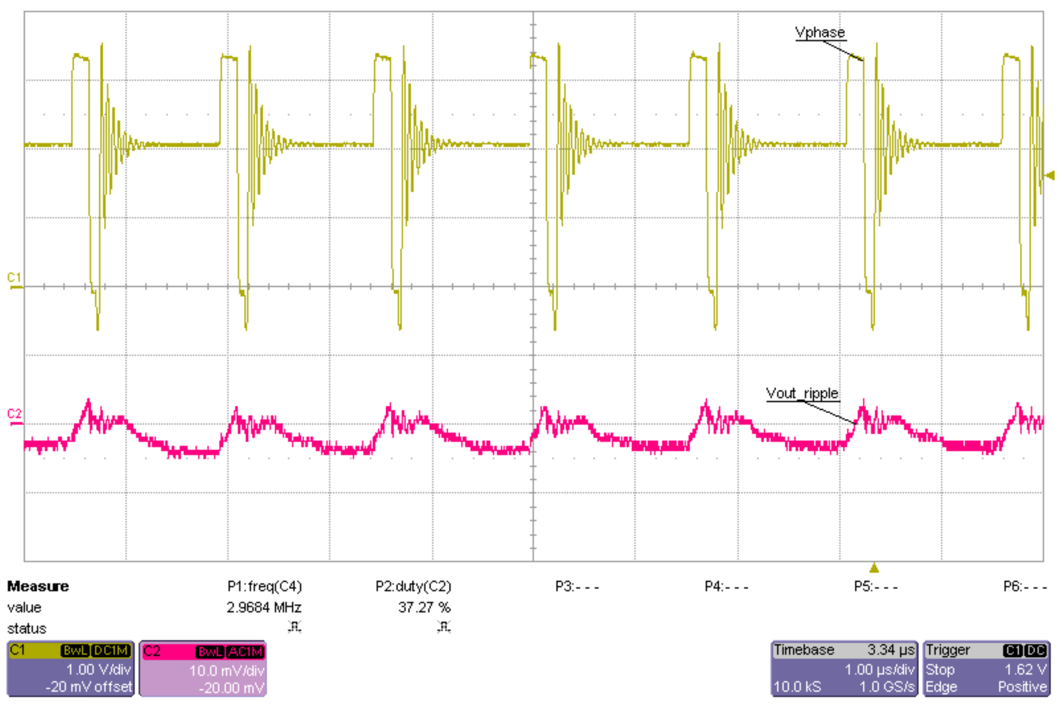

Figure 8. PFM Mode at Low Load, 11 mA – CH1: Phase; CH2: Output Ripple; 1 μs/div

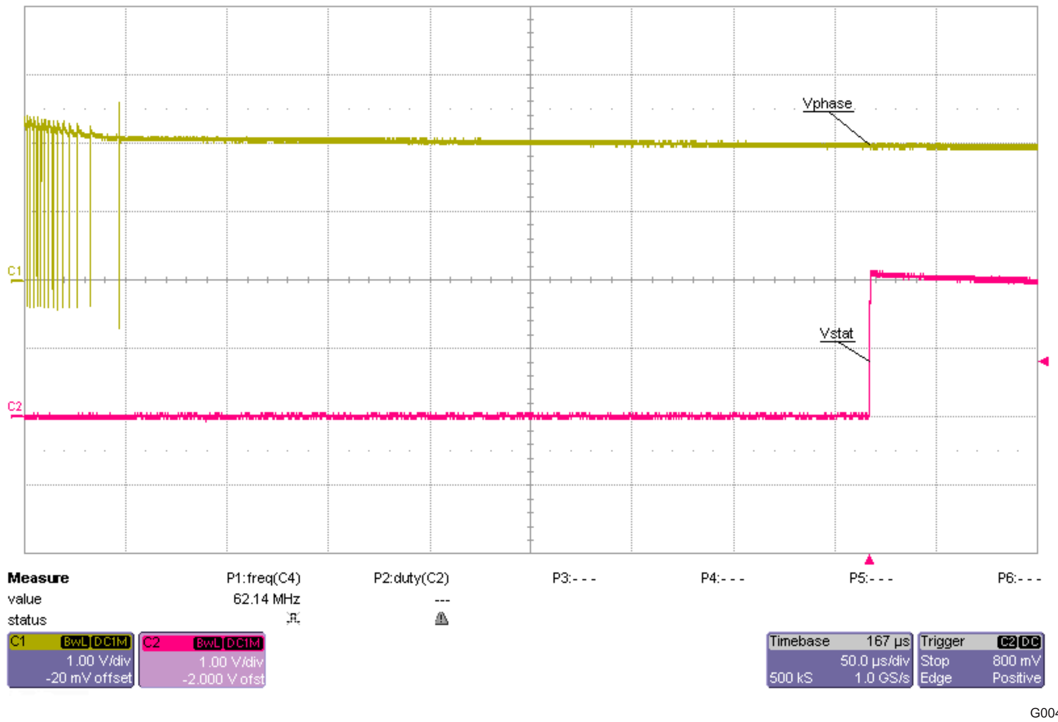

Figure 9. Transition From Switching Converter to Bypass Mode by Removing Input Power – CH1: Phase Node; CH2: STAT Pin

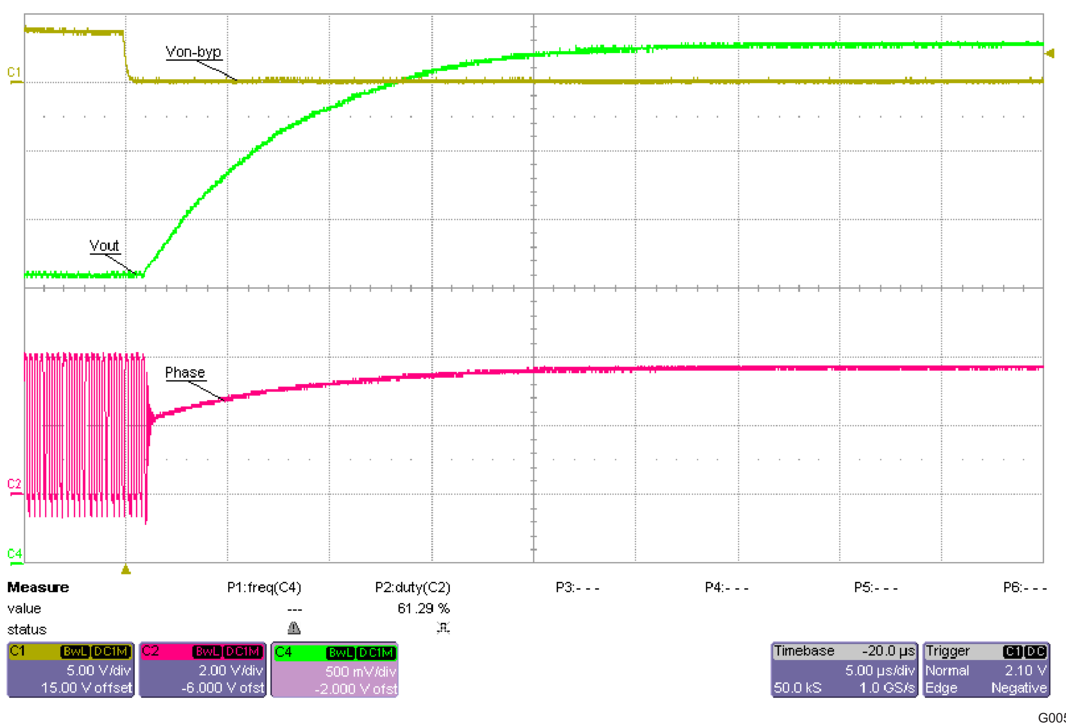

Figure 10. Transition From Converter Switch Mode to Bypass Mode by Pulling ON/BYP Pin Low

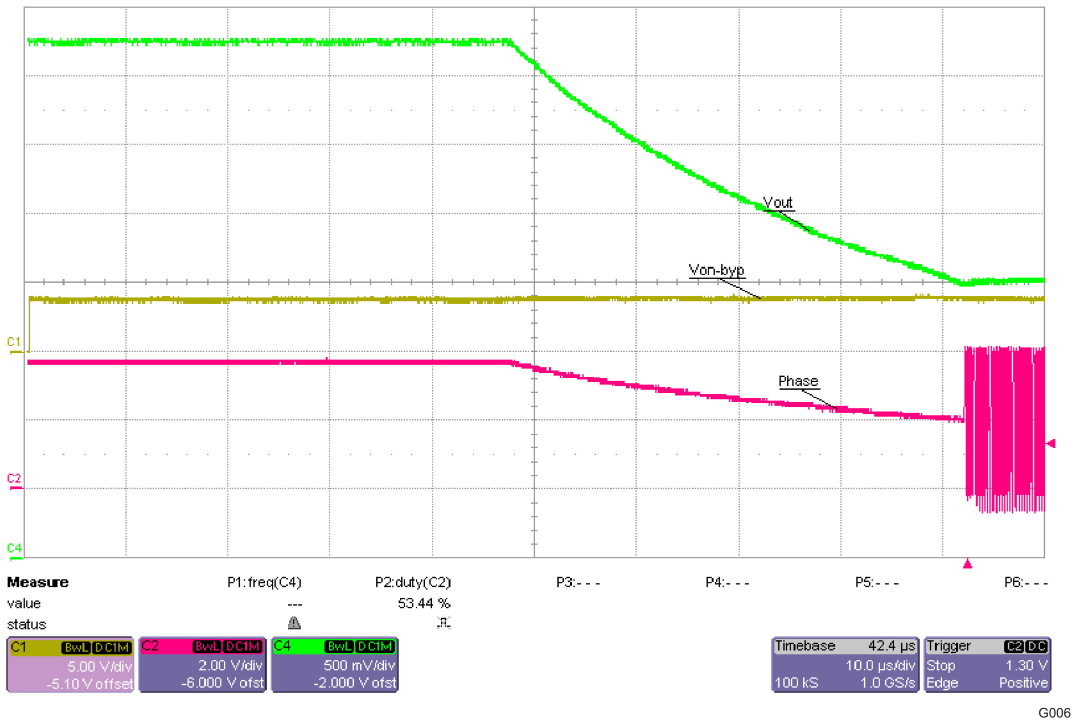

Figure 11. Transition From Bypass Mode to Converter Switch Mode by Pulling ON/BYP Pin High

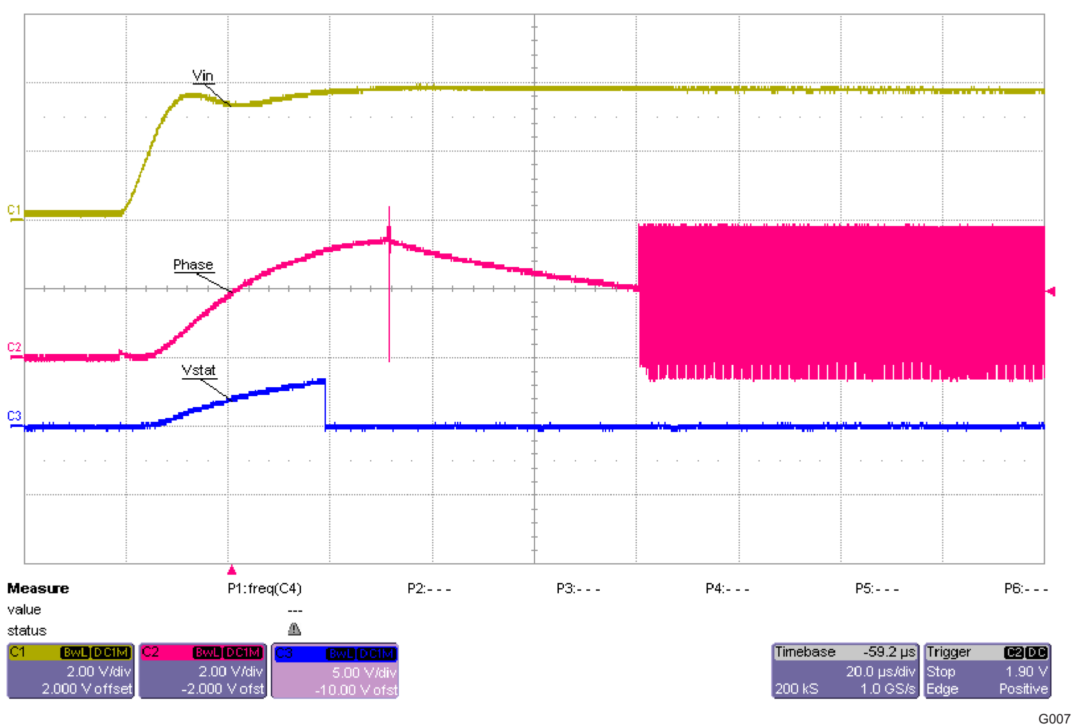

Figure 12. Startup by Hot-Plugging the Input Power Source

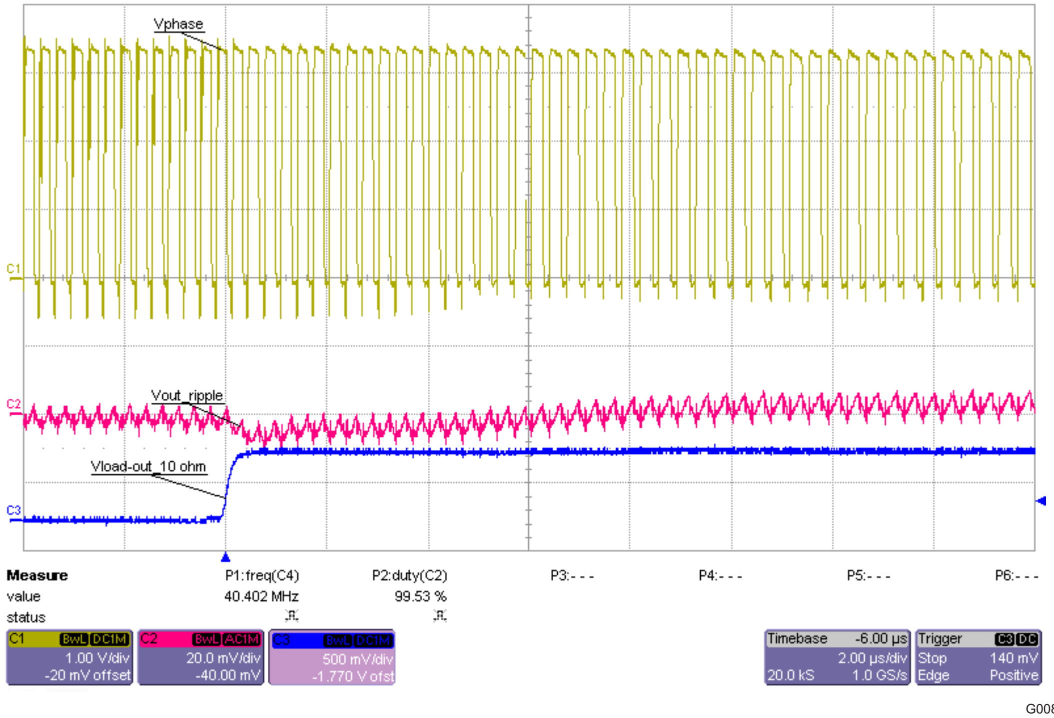

Figure 13. Transient Output Load Step From 50 mA to 100 mA

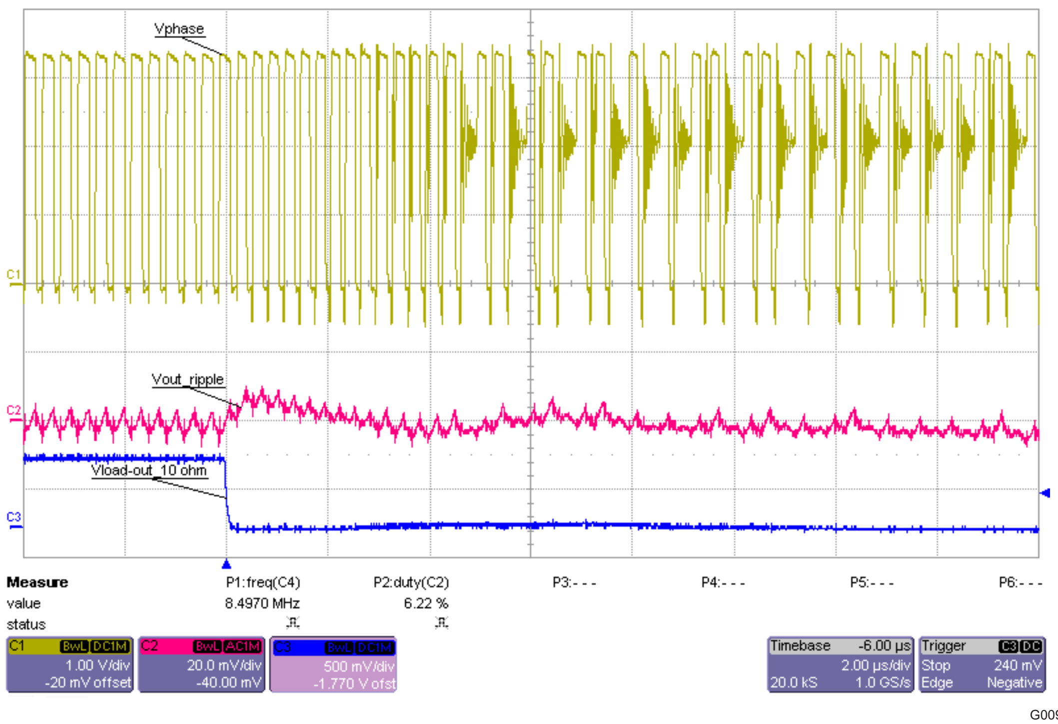

Figure 14. Transient Output Load Step From 100 mA to 50 mA

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 1.9 V to 3.9 V and the output voltage range of 1.9 V to 3.9 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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