Virtex-5 Data Sheet: DC and Switching Characteristics

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Advance Product Specification

Virtex-5 Electrical Characteristics

Virtex™-5 FPGAs are available in -3, -2, -1 speed grades, with -3 having the highest performance.

Virtex-5 DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-5 data sheet, part of an overall set of documentation on the Virtex-5 family of FPGAs, is available on the Xilinx website:

- Virtex-5 Family Overview
- Virtex-5 User Guide
- Virtex-5 Configuration Guide
- Virtex-5 XtremeDSP™ Design Considerations
- Virtex-5 Packaging and Pinout Specification
- Virtex-5 RocketIO™ GTP Transceiver User Guide
- Virtex-5 Tri-mode Ethernet MAC User Guide
- Virtex-5 Integrated Endpoint Block User Guide for PCI Express® Designs
- Virtex-5 System Monitor User Guide
- Virtex-5 PCB Designer's Guide

All specifications are subject to change without notice.

Virtex-5 DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.05	V
V_{REF}	Input reference voltage	–0.5 to 3.75	V
V_{IN}(3)	3.3V I/O input voltage relative to GND(4) (user and dedicated I/Os)	–0.75 to 4.05	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 3.3V output(4) (user and dedicated I/Os)	–0.75 to 4.05	V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(2)	+220	°C
T_J	Maximum junction temperature(2)	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see **UG195**: *Virtex-5 Packaging and Pinout Specification* on the Xilinx website.
3. 3.3V I/O absolute maximum limit applied to DC and AC signals.
4. For 3.3V I/O operation, refer to **UG190**: *Virtex-5 User Guide, Chapter 6, 3.3V I/O Design Guidelines*.

Table 2: **Recommended Operating Conditions**

Symbol	Description	Temperature Range	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	0.95	1.05	V
	Internal supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	0.95	1.05	V
V_{CCAUX}(1)	Auxiliary supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	2.375	2.625	V
V_{CCO}(2,4,5)	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	1.14	3.45	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.14	3.45	V
V_{IN}	3.3V supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	GND – 0.20	3.45	V
	3.3V supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	GND – 0.20	3.45	V
	2.5V and below supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	GND – 0.20	V_{CCO} + 0.2	V
	2.5V and below supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	Commercial		10	mA
		Industrial		10	mA
V_{BATT}(3)	Battery voltage relative to GND, T_J = 0°C to +85°C	Commercial	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:
1. Recommended maximum voltage drop for V_{CCAUX} is 10 mV/ms.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Data Rate	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)		0.75			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)		2.0			V
I_{REF}	V_{REF} leakage current per pin				10	µA
I_L	Input or output leakage current per pin (sample-tested)				10	µA
C_{IN}	Input capacitance (sample-tested)				8	pF
I_{RPU}(1)	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V		20		150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V		10		90	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V		5		45	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V		3		30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V		2		15	µA
I_{RPD}(1)	Pad pull-down (when selected) @ V_{IN} = 2.5V		5		110	µA
I_{BATT}(2)	Battery supply current				150	nA
n	Temperature diode ideality factor			1.0002		n
r	Series resistance			5.0		Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.

Important Note

Typical values for queiscent supply current are now specified at nominal voltage, 85ºC junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85ºC because the majority of designs operate near the high end of the commercial temperature range. Data sheets for older products (e.g., Virtex-4 devices) still specify typical quiescent supply current at T_j = 25ºC. Queiscent supply current is specified by speed grade for Virtex-5 devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade			Units
			-3 (C)	-2 (C & I)	-1 (C & I)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC5VLX30	480	480	300	mA
		XC5VLX30T	507	507	317	mA
		XC5VLX50	651	651	449	mA
		XC5VLX50T	689	689	475	mA
		XC5VLX85	1072	1072	883	mA
		XC5VLX85T	1115	1115	866	mA
		XC5VLX110	1391	1391	1109	mA
		XC5VLX110T	1448	1448	1154	mA
		XC5VLX220	N/A	2783	2278	mA
		XC5VLX220T	N/A	2844	2328	mA
		XC5VLX330	N/A	4193	3432	mA
		XC5VLX330T	N/A	4267	3492	mA
		XC5VSX35T	720	720	554	mA
		XC5VSX50T	1092	1092	840	mA
		XC5VSX95T	N/A	1924	1475	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC5VLX30	1.5	1.5	1.5	mA
		XC5VLX30T	1.5	1.5	1.5	mA
		XC5VLX50	2	2	2	mA
		XC5VLX50T	2	2	2	mA
		XC5VLX85	3	3	3	mA
		XC5VLX85T	3	3	3	mA
		XC5VLX110	4	4	4	mA
		XC5VLX110T	4	4	4	mA
		XC5VLX220	N/A	8	8	mA
		XC5VLX220T	N/A	8	8	mA
		XC5VLX330	N/A	12	12	mA
		XC5VLX330T	N/A	12	12	mA
		XC5VSX35T	1.5	1.5	1.5	mA
		XC5VSX50T	2	2	2	mA
		XC5VSX95T	N/A	4	4	mA

Table 4: **Typical Quiescent Supply Current *(Continued)***

Symbol	Description	Device	Speed and Temperature Grade			Units
			-3 (C)	-2 (C & I)	-1 (C & I)	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC5VLX30	38	38	38	mA
		XC5VLX30T	43	43	43	mA
		XC5VLX50	57	57	57	mA
		XC5VLX50T	62	62	62	mA
		XC5VLX85	93	93	93	mA
		XC5VLX85T	98	98	98	mA
		XC5VLX110	125	125	125	mA
		XC5VLX110T	130	130	130	mA
		XC5VLX220	N/A	229	229	mA
		XC5VLX220T	N/A	236	236	mA
		XC5VLX330	N/A	345	345	mA
		XC5VLX330T	N/A	353	353	mA
		XC5VSX35T	49	49	49	mA
		XC5VSX50T	74	74	74	mA
		XC5VSX95T	N/A	131	131	mA

Notes:
1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). Industrial(I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The power supplies can be can be turned on in any sequence, though the specifications shown in Table 5 are for the recommended power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. Xilinx does not specify the current for other power-on sequences.

Table 5 shows the minimum current required by Virtex-5 devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-5 Devices**

Device	$I_{CCINTMIN}$		$I_{CCAUXMIN}$		I_{CCOMIN}		Units
	Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
XC5VLX30	235		76		50		mA
XC5VLX30T	246		86		50		mA
XC5VLX50	320		114		50		mA
XC5VLX50T	336		124		50		mA
XC5VLX85	492		186		100		mA
XC5VLX85T	515		196		100		mA

Table 5: **Power-On Current for Virtex-5 Devices *(Continued)***

Device	$I_{CCINTMIN}$		$I_{CCAUXMIN}$		I_{CCOMIN}		Units
	Typ(1)	Max	Typ(1)	Max	Typ(1)	Max	
XC5VLX110	623		250		100		mA
XC5VLX110T	651		260		100		mA
XC5VLX220	1023		458		150		mA
XC5VLX220T	1056		472		150		mA
XC5VLX330	1470		690		150		mA
XC5VLX330T	1509		706		150		mA
XC5VSX35T	307		98		50		mA
XC5VSX50T	472		148		50		mA
XC5VSX95T	804		262		100		mA

Notes:
1. Typical values are specified at nominal voltage, 25°C.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.3	0.8	2.0	3.45	0.4	2.4	Note(3)	Note(3)
LVCMOS33, LVDCI33	–0.3	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(4)	Note(4)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note(6)	Note(6)
PCI33_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note(5)	Note(5)
PCI66_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note(5)	Note(5)
PCI-X(5)	–0.2	35% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note(5)	Note(5)

Table 7: **SelectIO DC Input and Output Levels *(Continued)***

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
GTLP	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	–	0.6	N/A	36	N/A
GTL	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	–	0.4	N/A	32	N/A
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
HSTL IV(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	48	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–

Notes:
1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33_3, PCI66_3, and PCI-X, refer to refer to **UG190**: *Virtex-5 User Guide, Chapter 6, 3.3V I/O Design Guidelines.*
6. Supported drive strengths of 2, 4, 6, or 8 mA.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15		15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15		15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15		15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15		15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825			V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals		–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	820	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see **UG190**: *Virtex-5 User Guide, Chapter 6, SelectIO Resources*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6		2.2	V
V_{IDIFF}	Differential Input Voltage(1,2)	0.100		1.5	V

Notes:
1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

RocketIO GTP Transceiver Specifications

RocketIO GTP Transceiver DC Characteristics

Table 12: **Absolute Maximum Ratings**

Symbol	Description		Units
MGTAVCCPLL	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	–0.5 to 1.32	V
MGTAVTTTX	Analog supply voltage for the GTP_DUAL transmitters relative to GND	–0.5 to 1.32	V
MGTAVTTRX	Analog supply voltage for the GTP_DUAL receivers relative to GND	–0.5 to 1.32	V
MGTAVCC	Analog supply voltage for the GTP_DUAL common circuits relative to GND	–0.5 to 1.32	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	–0.5 to 1.32	V

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Max	Units
MGTAVCCPLL(1)	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	1.14	1.26	V
MGTAVTTTX(1)	Analog supply voltage for the GTP_DUAL transmitters relative to GND	1.14	1.26	V
MGTAVTTRX(1)	Analog supply voltage for the GTP_DUAL receivers relative to GND	1.14	1.26	V
MGTAVCC(1)	Analog supply voltage for the GTP_DUAL common circuits relative to GND	0.95	1.05	V
MGTAVTTRXC(1)	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	1.14	1.26	V

Notes:
1. Each voltage listed requires the filter circuit described in **UG196**: *Virtex-5 RocketIO GTP Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_J = –40°C to +100°C.

Table 14: **DC Characteristics Over Recommended Operating Conditions(2)**

Symbol	Description	Min	Typ	Max	Units
$I_{MGTAVTTTX}$	GTP_DUAL tile transmitter termination supply current(3)		71	90	mA
$I_{MGTAVCCPLL}$	GTP_DUAL tile shared PLL supply current		36	60	mA
$I_{MGTAVTTRXC}$	GTP_DUAL tile resistor termination calibration supply current		0.1	0.5	mA
$I_{MGTAVTTRX}$	GTP_DUAL tile receiver termination supply current(3)		0.1	0.5	mA
$I_{MGTAVCC}$	GTP_DUAL tile internal analog supply current		56	110	mA
R_{REF}	Precision reference resistor for internal calibration termination	49.5	50	50.5	Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C, with a 3.2 Gb/s line rate.
2. I_{CC} numbers are given per GTP_DUAL tile with both GTP devices operating with default settings.
3. AC coupled TX/RX link.

Table 15: **Quiescent Supply Current**

Symbol	Description	Device	Typ(1)	Max	Units
I_{CCINTQ}	Quiescent internal supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
I_{VTTTXQ}	Quiescent transmitter supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
$I_{AVCCPLLQ}$	Quiescent GTP_DUAL PLL supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
$I_{VTTRXCQ}$	Quiescent receiver termination switching supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA

Table 15: **Quiescent Supply Current *(Continued)***

Symbol	Description	Device	Typ(1)	Max	Units
I_{TTRXQ}	Quiescent receiver termination supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
I_{VCCQ}	Quiescent internal analog supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. Given for entire die. Powered and unconfigured.
3. Unconnected (if channel is driven to voltage).
4. More accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

RocketIO GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the Virtex-5 RocketIO GTP Transceivers. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage. Consult **UG196**: *Virtex-5 RocketIO GTP Transceiver User Guide* for further details.

Table 16: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 3.2 Gb/s	150		2000	mV
		External AC coupled > 3.2 Gb/s	180		2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400		1200	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V		800		mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			1400	mV
V_{SEOUT}	Single-ended output voltage swing(1)	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			700	mV
V_{CMOUT}	Common mode output voltage	Equation based MGTAVTTTX = 1.2V	1200 – Amplitude/2			mV
R_{IN}	Differential input resistance		90	100	120	Ω
R_{OUT}	Differential output resistance		90	100	120	Ω
T_{OSKEW}	Transmitter output skew				15	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:
1. The output swing and preemphasis levels are programmable using the attributes discussed in **UG196**: *Virtex-5 RocketIO GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

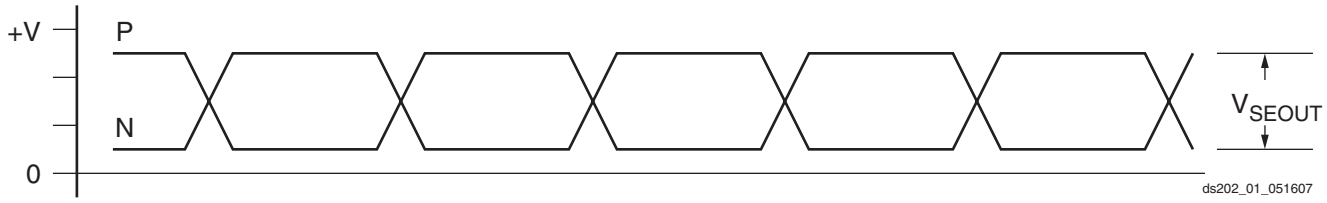

Figure 1: **Single-Ended Output Voltage Swing**

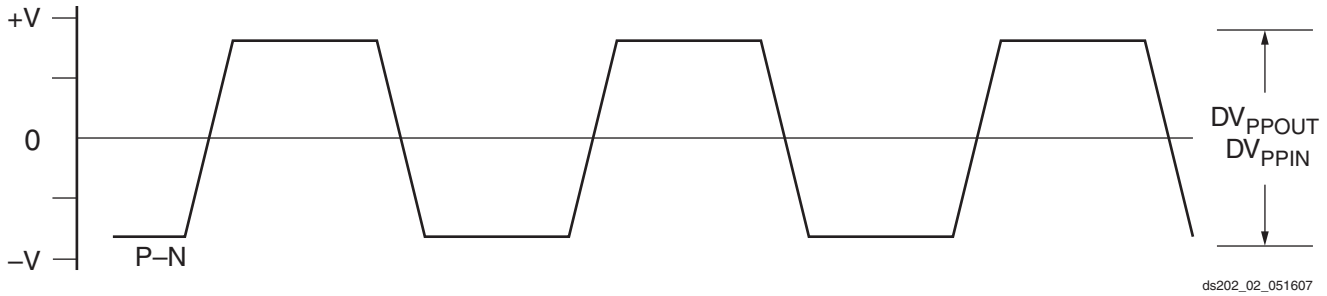

Figure 2: **Peak-to-Peak Differential Output Voltage**

Table 17 summarizes the DC input specifications of the Virtex-5 RocketIO GTP Transceivers. Figure 3 shows the single-ended input voltage swing. Figure 4 shows the peak-to-peak differential clock input voltage swing. Consult **UG196**: *Virtex-5 RocketIO GTP Transceiver User Guide* for further details.

Table 17: **RocketIO GTP Clock DC Input Level Specification(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage		200	800	2000	mV
V_{SEIN}	Single-ended input voltage		100	400	1000	mV
R_{IN}	Differential input resistance		80	105	130	Ω
C_{EXT}	Required external AC coupling capacitor		75	100	200	nF

Notes:
1. V_{MIN} = 0V and V_{MAX} = 1200mV

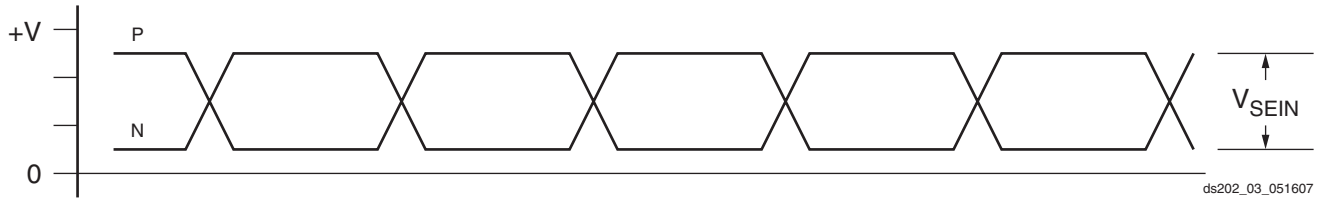

Figure 3: **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

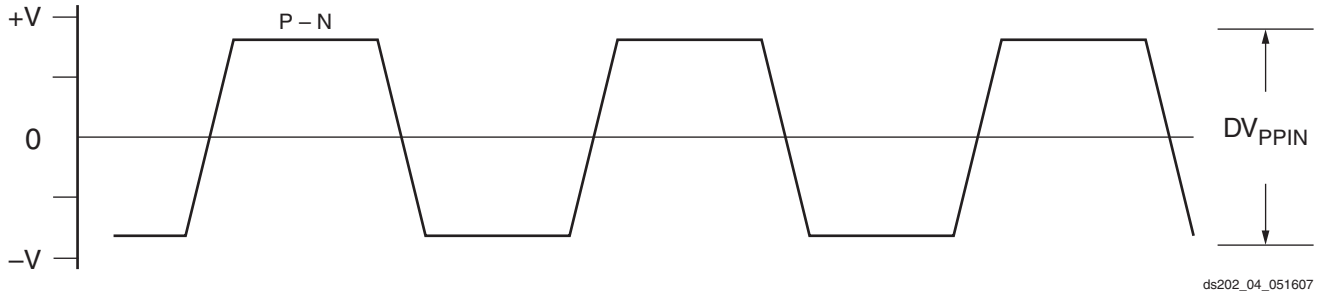

Figure 4: **Differential Clock Input Voltage Swing Peak-to-Peak**

RocketIO GTP Switching Characteristics

Consult **UG196**: *Virtex-5 RocketIO GTP Transceiver User Guide* for further information.

Table 18: **GTP Transceiver Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.75	3.75	3.2	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.0	2.0	2.0	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.0	1.0	1.0	GHz

Table 19: **CRC Block Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{CRC}	CRCCLK maximum frequency	320	320	250	MHz

Table 20: **GTP Transceiver Reference Clock Switching Characteristics**

			All Speed Grades			
Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GCLK}	Reference clock frequency range(1)	CLK	60		350	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200	400	ps
T_{FCLK}	Reference clock fall time	80% – 20%		200	400	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{GJTT}	Reference clock total jitter, peak-peak(2)	CLK			40	ps
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock			1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has relocked to the reference clock. Includes lock to reference time.			200	µs

Notes:
1. The clock from the GTP_DUAL differential clock pin pair can be used for all serial bit rates. GREFCLK can be used for serial bit rates up to 1 Gb/s.
2. Measured at the package pin.

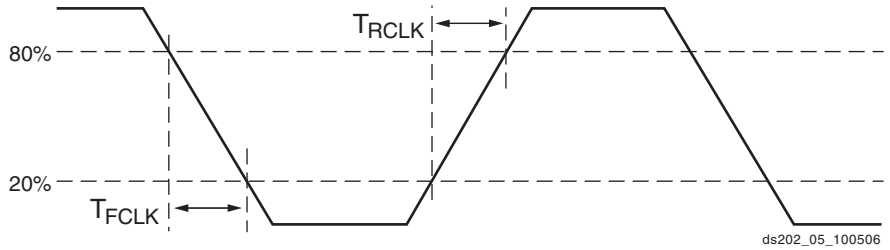

Figure 5: **Reference Clock Timing Parameters**

Table 21: **GTP User Clock Switching Characteristics(1)**

			Speed Grade			
Symbol	**Description**	**Conditions**	**-3**	**-2**	**-1**	**Units**
F_{TXOUT}	TXOUTCLK maximum frequency		375	375	320	MHz
F_{RXREC}	RXRECCLK maximum frequency		375	375	320	MHz
T_{RX}	RXUSRCLK maximum frequency		375	375	320	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	RXDATAWIDTH = 0	350	350	320	MHz
		RXDATAWIDTH = 1	187.5	187.5	160	MHz
T_{TX}	TXUSRCLK maximum frequency		375	375	320	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	TXDATAWIDTH = 0	350	350	320	MHz
		TXDATAWIDTH = 1	187.5	187.5	160	MHz

Notes:
1. Clocking must be implemented as described in **UG196**: *Virtex-5 RocketIO GTP Transceiver User Guide*

Table 22: **GTP Transmitter Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTX}	Serial data rate range		0.1		F_{GTPMAX}	Gb/s
T_{RTX}	TX Rise time			140		ps
T_{FTX}	TX Fall time			120		ps
T_{LLSKEW}	TX lane-to-lane skew(1)				2 + 500 ps	UI
$V_{TXOOBVDPP}$	Electrical idle amplitude				20	mV
$T_{TXOOBTRANS}$	Electrical idle transition time				40	ns
$T_{J3.75}$	Total Jitter(2)	3.75 Gb/s			0.35	UI
$D_{J3.75}$	Deterministic Jitter(2)				0.19	UI
$T_{J3.2}$	Total Jitter(2)	3.20 Gb/s			0.35	UI
$D_{J3.2}$	Deterministic Jitter(2)				0.19	UI
$T_{J2.5}$	Total Jitter(2)	2.50 Gb/s			0.30	UI
$D_{J2.5}$	Deterministic Jitter(2)				0.14	UI
$T_{J2.0}$	Total Jitter(2)	2.00 Gb/s			0.30	UI
$D_{J2.0}$	Deterministic Jitter(2)				0.14	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s			0.20	UI
$D_{J1.25}$	Deterministic Jitter(2)				0.10	UI
$T_{J1.00}$	Total Jitter(2)	1.00 Gb/s			0.20	UI
$D_{J1.00}$	Deterministic Jitter(2)				0.10	UI
T_{J500}	Total Jitter(2)	500 Mb/s			0.10	UI
D_{J500}	Deterministic Jitter(2)				0.04	UI
T_{J100}	Total Jitter(2)	100 Mb/s			0.02	UI
D_{J100}	Deterministic Jitter(2)				0.01	UI

Notes:
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP_DUAL sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1.
3. All jitter values are based on a Bit-Error Ratio of $1e^{-12}$.

Table 23: **GTP Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GRX}	Serial data rate	RX oversampler not enabled	0.5		F_{GTPMAX}	Gb/s
		RX oversampler enabled	0.1		0.5	Gb/s
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak	OOBDETECT_THRESHOLD = 100	60	105	165	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000		0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed			150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	ACDR 2nd-order loop enabled	–1000		1000	ppm
SJ Jitter Tolerance						
$JT\_SJ_{3.75}$	Sinusoidal Jitter(2)	3.75 Gb/s	0.30			UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(2)	3.20 Gb/s	0.40			UI
$JT\_SJ_{2.50}$	Sinusoidal Jitter(2)	2.50 Gb/s	0.40			UI
$JT\_SJ_{2.00}$	Sinusoidal Jitter(2)	2.00 Gb/s	0.40			UI
$JT\_SJ_{1.00}$	Sinusoidal Jitter(2)	1.00 Gb/s	0.30			UI
JT_SJ_{500}	Sinusoidal Jitter(2)	500 Mb/s	0.30			UI
JT_SJ_{500}	Sinusoidal Jitter(2)	500 Mb/s OS	0.30			UI
JT_SJ_{100}	Sinusoidal Jitter(2)	100 Mb/s OS	0.30			UI
SJ Jitter Tolerance with Stressed Eye						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(3)	3.20 Gb/s	0.87			UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(3)	3.20 Gb/s	0.30			UI

Notes:
1. Using PLL_RX_DIVSEL_OUT = 1.
2. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
3. Stimulus signal includes 0.4UI of DJ and 0.17UI of RJ. RX equalizer is enabled.
4. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.

Ethernet MAC Switching Characteristics

Consult **UG194**: *Virtex-5 Tri-mode Ethernet Media Access Controller User Guide* for further information.

Table 24: **Maximum Ethernet MAC Performance**

Description	Speed Grade			Units
	-3	-2	-1	
Ethernet MAC Maximum Performance	10/100/1000			Mb/s

System Monitor Analog-to-Digital Converter Specification

Table 25: **Analog-to-Digital Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV_{DD} = 2.5V ± 2%, V_{REFP} = 2.5V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_A = T_{MIN} to T_{MAX}, Typical values at T_A=+25°C						
DC Accuracy: All external input channels such as V_P/V_N and $V_{AUXP}[15:0]/V_{AUXN}[15:0]$, Unipolar Mode, and Common Mode = 0V						
Resolution			10			Bits
Integral Nonlinearity	INL				±2	LSBs
Differential Nonlinearity	DNL	No missing codes (T_{MIN} to T_{MAX}) Guaranteed Monotonic			±0.9	LSBs
Unipolar Offset Error(1)		Uncalibrated		±2	±30	LSBs
Bipolar Offset Error(1)		Uncalibrated measured in bipolar mode		±2	±30	LSBs
Gain Error(1)		Uncalibrated		±0.2	±2	%
Bipolar Gain Error(1)		Uncalibrated measured in bipolar mode		±0.2	±2	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. $V_{REFP} - V_{REFN}$ = 2.5V		±10		LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. $V_{REFP} - V_{REFN}$ = 2.5V		±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature		±0.01		LSB/°C
DC Common-Mode Reject	$CMRR_{DC}$	$V_N = V_{CM}$ = 0.5V ± 0.5V, $V_P - V_N$ = 100mV		70		dB
Conversion Rate(2)						
Conversion Time - Continuous	t_{CONV}	Number of CLK cycles	26		32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles			21	
T/H Acquisition Time	t_{ACQ}	Number of CLK cycles	4			
DRP Clock Frequency	DCLK	DRP clock frequency	8		250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1		5.2	MHz
CLK Duty cycle			40		60	%
Analog Inputs(3)						
Dedicated Analog Inputs Input Voltage Range V_P - V_N		Unipolar Operation	0		1	Volts
		Differential Inputs	–0.25		+0.25	
		Unipolar Common Mode Range (FS input)	0		+0.5	
		Differential Common Mode Range (FS input)	+0.3		+0.7	
		Bandwidth		20		MHz
Auxiliary Analog Inputs Input Voltage Range $V_{AUXP[0]}/V_{AUXN[0]}$ to $V_{AUXP[15]}/V_{AUXN[15]}$		Unipolar Operation	0		1	Volts
		Differential Operation	–0.25		+0.25	
		Unipolar Common Mode Range (FS input)	0		+0.5	
		Differential Common Mode Range (FS input)	+0.3		+0.7	
		Bandwidth		10		kHz
Input Leakage Current		A/D not converting, ADCCLK stopped		±1.0		µA

Table 25: **Analog-to-Digital Specifications *(Continued)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Input Capacitance				10		pF
On-chip Supply Monitor Error		V_{CCINT} and V_{CCAUX} with calibration enabled			±1.0	% Reading
On-chip Temperature Monitor Error		–40°C to +125°C with calibration enabled			±4	°C
External Reference Inputs(4)						
Positive Reference Input Voltage Range	V_{REFP}	Measured Relative to V_{REFN}	2.45	2.5	2.55	Volts
Negative Reference Input Voltage Range	V_{REFN}	Measured Relative to AGND	–50	0	100	mV
Input current	I_{REF}	ADCCLK = 5.2 MHz			100	µA
Power Requirements						
Analog Power Supply	AV_{DD}	Measured Relative to AV_{SS}	2.45	2.5	2.55	Volts
Analog Supply Current	AI_{DD}	ADCCLK = 5.2 MHz	5		8	mA

Notes:
1. Offset and gain errors are removed by enabling the System Monitor automatic gain calibration feature. See **UG192**: *Virtex-5 System Monitor User Guide*.
2. See "System Monitor Timing" in **UG192**: *Virtex-5 System Monitor User Guide*.
3. See "Analog Inputs" in **UG192**: *Virtex-5 System Monitor User Guide* for a detailed description.
4. Any variation in the reference voltage from the nominal V_{REFP} = 2.5V and V_{REFN} = 0V will result is a deviation from the ideal transfer function.This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing the supply voltage and reference to vary by ±2% is permitted.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-5 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the **Switching Characteristics**, page 21. Table 26 shows internal (register-to-register) performance.

Table 26: **Register-to-Register Performance**

Description	Register-to-Register (with I/O Delays)			Units
	Speed Grade			
	-3	-2	-1	
Basic Functions				
16:1 Multiplexer	550	500	450	MHz
32:1 Multiplexer	550	500	450	MHz
64:1 Multiplexer	511	467	407	MHz
9 x 9 Logic Multiplier with 4 pipe stages	468	438	428	MHz
9 x 9 Logic Multiplier with 5 pipe stages	550	500	428	MHz
16-bit Adder	550	500	450	MHz
32-bit Adder	550	500	447	MHz
64-bit Adder	423	377	323	MHz
Register to LUT to Register	550	500	450	MHz
16-bit Counter	550	500	450	MHz
32-bit Counter	550	500	450	MHz
64-bit Counter	428	381	333	MHz
Memory				
Cascaded block RAM (64K)	500	450	400	MHz
Block RAM Pipelined				
Single-Port 512 x 36 bits	550	500	450	MHz
Single-Port 4096 x 4 bits	550	500	450	MHz
Dual-Port A: 4096 x 4 bits and B: 1024 x 18 bits	550	500	450	MHz
Distributed RAM				
Single-Port 16 x 8	550	500	450	MHz
Single-Port 32 x 8	550	500	450	MHz
Single-Port 64 x 8	550	500	450	MHz
Dual-Port 16 x 8				MHz
Shift Register Chain				
16-bit	550	500	450	MHz
32-bit	550	500	450	MHz
64-bit	550	500	438	MHz

Table 26: **Register-to-Register Performance *(Continued)***

Description	Register-to-Register (with I/O Delays)			Units
	Speed Grade			
	-3	-2	-1	
Dedicated Arithmetic Logic				
DSP48E Quad 12-bit Adder/Subtracter	550	500	450	MHz
DSP48E Dual 24-bit Adder/Subtracter	550	500	450	MHz
DSP48E 48-bit Adder/Subtracter	550	500	450	MHz
DSP48E 48-bit Counter	550	500	450	MHz
DSP48E 48-bit Comparator	550	500	450	MHz
DSP48E 25 x 18 bit Pipelined Multiplier	550	500	450	MHz
DSP48E Direct 4-tap FIR Filter Pipelined	510	458	397	MHz
DSP48E Systolic n-tap FIR Filter Pipelined	550	500	450	MHz

Notes:
1. Deviced used is the XC5VLX50T- FF1136

Table 27: **Interface Performances**

Description	Speed Grade		
	-3	-2	-1
Networking Applications			
SFI-4.1 (SDR LVDS Interface)	710 MHz	710 MHz	645 MHz
SPI-4.2 (DDR LVDS Interface)	1.25 Gb/s	1.0 Gb/s	1.0 Gb/s
Memory Interfaces			
DDR	200 MHz	200 MHz	200 MHz
DDR2	333 MHz	300 MHz	267 MHz
QDR II SRAM	300 MHz	300 MHz	250 MHz
RLDRAM II	333 MHz	300 MHz	250 MHz

Switching Characteristics

All values represented in this data sheet are based on speed specification version 1.57. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 28 correlates the current status of each Virtex-5 device on a per speed grade basis.

Table 28: **Virtex-5 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC5VLX30			-3, -2, -1
XC5VLX30T			-3, -2, -1
XC5VLX50			-3, -2, -1
XC5VLX50T			-3, -2, -1
XC5VLX85			-3, -2, -1
XC5VLX85T			-3, -2, -1
XC5VLX110			-3, -2, -1
XC5VLX110T			-3, -2, -1
XC5VLX220			-2, -1
XC5VLX220T			-2, -1
XC5VLX330			-2, -1
XC5VLX330T			-2, -1
XC5VSX35T			-3, -2, -1
XC5VSX50T			-3, -2, -1
XC5VSX95T			-2, -1

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-5 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 29 lists the production released Virtex-5 family member, speed grade, and the corresponding supported speed specification version and ISE software revisions.

Table 29: **Virtex-5 Production Software and Speed Specification Release**

Device	Speed Grade Designations		
	-3	-2	-1
XC5VLX30	ISE 9.2i SP2 v1.56		
XC5VLX30T	ISE 9.2i SP2 v1.56		
XC5VLX50	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX50T	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX85	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX85T	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX110	ISE 9.2i SP2 v1.56		
XC5VLX110T	ISE 9.2i SP2 v1.56		
XC5VLX220	N/A	ISE 9.2i SP3 v1.57	
XC5VLX220T	N/A	ISE 9.2i SP3 v1.57	
XC5VLX330	N/A	ISE 9.2i SP3 v1.57	
XC5VLX330T	N/A	ISE 9.2i SP3 v1.57	
XC5VSX35T	ISE 9.2i SP3 v1.57		
XC5VSX50T	ISE 9.2i SP3 v1.57	ISE 9.2i SP2 v1.56	
XC5VSX95T	N/A	ISE 9.2i SP3 v1.57	

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 30 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 31 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 30: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVDS_25	0.80	0.90	1.06	1.13	1.29	1.44	1.13	1.29	1.44	ns
LVDSEXT_25	1.01	1.16	1.30	1.17	1.34	1.49	1.17	1.34	1.49	ns
HT_25	0.80	0.90	1.06	1.10	1.26	1.40	1.10	1.26	1.40	ns
BLVDS_25	0.80	0.90	1.06	1.24	1.38	1.58	1.24	1.38	1.58	ns
RSDS_25 (point to point)	0.80	0.90	1.06	1.13	1.29	1.44	1.13	1.29	1.44	ns
ULVDS_25	0.80	0.90	1.06	1.10	1.27	1.41	1.10	1.27	1.41	ns
PCI33_3	0.62	0.70	0.82	1.85	2.06	2.38	1.85	2.06	2.38	ns
PCI66_3	0.62	0.70	0.82	1.85	2.06	2.38	1.85	2.06	2.38	ns
PCI-X	0.62	0.70	0.82	1.40	1.56	1.80	1.40	1.56	1.80	ns
GTL	0.76	0.85	1.00	1.47	1.63	1.86	1.47	1.63	1.86	ns
GTLP	0.76	0.85	1.00	1.51	1.68	1.93	1.51	1.68	1.93	ns
HSTL_I	0.76	0.85	1.00	1.42	1.57	1.79	1.42	1.57	1.79	ns
HSTL_II	0.76	0.85	1.00	1.39	1.53	1.74	1.39	1.53	1.74	ns
HSTL_III	0.76	0.85	1.00	1.44	1.60	1.85	1.44	1.60	1.85	ns
HSTL_IV	0.76	0.85	1.00	1.44	1.60	1.83	1.44	1.60	1.83	ns
HSTL_I _18	0.76	0.85	1.00	1.40	1.55	1.77	1.40	1.55	1.77	ns
HSTL_II _18	0.76	0.85	1.00	1.36	1.51	1.72	1.36	1.51	1.72	ns
HSTL_III _18	0.76	0.85	1.00	1.45	1.61	1.85	1.45	1.61	1.85	ns
HSTL_IV_18	0.76	0.85	1.00	1.41	1.57	1.81	1.41	1.57	1.81	ns
SSTL2_I	0.76	0.85	1.00	1.48	1.64	1.87	1.48	1.64	1.87	ns
SSTL2_II	0.76	0.85	1.00	1.40	1.55	1.76	1.40	1.55	1.76	ns
LVTTL, Slow, 2 mA	0.62	0.70	0.82	4.10	4.47	5.01	4.10	4.47	5.01	ns
LVTTL, Slow, 4 mA	0.62	0.70	0.82	2.87	3.09	3.41	2.87	3.09	3.41	ns
LVTTL, Slow, 6 mA	0.62	0.70	0.82	2.66	2.91	3.29	2.66	2.91	3.29	ns
LVTTL, Slow, 8 mA	0.62	0.70	0.82	2.09	2.30	2.61	2.09	2.30	2.61	ns
LVTTL, Slow, 12 mA	0.62	0.70	0.82	1.94	2.15	2.46	1.94	2.15	2.46	ns
LVTTL, Slow, 16 mA	0.62	0.70	0.82	1.84	2.04	2.34	1.84	2.04	2.34	ns

Table 30: **IOB Switching Characteristics *(Continued)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVTTL, Slow, 24 mA	0.62	0.70	0.82	1.87	2.07	2.38	1.87	2.07	2.38	ns
LVTTL, Fast, 2 mA	0.62	0.70	0.82	3.32	3.61	4.05	3.32	3.61	4.05	ns
LVTTL, Fast, 4 mA	0.62	0.70	0.82	2.32	2.55	2.90	2.32	2.55	2.90	ns
LVTTL, Fast, 6 mA	0.62	0.70	0.82	2.10	2.31	2.63	2.10	2.31	2.63	ns
LVTTL, Fast, 8 mA	0.62	0.70	0.82	1.65	1.82	2.09	1.65	1.82	2.09	ns
LVTTL, Fast, 12 mA	0.62	0.70	0.82	1.47	1.63	1.89	1.47	1.63	1.89	ns
LVTTL, Fast, 16 mA	0.62	0.70	0.82	1.41	1.57	1.81	1.41	1.57	1.81	ns
LVTTL, Fast, 24 mA	0.62	0.70	0.82	1.36	1.52	1.74	1.36	1.52	1.74	ns
LVCMOS33, Slow, 2 mA	0.62	0.70	0.82	3.63	3.96	4.44	3.63	3.96	4.44	ns
LVCMOS33, Slow, 4 mA	0.62	0.70	0.82	2.82	3.09	3.49	2.82	3.09	3.49	ns
LVCMOS33, Slow, 6 mA	0.62	0.70	0.82	2.61	2.86	3.24	2.61	2.86	3.24	ns
LVCMOS33, Slow, 8 mA	0.62	0.70	0.82	2.06	2.26	2.57	2.06	2.26	2.57	ns
LVCMOS33, Slow, 12 mA	0.62	0.70	0.82	1.95	2.14	2.42	1.95	2.14	2.42	ns
LVCMOS33, Slow, 16 mA	0.62	0.70	0.82	1.86	2.04	2.31	1.86	2.04	2.31	ns
LVCMOS33, Slow, 24 mA	0.62	0.70	0.82	1.87	2.07	2.35	1.87	2.07	2.35	ns
LVCMOS33, Fast, 2 mA	0.62	0.70	0.82	2.94	3.20	3.59	2.94	3.20	3.59	ns
LVCMOS33, Fast, 4 mA	0.62	0.70	0.82	2.27	2.50	2.84	2.27	2.50	2.84	ns
LVCMOS33, Fast, 6 mA	0.62	0.70	0.82	2.06	2.27	2.59	2.06	2.27	2.59	ns
LVCMOS33, Fast, 8 mA	0.62	0.70	0.82	1.61	1.79	2.05	1.61	1.79	2.05	ns
LVCMOS33, Fast, 12 mA	0.62	0.70	0.82	1.45	1.61	1.86	1.45	1.61	1.86	ns
LVCMOS33, Fast, 16 mA	0.62	0.70	0.82	1.40	1.56	1.80	1.40	1.56	1.80	ns
LVCMOS33, Fast, 24 mA	0.62	0.70	0.82	1.35	1.51	1.74	1.35	1.51	1.74	ns
LVCMOS25, Slow, 2 mA	0.61	0.70	0.82	3.67	3.97	4.42	3.67	3.97	4.42	ns
LVCMOS25, Slow, 4 mA	0.61	0.70	0.82	2.37	2.60	2.94	2.37	2.60	2.94	ns
LVCMOS25, Slow, 6 mA	0.61	0.70	0.82	2.19	2.41	2.74	2.19	2.41	2.74	ns
LVCMOS25, Slow, 8 mA	0.61	0.70	0.82	2.05	2.26	2.56	2.05	2.26	2.56	ns
LVCMOS25, Slow, 12 mA	0.61	0.70	0.82	2.10	2.31	2.63	2.10	2.31	2.63	ns
LVCMOS25, Slow, 16 mA	0.61	0.70	0.82	1.84	2.02	2.30	1.84	2.02	2.30	ns
LVCMOS25, Slow, 24 mA	0.61	0.70	0.82	1.83	2.04	2.34	1.83	2.04	2.34	ns
LVCMOS25, Fast, 2 mA	0.61	0.70	0.82	3.14	3.41	3.82	3.14	3.41	3.82	ns
LVCMOS25, Fast, 4 mA	0.61	0.70	0.82	1.89	2.08	2.37	1.89	2.08	2.37	ns
LVCMOS25, Fast, 6 mA	0.61	0.70	0.82	1.74	1.92	2.20	1.74	1.92	2.20	ns
LVCMOS25, Fast, 8 mA	0.61	0.70	0.82	1.66	1.83	2.09	1.66	1.83	2.09	ns
LVCMOS25, Fast, 12 mA	0.61	0.70	0.82	1.52	1.69	1.94	1.52	1.69	1.94	ns
LVCMOS25, Fast, 16 mA	0.61	0.70	0.82	1.43	1.60	1.85	1.43	1.60	1.85	ns
LVCMOS25, Fast, 24 mA	0.61	0.70	0.82	1.40	1.54	1.76	1.40	1.54	1.76	ns

Table 30: **IOB Switching Characteristics *(Continued)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVCMOS18, Slow, 2 mA	0.67	0.76	0.89	4.20	4.56	5.09	4.20	4.56	5.09	ns
LVCMOS18, Slow, 4 mA	0.67	0.76	0.89	3.03	3.32	3.75	3.03	3.32	3.75	ns
LVCMOS18, Slow, 6 mA	0.67	0.76	0.89	2.37	2.61	2.97	2.37	2.61	2.97	ns
LVCMOS18, Slow, 8 mA	0.67	0.76	0.89	2.15	2.37	2.69	2.15	2.37	2.69	ns
LVCMOS18, Slow, 12 mA	0.67	0.76	0.89	1.95	2.16	2.47	1.95	2.16	2.47	ns
LVCMOS18, Slow, 16 mA	0.67	0.76	0.89	1.93	2.14	2.45	1.93	2.14	2.45	ns
LVCMOS18, Fast, 2 mA	0.67	0.76	0.89	3.41	3.71	4.16	3.41	3.71	4.16	ns
LVCMOS18, Fast, 4 mA	0.67	0.76	0.89	2.36	2.61	2.98	2.36	2.61	2.98	ns
LVCMOS18, Fast, 6 mA	0.67	0.76	0.89	1.87	2.06	2.35	1.87	2.06	2.35	ns
LVCMOS18, Fast, 8 mA	0.67	0.76	0.89	1.69	1.87	2.13	1.69	1.87	2.13	ns
LVCMOS18, Fast, 12 mA	0.67	0.76	0.89	1.51	1.68	1.93	1.51	1.68	1.93	ns
LVCMOS18, Fast, 16 mA	0.67	0.76	0.89	1.44	1.61	1.86	1.44	1.61	1.86	ns
LVCMOS15, Slow, 2 mA	0.73	0.83	0.98	3.50	3.84	4.34	3.50	3.84	4.34	ns
LVCMOS15, Slow, 4 mA	0.73	0.83	0.98	2.17	2.40	2.74	2.17	2.40	2.74	ns
LVCMOS15, Slow, 6 mA	0.73	0.83	0.98	1.99	2.20	2.52	1.99	2.20	2.52	ns
LVCMOS15, Slow, 8 mA	0.73	0.83	0.98	1.91	2.12	2.43	1.91	2.12	2.43	ns
LVCMOS15, Slow, 12 mA	0.73	0.83	0.98	1.74	1.95	2.25	1.74	1.95	2.25	ns
LVCMOS15, Slow, 16 mA	0.73	0.83	0.98	1.71	1.91	2.20	1.71	1.91	2.20	ns
LVCMOS15, Fast, 2 mA	0.73	0.83	0.98	2.80	3.07	3.48	2.80	3.07	3.48	ns
LVCMOS15, Fast, 4 mA	0.73	0.83	0.98	1.76	1.95	2.23	1.76	1.95	2.23	ns
LVCMOS15, Fast, 6 mA	0.73	0.83	0.98	1.62	1.80	2.06	1.62	1.80	2.06	ns
LVCMOS15, Fast, 8 mA	0.73	0.83	0.98	1.57	1.74	2.00	1.57	1.74	2.00	ns
LVCMOS15, Fast, 12 mA	0.73	0.83	0.98	1.43	1.60	1.86	1.43	1.60	1.86	ns
LVCMOS15, Fast, 16 mA	0.73	0.83	0.98	1.37	1.53	1.77	1.37	1.53	1.77	ns
LVCMOS12, Slow, 2 mA	0.84	0.96	1.14	3.58	3.98	4.58	3.58	3.98	4.58	ns
LVCMOS12, Slow, 4 mA	0.84	0.96	1.14	2.10	2.33	2.66	2.10	2.33	2.66	ns
LVCMOS12, Slow, 6 mA	0.84	0.96	1.14	2.00	2.18	2.45	2.00	2.18	2.45	ns
LVCMOS12, Slow, 8 mA	0.84	0.96	1.14	1.91	2.14	2.48	1.91	2.14	2.48	ns
LVCMOS12, Fast, 2 mA	0.84	0.96	1.14	3.05	3.38	3.87	3.05	3.38	3.87	ns
LVCMOS12, Fast, 4 mA	0.84	0.96	1.14	1.71	1.91	2.20	1.71	1.91	2.20	ns
LVCMOS12, Fast, 6 mA	0.84	0.96	1.14	1.58	1.78	2.08	1.58	1.78	2.08	ns
LVCMOS12, Fast, 8 mA	0.84	0.96	1.14	1.52	1.70	1.97	1.52	1.70	1.97	ns

Table 30: **IOB Switching Characteristics *(Continued)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVDCI_33	0.62	0.70	0.82	1.50	1.66	1.90	1.50	1.66	1.90	ns
LVDCI_25	0.61	0.70	0.82	1.55	1.71	1.93	1.55	1.71	1.93	ns
LVDCI_18	0.67	0.76	0.89	1.65	1.78	1.99	1.65	1.78	1.99	ns
LVDCI_15	0.73	0.83	0.98	1.58	1.75	2.02	1.58	1.75	2.02	ns
LVDCI_DV2_25	0.61	0.70	0.82	1.36	1.51	1.74	1.36	1.51	1.74	ns
LVDCI_DV2_18	0.67	0.76	0.89	1.43	1.60	1.85	1.43	1.60	1.85	ns
LVDCI_DV2_15	0.73	0.83	0.98	1.48	1.65	1.91	1.48	1.65	1.91	ns
GTL_DCI	0.76	0.85	1.00	1.36	1.47	1.65	1.36	1.47	1.65	ns
GTLP_DCI	0.76	0.85	1.00	1.37	1.52	1.76	1.37	1.52	1.76	ns
LVPECL_25	0.80	0.90	1.06	1.28	1.42	1.62	1.28	1.42	1.62	ns
HSTL_I_12	0.76	0.85	1.00	1.45	1.61	1.85	1.45	1.61	1.85	ns
HSTL_I_DCI	0.76	0.85	1.00	1.41	1.56	1.77	1.41	1.56	1.77	ns
HSTL_II_DCI	0.76	0.85	1.00	1.34	1.48	1.69	1.34	1.48	1.69	ns
HSTL_II_T_DCI	0.76	0.85	1.00	1.41	1.56	1.77	1.41	1.56	1.77	ns
HSTL_III_DCI	0.76	0.85	1.00	1.57	1.72	1.95	1.57	1.72	1.95	ns
HSTL_IV_DCI	0.76	0.85	1.00	1.34	1.46	1.64	1.34	1.46	1.64	ns
HSTL_I_DCI_18	0.76	0.85	1.00	1.36	1.50	1.70	1.36	1.50	1.70	ns
HSTL_II_DCI_18	0.76	0.85	1.00	1.30	1.43	1.64	1.30	1.43	1.64	ns
HSTL_II _T_DCI_18	0.76	0.85	1.00	1.36	1.50	1.70	1.36	1.50	1.70	ns
HSTL_III_DCI_18	0.76	0.85	1.00	1.55	1.69	1.91	1.55	1.69	1.91	ns
HSTL_IV_DCI_18	0.76	0.85	1.00	1.31	1.44	1.62	1.31	1.44	1.62	ns
DIFF_HSTL_I_18	0.80	0.90	1.06	1.40	1.55	1.77	1.40	1.55	1.77	ns
DIFF_HSTL_I_DCI_18	0.80	0.90	1.06	1.36	1.50	1.70	1.36	1.50	1.70	ns
DIFF_HSTL_I	0.80	0.90	1.06	1.42	1.57	1.79	1.42	1.57	1.79	ns
DIFF_HSTL_I_DCI	0.80	0.90	1.06	1.41	1.56	1.77	1.41	1.56	1.77	ns
DIFF_HSTL_II_18	0.80	0.90	1.06	1.36	1.51	1.72	1.36	1.51	1.72	ns
DIFF_HSTL_II_DCI_18	0.80	0.90	1.06	1.30	1.43	1.64	1.30	1.43	1.64	ns
DIFF_HSTL_II	0.80	0.90	1.06	1.39	1.53	1.74	1.39	1.53	1.74	ns
DIFF_HSTL_II_DCI	0.80	0.90	1.06	1.34	1.48	1.69	1.34	1.48	1.69	ns

Table 30: **IOB Switching Characteristics *(Continued)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
SSTL2_I_DCI	0.76	0.85	1.00	1.42	1.56	1.78	1.42	1.56	1.78	ns
SSTL2_II_DCI	0.76	0.85	1.00	1.34	1.48	1.70	1.34	1.48	1.70	ns
SSTL2_II_T_DCI	0.76	0.85	1.00	1.42	1.56	1.78	1.42	1.56	1.78	ns
SSTL18_I	0.76	0.85	1.00	1.46	1.61	1.84	1.46	1.61	1.84	ns
SSTL18_II	0.76	0.85	1.00	1.39	1.53	1.75	1.39	1.53	1.75	ns
SSTL18_I_DCI	0.76	0.85	1.00	1.39	1.53	1.74	1.39	1.53	1.74	ns
SSTL18_II_DCI	0.76	0.85	1.00	1.30	1.44	1.64	1.30	1.44	1.64	ns
SSTL18_II_T_DCI	0.76	0.85	1.00	1.39	1.53	1.74	1.39	1.53	1.74	ns
DIFF_SSTL2_I	0.80	0.90	1.06	1.48	1.64	1.87	1.48	1.64	1.87	ns
DIFF_SSTL2_I_DCI	0.80	0.90	1.06	1.42	1.56	1.78	1.42	1.56	1.78	ns
DIFF_SSTL18_I	0.80	0.90	1.06	1.46	1.61	1.84	1.46	1.61	1.84	ns
DIFF_SSTL18_I_DCI	0.80	0.90	1.06	1.39	1.53	1.74	1.39	1.53	1.74	ns
DIFF_SSTL2_II	0.80	0.90	1.06	1.40	1.55	1.76	1.40	1.55	1.76	ns
DIFF_SSTL2_II_DCI	0.80	0.90	1.06	1.34	1.48	1.70	1.34	1.48	1.70	ns
DIFF_SSTL18_II	0.80	0.90	1.06	1.39	1.53	1.75	1.39	1.53	1.75	ns
DIFF_SSTL18_II_DCI	0.80	0.90	1.06	1.30	1.44	1.64	1.30	1.44	1.64	ns

Table 31: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{IOTPHZ}	T input to Pad high-impedance	0.88	1.01	1.12	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 32 shows the test setup parameters used for measuring input delay.

Table 32: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	V_{REF} – (0.2 x V_{CCO})	V_{REF} + (0.2 x V_{CCO})	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 2.5V	LVPECL_25	1.15 – 0.3	1.15 – 0.3	1.15	

Notes:
1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 6.

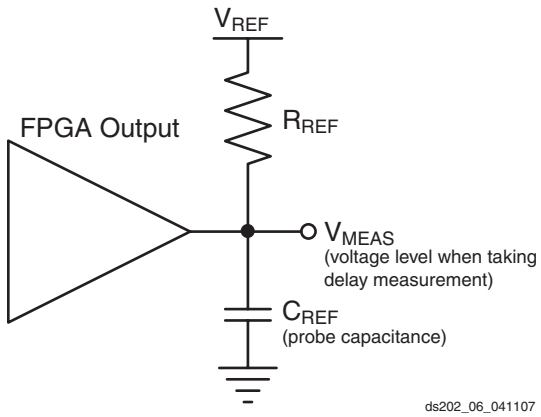

Figure 6: **Generalized Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 33.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual worst-case propagation delay (clock-to-input) of the PCB trace.

Table 33: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10[2]	0.94	0
	PCI33_3 (falling edge)	25	10[2]	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10[2]	0.94	0
	PCI66_3 (falling edge)	25	10[2]	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10[3]	0.94	
	PCIX (falling edge	25	10[3]	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9

Table 33: **Output Delay Measurement Methodology *(Continued)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V_{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	50	0	V_{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V_{REF}	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1M	0	0.90	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.

Input/Output Logic Switching Characteristics

Table 34: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.43 –0.24	0.49 –0.24	0.59 –0.24	ns
T_{ISRCK}/T_{ICKSR}	SR/REV pin Setup/Hold with respect to CLK	0.85 –0.20	1.00 –0.20	1.22 –0.20	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.34 –0.12	0.37 –0.12	0.39 –0.12	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.31 –0.09	0.33 –0.09	0.36 –0.08	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no Delay	0.24	0.26	0.30	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.20	0.22	0.26	ns
Sequential Delays					
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.44	0.50	0.58	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.41	0.46	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.47	0.52	0.60	ns
T_{RQ}	SR/REV pin to OQ/TQ out	1.12	1.28	1.53	ns
T_{GSRQ}	Global Set/Reset to Q outputs	7.30	7.30	10.10	ns
Set/Reset					
T_{RPW}	Minimum Pulse Width, SR/REV inputs	0.78	0.95	1.20	ns, Min

Table 35: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.30 –0.21	0.36 –0.21	0.44 –0.21	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.16 –0.07	0.19 –0.07	0.23 –0.07	ns
T_{OSRCK}/T_{OCKSR}	SR/REV pin Setup/Hold with respect to CLK	0.93 –0.20	1.02 –0.20	1.16 –0.20	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.28 –0.18	0.34 –0.18	0.41 –0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.20 –0.06	0.23 –0.06	0.29 –0.06	ns
Combinatorial					
T_{DOQ}	D1 to OQ out or T1 to TQ out	0.62	0.70	0.83	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out	0.61	0.62	0.62	ns
T_{RQ}	SR/REV pin to OQ/TQ out	1.63	1.89	2.27	ns
T_{GSRQ}	Global Set/Reset to Q outputs	7.30	7.30	10.10	ns
Set/Reset					
T_{RPW}	Minimum Pulse Width, SR/REV inputs	0.80	0.98	1.25	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 36: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.10 0.00	0.11 0.00	0.12 0.00	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.43 –0.24	0.49 –0.24	0.59 –0.24	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.03 0.11	0.04 0.13	0.06 0.15	ns
Setup/Hold for Data Lines					
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.34 –0.12	0.37 –0.12	0.39 –0.12	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.31 –0.09	0.33 –0.09	0.36 –0.08	ns
T_{ISDCK_DDR} /T_{ISCKD_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.34 –0.12	0.37 –0.12	0.39 –0.12	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)	0.31 –0.09	0.33 –0.09	0.36 –0.08	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.51	0.60	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.20	0.22	0.26	ns

Notes:
1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics Input Delay Switching Characteristics

Table 37: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup/Hold					
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.21 –0.02	0.24 –0.02	0.30 –0.02	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.28 –0.18	0.34 –0.18	0.41 –0.18	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.21 –0.03	0.24 –0.03	0.28 –0.03	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.16 –0.07	0.19 –0.07	0.23 –0.07	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.52	0.58	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.20 –0.06	0.23 –0.06	0.29 –0.06	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.59	0.60	0.61	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.61	0.62	0.62	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ Out	0.62	0.70	0.83	ns
T_{OSCO_OQ}	Asynchronous Reset to OQ	1.57	1.82	2.19	ns
T_{OSCO_TQ}	Asynchronous Reset to TQ	1.63	1.89	2.27	ns

Notes:
1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Table 38: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution	$1/(64 \times F_{REF} \times 1e^6)$(1)			ps
$T_{IDELAYCTRLCO\_RDY}$	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency	200.00	200.00	200.00	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50.00	50.00	50.00	ns
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern	0	0	0	Note 2
	Pattern dependent period jitter in delay chain for randon data pattern (PRBS 23)	±5	±5	±5	Note 2
$T_{IODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IODELAY	300	250	250	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.29 –0.06	0.34 –0.06	0.42 –0.06	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.18 0.02	0.20 0.04	0.24 0.06	ns
T_{IODCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.25 –0.12	0.28 –0.12	0.33 –0.12	ns

Notes:
1. Average Tap Delay at 200 MHz = 78 ps.
2. Units in ps, peak-to-peak per tap, in High Performance mode.

CLB Switching Characteristics

Table 39: **CLB Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A	0.08	0.09	0.10	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.31	0.35	0.40	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.67	0.77	0.90	ns, Max
T_{AXA}	AX inputs to AMUX output	0.39	0.44	0.53	ns, Max
T_{AXB}	AX inputs to BMUX output	0.46	0.52	0.61	ns, Max
T_{AXC}	AX inputs to CMUX output	0.31	0.36	0.42	ns, Max
T_{AXD}	AX inputs to DMUX output	0.55	0.62	0.73	ns, Max
T_{BXB}	BX inputs to BMUX output	0.36	0.41	0.48	ns, Max
T_{BXD}	BX inputs to DMUX output	0.45	0.51	0.59	ns, Max
T_{CXB}	CX inputs to CMUX output	0.33	0.36	0.42	ns, Max
T_{CXD}	CX inputs to DMUX output	0.37	0.42	0.49	ns, Max
T_{DXD}	DX inputs to DMUX output	0.38	0.42	0.49	ns, Max

Table 39: **CLB Switching Characteristics *(Continued)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{OPCYA}	An input to COUT output	0.43	0.50	0.59	ns, Max
T_{OPCYB}	Bn input to COUT output	0.39	0.44	0.51	ns, Max
T_{OPCYC}	Cn input to COUT output	0.33	0.37	0.43	ns, Max
T_{OPCYD}	Dn input to COUT output	0.30	0.34	0.40	ns, Max
T_{AXCY}	AX input to COUT output	0.36	0.42	0.50	ns, Max
T_{BXCY}	BX input to COUT output	0.26	0.30	0.37	ns, Max
T_{CXCY}	CX input to COUT output	0.20	0.22	0.26	ns, Max
T_{DXCY}	DX input to COUT output	0.20	0.22	0.26	ns, Max
T_{BYP}	CIN input to COUT output	0.09	0.10	0.11	ns, Max
T_{CINA}	CIN input to AMUX output	0.24	0.27	0.31	ns, Max
T_{CINB}	CIN input to BMUX output	0.27	0.30	0.35	ns, Max
T_{CINC}	CIN input to CMUX output	0.29	0.32	0.36	ns, Max
T_{CIND}	CIN input to DMUX output	0.31	0.35	0.41	ns, Max
Sequential Delays					
T_{CKO}	Clock to AQ – DQ outputs	0.35	0.40	0.47	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.36 0.19	0.41 0.21	0.49 0.24	ns, Min
T_{RCK}	DX input to CLK when used as REV	0.37	0.42	0.51	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK on A – D Flip Flops	0.18 –0.04	0.20 –0.04	0.23 –0.04	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.41 –0.19	0.49 –0.19	0.59 –0.19	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.14 0.14	0.16 0.16	0.18 0.19	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width	0.90	0.90	0.90	ns, Min
T_{RQ}	Delay from SR or REV input to AQ – DQ flip-flops	0.74	0.86	1.03	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.46	0.52	0.63	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1265	1098	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 40: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Sequential Delays					
T_{SHCKO}	Clock to A – B outputs	1.08	1.26	1.54	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.19	1.38	1.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS}/T_{DH}	A – D inputs to CLK	0.72 0.20	0.84 0.22	1.03 0.26	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.41 0.20	0.46 0.22	0.54 0.27	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.34 –0.06	0.39 –0.04	0.46 –0.02	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.36 –0.08	0.42 –0.07	0.51 –0.06	ns, Min
Clock CLK					
T_{MPW}	Minimum pulse width	0.70	0.82	1.00	ns, Min
T_{MCP}	Minimum clock period	1.40	1.64	2.00	ns, Min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 41: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Sequential Delays					
T_{REG}	Clock to A – D outputs	1.23	1.43	1.73	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.33	1.55	1.87	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.99	1.15	1.38	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{WS}/T_{WH}	WE input	0.21 –0.06	0.24 –0.04	0.29 –0.02	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.23 –0.08	0.27 –0.07	0.33 –0.06	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.57 0.07	0.66 0.09	0.78 0.11	ns, Min

Table 41: **CLB Shift Register Switching Characteristics *(Continued)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Clock CLK					
T_{MPW}	Minimum pulse width	0.60	0.70	0.85	ns, Min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 42: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Block RAM and FIFO Clock to Out Delays					
T_{RCKO_DO} and T_{RCKO_DOR}(1)	Clock CLK to DOUT output (without output register)(2)(3)	1.79	1.92	2.19	ns, Max
	Clock CLK to DOUT output (with output register)(4)(5)	0.61	0.69	0.82	ns, Max
	Clock CLK to DOUT output with ECC (without output register)(2)(3)	2.64	3.03	3.61	ns, Max
	Clock CLK to DOUT output with ECC (with output register)(4)(5)	0.66	0.77	0.93	ns, Max
	Clock CLK to DOUT output with Cascade (without output register)(2)	2.10	2.44	2.94	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)(4)	0.91	1.07	1.30	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs(6)	0.76	0.87	1.02	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointer outputs(7)	1.10	1.26	1.48	ns, Max
T_{RCKO_ECCR}	Clock CLK to BITERR (with output register)	0.66	0.77	0.93	ns, Max
T_{RCKO_ECC}	Clock CLK to BITERR (without output register)	2.48	2.85	3.41	ns, Max
	Clock CLK to ECCPARITY in standard ECC mode	1.29	1.47	1.74	ns, Max
	Clock CLK to ECCPARITY in ECC encode only mode	0.77	0.89	1.05	ns, Max

Table 42: **Block RAM and FIFO Switching Characteristics *(Continued)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Setup and Hold Times Before/After Clock CLK					
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs	0.34 0.30	0.40 0.32	0.48 0.36	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(8)	0.27 0.28	0.30 0.28	0.35 0.29	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with ECC in standard mode(8)	0.33 0.32	0.37 0.33	0.42 0.36	ns, Min
	DIN inputs with ECC encode only(8)	0.68 0.32	0.72 0.33	0.77 0.36	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.32 0.15	0.36 0.15	0.42 0.15	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.15 0.22	0.16 0.24	0.18 0.27	ns, Min
$T_{RCCK\_SSR}/T_{RCKC\_SSR}$	Synchronous Set/ Reset (SSR) input	0.17 0.23	0.21 0.25	0.26 0.28	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.44 0.16	0.51 0.17	0.63 0.18	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN/RDEN FIFO inputs(9)	0.36 0.30	0.41 0.34	0.48 0.40	ns, Min
Reset Delays					
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(10)	1.10	1.26	1.48	ns, Max
Maximum Frequency					
F_{MAX}	Block RAM in all modes	550	500	450	MHz
$F_{MAX\_CASCADE}$	Block RAM in Cascade mode	500	450	400	MHz
F_{MAX_FIFO}	FIFO in all modes	550	500	450	MHz
F_{MAX_ECC}	Block RAM in ECC mode	415	375	325	MHz

Notes:
1. Trace will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
9. These parameters also apply to RDEN.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

DSP48E Switching Characteristics

Table 43: **DSP48E Switching Characteristics**

Symbol	Description	Speed			Units
		-3	-2	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
TDSPDCK_{AA, BB, ACINA, BCINB}/ TDSPCKD_{AA, BB, ACINA, BCINB}	{A, B, ACIN, BCIN} input to {A, B} register CLK	0.17 0.17	0.21 0.23	0.26 0.30	ns
TDSPDCK_CC/TDSPCKD_CC	C input to C register CLK	0.14 0.26	0.16 0.31	0.20 0.37	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
TDSPDCK_{AM, BM, ACINM, BCINM}/ TDSPCKD_{AM, BM, ACINM, BCINM}	{A, B, ACIN, BCIN} input to M register CLK	1.30 0.19	1.44 0.19	1.71 0.19	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
TDSPDCK_{AP, BP, ACINP, BCINP}_M/ TDSPCKD_{AP, BP, ACINP, BCINP}_M	{A, B, ACIN, BCIN} input to P register CLK using multiplier	2.39 –0.30	2.74 –0.30	3.25 –0.30	ns
TDSPDCK_{AP, BP, ACINP, BCINP}_NM/ TDSPCKD_{AP, BP, ACINP, BCINP}_NM	{A, B, ACIN, BCIN} input to P register CLK not using multiplier	1.35 –0.10	1.54 –0.10	1.83 –0.10	ns
TDSPDCK_CP/TDSPCKD_CP	C input to P register CLK	1.30 –0.13	1.42 –0.13	1.70 –0.13	ns
TDSPDCK_{PCINP, CRYCINP, MULTSIGNINP}/ TDSPCKD_{PCINP, CRYCINP, MULTSIGNINP}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.06 0.11	1.17 0.11	1.31 0.11	ns
Setup and Hold Times of the CE Pins					
TDSPCCK_{CEA1A, CEA2A, CEB1B, CEB2B}/ TDSPCKC_{CEA1A, CEA2A, CEB1A, CEB2B}	{CEA1, CEA2A, CEB1B, CEB2B} input to {A, B} register CLK	0.24 0.21	0.28 0.25	0.33 0.31	ns
TDSPCCK_CECC/TDSPCKC_CECC	CEC input to C register CLK	0.19 0.17	0.21 0.21	0.26 0.28	ns
TDSPCCK_CEMM/TDSPCKC_CEMM	CEM input to M register CLK	0.25 0.18	0.29 0.21	0.36 0.26	ns
TDSPCCK_CEPP/TDSPCKC_CEPP	CEP input to P register CLK	0.56 0.01	0.63 0.01	0.73 0.01	ns
Setup and Hold Times of the RST Pins					
TDSPCCK_{RSTAA, RSTBB}/ TDSPCKC_{RSTAA, RSTBB}	{RSTA, RSTB} input to {A, B} register CLK	0.24 0.23	0.28 0.26	0.33 0.31	ns
TDSPCCK_RSTCC/ TDSPCKC_RSTCC	RSTC input to C register CLK	0.19 0.17	0.21 0.21	0.26 0.28	ns
TDSPCCK_RSTMM/ TDSPCKC_RSTMM	RSTM input to M register CLK	0.25 0.18	0.29 0.21	0.36 0.26	ns
TDSPCCK_RSTPP/TDSPCKC_RSTPP	RSTP input to P register CLK	0.56 0.01	0.63 0.01	0.73 0.01	ns

Table 43: **DSP48E Switching Characteristics *(Continued)***

Symbol	Description	Speed			Units
		-3	-2	-1	
Combinatorial Delays from Input Pins to Output Pins					
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_M	{A, B} input to {P, CARRYOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_NM	{A, B} input to {P, CARRYOUT} output not using multiplier	1.59	1.77	2.22	ns
TDSPDO_{CP, CCRYOUT, CRYINP, CRYINCRYOUT}	{C, CARRYIN} input to {P, CARRYOUT} output	1.50	1.67	2.08	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
TDSPDO_{AACOUT, BBCOUT}	{A, B} input to {ACOUT, BCOUT} output	1.00	1.12	1.31	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_M	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_NM	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.72	1.92	2.42	ns
TDSPDO_{CPCOUT, CCRYCOUT, CMULTSIGNOUT, CRYINPCOUT, CRYINCRYCOUT, CRYINMULTSIGNOUT}	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.63	1.82	2.28	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_M	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_NM	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.59	1.77	2.22	ns
TDSPDO_{ACINACOUT, BCINBCOUT}	{ACIN, BCIN} input to {ACOUT, BCOUT} output	1.00	1.12	1.31	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_M	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_NM	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.72	1.92	2.42	ns
TDSPDO_{PCINP, CRYCINP, MULTSIGNINP, PCINCRYOUT, CRYCINCRYOUT, MULTSIGNINCRYOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.30	1.45	1.82	ns
TDSPDO_{PCINPCOUT, CRYCINPCOUT, MULTSIGNINPCOUT, PCINCRYCOUT, CRYCINCRYCOUT, MULTSIGNINCRYCOUT, PCINMULTSIGNOUT, CRYCINMULTSIGNOUT, MULTSIGNINMULTSIGNOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.43	1.60	2.02	ns
Clock to Outs from Output Register Clock to Output Pins					
TDSPCKO_{PP, CRYOUTP}	CLK (PREG) to {P, CARRYOUT} output	0.45	0.48	0.56	ns
TDSPCKO_{CRYCOUTP, PCOUTP, MULTSIGNOUTP}	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.48	0.53	0.62	ns

Table 43: **DSP48E Switching Characteristics *(Continued)***

Symbol	Description	Speed			Units
		-3	-2	-1	
Clock to Outs from Pipeline Register Clock to Output Pins					
TDSPCKO_{PM, CRYOUTM}	CLK (MREG) to {P, CARRYOUT} output	1.81	2.10	2.47	ns
TDSPCKO_{PCOUTM, CRYCOUTM, MULTSIGNOUTM}	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.91	2.13	2.66	ns
Clock to Outs from Input Register Clock to Output Pins					
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_M	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.09	3.57	4.23	ns
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_NM	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	1.90	2.11	2.63	ns
TDSPCKO_{PC, CRYOUTC}	CLK (CREG) to {P, CARRYOUT} output	1.89	2.11	2.62	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
TDSPCKO_{ACOUTA, BCOUTB}	CLK (AREG, BREG) to {ACOUT, BCOUT}	0.61	0.68	0.79	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_M	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.09	3.57	4.23	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_NM	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.03	2.27	2.82	ns
TDSPCKO_{PCOUTC, CRYCOUTC, MULTSIGNOUTC}	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.03	2.26	2.82	ns
Maximum Frequency					
F_{MAX}	With all registers used	550	500	450	MHz
F_{MAX_PATDET}	With pattern detector	515	465	410	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	374	324	275	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	345	300	254	MHz

Configuration Switching Characteristics

Table 44: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Power-up Timing Characteristics					
T_{PL}	Program Latency	3	3	3	ms, Max
T_{POR}	Power-on-Reset	10 50	10 50	10 50	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	250	ns, Min
Master/Slave Serial Mode Programming Switching(1)					
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0 0.0	4.0 0.0	4.0 0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0 0.0	4.0 0.0	4.0 0.0	ns, Min
T_{CCO}	DOUT	7.5	7.5	7.5	ns, Max
F_{MCCK}	Maximum Frequency, master mode with respect to nominal CCLK.	100	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%
F_{MSCCK}	Slave mode external CCLK	100	100	100	MHz
SelectMAP Mode Programming Switching(1)					
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	3.0 0.5	3.0 0.5	3.0 0.5	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CS_B Setup/Hold	3.0 0.5	3.0 0.5	3.0 0.5	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	8.0 0.5	8.0 0.5	8.0 0.5	ns, Min
T_{SMCKBY}	BUSY Propagation Delay	7.5	7.5	7.5	ns, Max
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	10	10	10	ns, Min
T_{SMCO}	CCLK to DATA out in readback	9.0	9.0	9.0	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback	7.5	7.5	7.5	ns, Max
F_{SMCCK}	Maximum Frequency, master mode with respect to nominal CCLK.	100	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}	TMS and TDI Setup time before TCK	1.0	1.0	1.0	ns, Min
T_{TCKTAP}	TMS and TDI Hold time after TCK	2.0	2.0	2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid	6	6	6	ns, Max

Table 44: **Configuration Switching Characteristics *(Continued)***

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{TCK}	Maximum configuration TCK clock frequency	66	66	66	MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching					
T_{BPICCO}(4)	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge	10	10	10	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	3.0 0.5	3.0 0.5	3.0 0.5	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3.0	3.0	3.0	CCLK cycles
SPI Master Flash Mode Programming Switching					
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge	4.0 0.0	4.0 0.0	4.0 0.0	ns
T_{SPICCM}	MOSI clock to out	10	10	10	ns
$T_{SPICCFC}$	FCS_B clock to out	10	10	10	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	µs
CCLK Output (Master Modes)					
T_{MCCKL}	Master CCLK clock minimum Low time	3.0	3.0	3.0	ns, Min
T_{MCCKH}	Master CCLK clock minimum High time	3.0	3.0	3.0	ns, Min
CCLK Input (Slave Modes)					
T_{SCCKL}	Slave CCLK clock minimum Low time	2.0	2.0	2.0	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.0	2.0	2.0	ns, Min
Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK					
F_{DCK}	Maximum frequency for DCLK	500	450	400	MHz
$T_{DMCCK\_DADDR}/T_{DMCKC\_DADDR}$	DADDR Setup/Hold	1.2 0.0	1.35 0.0	1.56 0.0	ns
$T_{DMCCK\_DI}/T_{DMCKC\_DI}$	DI Setup/Hold	1.2 0.0	1.35 0.0	1.56 0.0	ns
$T_{DMCCK\_DEN}/T_{DMCKC\_DEN}$	DEN Setup/Hold time	1.2 0.0	1.35 0.0	1.56 0.0	ns
$T_{DMCCK\_DWE}/T_{DMCKC\_DWE}$	DWE Setup/Hold time	1.2 0.0	1.35 0.0	1.56 0.0	ns
T_{DMCKO_DO}	CLK to out of DO(3)	1.0	1.12	1.3	ns
$T_{DMCKO\_DRDY}/T_{DMCKCO\_DRDY}$	CLK to out of DRDY	1.0	1.12	1.3	ns

Notes:
1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in **UG190**: *Virtex-5 User Guide*.
3. DO will hold until next DRP operation.
4. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

Clock Buffers and Networks

Table 45: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.27 0.00	0.27 0.00	0.31 0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.27 0.00	0.27 0.00	0.31 0.00	ns
T_{BCCKO_O}	BUFGCTRL delay from I0/I1 to O	0.19	0.22	0.25	ns
T_{BGCKO_O}	BUFG delay from I0 to O	0.19	0.22	0.25	ns
Maximum Frequency					
F_{MAX}	Global clock tree (BUFG) for LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, and SX50T devices	710	650	600	MHz
F_{MAX}	Global clock tree (BUFG) for LX220, LX220T, LX330, LX330T, and SX95T devices	N/A	500	450	MHz

Notes:
1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.

Table 46: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{BUFIOCKO\_O}$	Clock to out delay from I to O	1.08	1.16	1.29	ns
Maximum Frequency					
F_{MAX}	I/O clock tree (BUFIO)	710	710	644	MHz

Table 47: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.56	0.59	0.67	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.23	0.24	0.26	ns
T_{BRDO_CLRO}	Propagation delay from CLR to O	0.61	0.70	0.82	ns
Maximum Frequency					
F_{MAX}	Regional clock tree (BUFR)	300	250	250	MHz

PLL Specification

Table 48: **PLL Specification**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{INMAX}	Maximum Input Clock Frequency	710	710	645	MHz
F_{INMIN}	Minimum Input Clock Frequency	19	19	19	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	<20% of clock input period or 1 ns Max			
F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25/75			%
	Allowable Input Duty Cycle: 50—199 MHz	30/70			%
	Allowable Input Duty Cycle: 200—399 MHz	35/65			%
	Allowable Input Duty Cycle: 400—499 MHz	40/60			%
	Allowable Input Duty Cycle: >500 MHz	45/55			%
F_{VCOMIN}	Minimum PLL VCO Frequency	400	400	400	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	1440	1200	1000	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical	1	1	1	MHz
	High PLL Bandwidth at Typical	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	120	120	120	ps
$T_{OUTJITTER}$	PLL Output Jitter(1)	Note 1			
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(2)	150	200	200	ps
$T_{LOCKMAX}$	PLL Maximum Lock Time(4)	100	100	100	µs
F_{OUTMAX}	PLL Maximum Output Frequency for LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, and SX50T devices	710	650	600	MHz
	PLL Maximum Output Frequency for LX220, LX220T, LX330, LX330T, and SX95T devices	N/A	500	450	MHz
F_{OUTMIN}	PLL Minimum Output Frequency(3)	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	<20% of clock input period or 1 ns Max			
$RST_{MINPULSE}$	Minimum Reset Pulse Width	5	5	5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	550	500	450	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19	19	19	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle			

Notes:
1. Values for this parameter are available in the Architecture Wizard.
2. Includes global clock buffer.
3. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
4. The LOCK signal must be sampled after TLOCKMAX. The LOCK signal is invalid after configuration or reset until the TLOCKMAX time has expired.

DCM Switching Characteristics

Table 49: **Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Outputs Clocks (Low Frequency Mode)					
$F_{1XLFMSMIN}$	CLK0, CLK90, CLK180, CLK270	32.00	32.00	32.00	MHz
$F_{1XLFMSMAX}$		150.00	135.00	120.00	MHz
$F_{2XLFMSMIN}$	CLK2X, CLK2X180	64.00	64.00	64.00	MHz
$F_{2XLFMSMAX}$		300.00	270.00	240.00	MHz
$F_{DVLFMSMIN}$	CLKDV	2.0	2.0	2.0	MHz
$F_{DVLFMSMAX}$		100.00	90.00	80.00	MHz
$F_{FXLFMSMIN}$	CLKFX, CLKFX180	32.00	32.00	32.00	MHz
$F_{FXLFMSMAX}$		180.00	160.00	140.00	MHz
Input Clocks (Low Frequency Mode)					
$F_{DLLLFMSMIN}$	CLKIN (using DLL outputs)(1, 3, 4)	32.00	32.00	32.00	MHz
$F_{DLLLFMSMAX}$		150.00	135.00	120.00	MHz
$F_{CLKINLFFXMSMIN}$	CLKIN (using DFS outputs only)(2, 3, 4)	1.00	1.00	1.00	MHz
$F_{CLKINLFFXMSMAX}$		180.00	160.00	140.00	MHz
$F_{PSCLKLFMSMIN}$	PSCLK	1.00	1.00	1.00	KHz
$F_{PSCLKLFMSMAX}$		550.00	500.00	450.00	MHz
Outputs Clocks (High Frequency Mode)					
$F_{1XHFMSMIN}$	CLK0, CLK90, CLK180, CLK270	120.00	120.00	120.00	MHz
$F_{1XHFMSMAX}$		550.00	500.00	450.00	MHz
$F_{2XHFMSMIN}$	CLK2X, CLK2X180	240.00	240.00	240.00	MHz
$F_{2XHFMSMAX}$		550.00	500.00	450.00	MHz
$F_{DVHFMSMIN}$	CLKDV	7.5	7.5	7.5	MHz
$F_{DVHFMSMAX}$		366.67	333.34	300.00	MHz
$F_{FXHFMSMIN}$	CLKFX, CLKFX180	140.00	140.00	140.00	MHz
$F_{FXHFMSMAX}$		400.00	375.00	350.00	MHz
Input Clocks (High Frequency Mode)					
$F_{DLLHFMSMIN}$	CLKIN (using DLL outputs)(1, 3, 4)	120.00	120.00	120.00	MHz
$F_{DLLHFMSMAX}$		550.00	500.00	450.00	MHz
$F_{CLKINHFFXMSMIN}$	CLKIN (using DFS outputs only)(2, 3, 4)	25.00	25.00	25.00	MHz
$F_{CLKINHFFXMSMAX}$		400.00	375.00	350.00	MHz
$F_{PSCLKHFMSMIN}$	PSCLK	1.00	1.00	1.00	KHz
$F_{PSCLKHFMSMAX}$		550.00	500.00	450.00	MHz

Notes:
1. DLL outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN_DIVIDE_BY_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN_DIVIDE_BY_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 50: **Operating Frequency Ranges for DCM in Maximum Range (MR) Mode**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Outputs Clocks (Low Frequency Mode)					
$F_{1XMRMIN}$	CLK0, CLK90, CLK180, CLK270	19.00	19.00	19.00	MHz
$F_{1XMRMAX}$		32.00	32.00	32.00	MHz
$F_{2XMRMIN}$	CLK2X, CLK2X180	38.00	38.00	38.00	MHz
$F_{2XMRMAX}$		64.00	64.00	64.00	MHz
$F_{DLLMRMIN}$	CLKDV	1.19	1.19	1.19	MHz
$F_{DLLMRMAX}$		21.34	21.34	21.34	MHz
$F_{FXMRMIN}$	CLKFX, CLKFX180	19.00	19.00	19.00	MHz
$F_{FXMRMAX}$		40.00	40.00	40.00	MHz
Input Clocks (Low Frequency Mode)					
$F_{CLKINDLLMRMIN}$	CLKIN (using DLL outputs)(1, 3, 4)	19.00	19.00	19.00	MHz
$F_{CLKINDLLMRMAX}$		32.00	32.00	32.00	MHz
$F_{CLKINFXMRMIN}$	CLKIN (using DFS outputs only)(2, 3, 4)	1.00	1.00	1.00	MHz
$F_{CLKINFXMRMAX}$		40.00	40.00	40.00	MHz
$F_{PSCLKMRMIN}$	PSCLK	1.00	1.00	1.00	KHz
$F_{PSCLKMRMAX}$		300.00	270.00	240.00	MHz

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN_DIVIDE_BY_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN_DIVIDE_BY_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 51: **Input Clock Tolerances**

Symbol	Description	Frequency Range	Value		Units
Duty Cycle Input Tolerance (in %)					
$T_{DUTYCYCRANGE\_1}$	PSCLK only	< 1 MHz	25 - 75		%
$T_{DUTYCYCRANGE\_1\_50}$	PSCLK and CLKIN	1 - 50 MHz	25 - 75		%
$T_{DUTYCYCRANGE\_50\_100}$		50 - 100 MHz	30 - 70		%
$T_{DUTYCYCRANGE\_100\_200}$		100 - 200 MHz	40 - 60		%
$T_{DUTYCYCRANGE\_200\_400}$		200 - 400 MHz(4)	45 - 55		%
$T_{DUTYCYCRANGE\_400}$		> 400 MHz	45 - 55		%
		Speed Grade			
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)		**-3**	**-2**	**-1**	**Units**
$T_{CYCLFDLL}$	CLKIN (using DLL outputs)(1)	300.00	300.00	345.00	ps
$T_{CYCLFFX}$	CLKIN (using DFS outputs)(2)	300.00	300.00	345.00	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)					
$T_{CYCHFDLL}$	CLKIN (using DLL outputs)(1)	150.00	150.00	173.00	ps
$T_{CYCHFFX}$	CLKIN (using DFS outputs)(2)	150.00	150.00	173.00	ps
Input Clock Period Jitter (Low Frequency Mode)					
$T_{PERLFDLL}$	CLKIN (using DLL outputs)(1)	1.00	1.00	1.15	ns
$T_{PERLFFX}$	CLKIN (using DFS outputs)(2)	1.00	1.00	1.15	ns
Input Clock Period Jitter (High Frequency Mode)					
$T_{PERHFDLL}$	CLKIN (using DLL outputs)(1)	1.00	1.00	1.15	ns
$T_{PERHFFX}$	CLKIN (using DFS outputs)(2)	1.00	1.00	1.15	ns
Feedback Clock Path Delay Variation					
$T_{CLKFB\_DELAY\_VAR}$	CLKFB off-chip feedback	1.00	1.00	1.15	ns

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. If both DLL and DFS outputs are used, follow the more restrictive specifications.
4. This duty cycle specification does not apply to the GTP_DUAL to DCM connection. The GTP transceivers drive the DCMs at the following frequencies: 320 MHz for -1 speed grade devices, 375 MHz for -2 speed grade devices, or 375 MHz for -3 speed grade devices.

Output Clock Jitter

Table 52: **Output Clock Jitter**

Symbol	Description	Constraints	Speed Grade			Units
			-3	-2	-1	
Clock Synthesis Period Jitter						
$T_{PERJITT\_0}$	CLK0		±120	±120	±120	ps
$T_{PERJITT\_90}$	CLK90		±120	±120	±120	ps
$T_{PERJITT\_180}$	CLK180		±120	±120	±120	ps
$T_{PERJITT\_270}$	CLK270		±120	±120	±120	ps
$T_{PERJITT\_2X}$	CLK2X, CLK2X180		±200	±200	±230	ps
$T_{PERJITT\_DV1}$	CLKDV (integer division)		±150	±150	±180	ps
$T_{PERJITT\_DV2}$	CLKDV (non-integer division)		±300	±300	±345	ps
$T_{PERJITT\_FX}$	CLKFX, CLKFX180		Note 1	Note 1	Note 1	ps

Notes:
1. Values for this parameter are available in the Architecture Wizard.

Output Clock Phase Alignment

Table 53: **Output Clock Phase Alignment**

Symbol	Description	Constraints	Speed Grade			Units
			-3	-2	-1	
Phase Offset Between CLKIN and CLKFB						
$T_{IN\_FB\_OFFSET}$	CLKIN/CLKFB		±50	±50	±60	ps
Phase Offset Between Any DCM Outputs(4)						
$T_{OUT\_OFFSET\_1X}$	CLK0, CLK90, CLK180, CLK270		±140	±140	±160	ps
$T_{OUT\_OFFSET\_2X}$	CLK2X, CLK2X180, CLKDV		±150	±150	±200	ps
$T_{OUT\_OFFSET\_FX}$	CLKFX, CLKFX180		±160	±160	±220	ps
Duty Cycle Precision						
$T_{DUTY\_CYC\_DLL}$(3)	DLL outputs(1)		±150	±150	±180	ps
$T_{DUTY\_CYC\_FX}$	DFS outputs(2)		±150	±150	±180	ps

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
4. All phase offsets are in respect to group CLK1X.

Table 54: **Miscellaneous Timing Parameters**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Time Required to Achieve LOCK					
T_{DLL_240}	DLL output – Frequency range > 240 MHz (1)	80.00	80.00	80.00	µs
$T_{DLL\_120\_240}$	DLL output – Frequency range 120 - 240 MHz (1)	250.00	250.00	250.00	µs
$T_{DLL\_60\_120}$	DLL output – Frequency range 60 - 120 MHz (1)	900.00	900.00	900.00	µs
$T_{DLL\_50\_60}$	DLL output – Frequency range 50 - 60 MHz(1)	1300.00	1300.00	1300.00	µs
$T_{DLL\_40\_50}$	DLL output – Frequency range 40 - 50 MHz (1)	2000.00	2000.00	2000.00	µs
$T_{DLL\_30\_40}$	DLL output – Frequency range 30 - 40 MHz (1)	3600.00	3600.00	3600.00	µs
$T_{DLL\_24\_30}$	DLL output – Frequency range 24 - 30 MHz(1)	5000.00	5000.00	5000.00	µs
T_{DLL_30}	DLL output – Frequency range < 30 MHz (1)	5000.00	5000.00	5000.00	µs
T_{FX_MIN}	DFS outputs(2)	10.00	10.00	10.00	ms
T_{FX_MAX}		10.00	10.00	10.00	ms
$T_{DLL\_FINE\_SHIFT}$	Multiplication factor for DLL lock time with Fine Shift	2.00	2.00	2.00	
Fine Phase Shifting					
T_{RANGE_MS}	Absolute shifting range in maximum speed mode	7.00	7.00	7.00	ns
T_{RANGE_MR}	Absolute shifting range in maximum range mode	10.00	10.00	10.00	ns
Delay Lines					
$T_{TAP\_MS\_MIN}$	Tap delay resolution (Min) in maximum speed mode	7.00	7.00	7.00	ps
$T_{TAP\_MS\_MAX}$	Tap delay resolution (Max) in maximum speed mode	30.00	30.00	30.00	ps
$T_{TAP\_MR\_MIN}$	Tap delay resolution (Min) in maximum range mode	10.00	10.00	10.00	ps
$T_{TAP\_MR\_MAX}$	Tap delay resolution (Max) in maximum range mode	40.00	40.00	40.00	ps

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 55: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	33
CLKFX_DIVIDE	1	32

Table 56: **DCM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{DMCCK_PSEN}/ T_{DMCKC_PSEN}	PSEN Setup/Hold	1.20 0.00	1.35 0.00	1.56 0.00	ns
$T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$	PSINCDEC Setup/Hold	1.20 0.00	1.35 0.00	1.56 0.00	ns
T_{DMCKO_PSDONE}	Clock to out of PSDONE	1.00	1.12	1.30	ns

Virtex-5 Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 57. Values are expressed in nanoseconds unless otherwise noted.

Table 57: **Global Clock Input to Output Delay Without DCM or PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL						
T_{ICKOF}	Global Clock and OUTFF *without* DCM or PLL	XC5VLX30	5.54	6.04	6.73	ns
		XC5VLX30T	5.54	6.04	6.73	ns
		XC5VLX50	5.59	6.09	6.79	ns
		XC5VLX50T	5.59	6.09	6.79	ns
		XC5VLX85	5.78	6.28	6.99	ns
		XC5VLX85T	5.78	6.28	6.99	ns
		XC5VLX110	5.84	6.35	7.06	ns
		XC5VLX110T	5.84	6.35	7.06	ns
		XC5VLX220	N/A	6.99	7.71	ns
		XC5VLX220T	N/A	6.99	7.71	ns
		XC5VLX330	N/A	7.17	7.91	ns
		XC5VLX330T	N/A	7.17	7.91	ns
		XC5VSX35T	5.72	6.22	6.92	ns
		XC5VSX50T	5.77	6.27	6.97	ns
		XC5VSX95T	N/A	6.59	7.30	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 58: **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode.						
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XC5VLX30	2.33	2.56	2.93	ns
		XC5VLX30T	2.33	2.56	2.93	ns
		XC5VLX50	2.35	2.58	2.95	ns
		XC5VLX50T	2.35	2.58	2.95	ns
		XC5VLX85	2.41	2.63	3.00	ns
		XC5VLX85T	2.41	2.63	3.00	ns
		XC5VLX110	2.46	2.69	3.06	ns
		XC5VLX110T	2.46	2.69	3.06	ns
		XC5VLX220	N/A	2.83	3.18	ns
		XC5VLX220T	N/A	2.83	3.18	ns
		XC5VLX330	N/A	3.00	3.37	ns
		XC5VLX330T	N/A	3.00	3.37	ns
		XC5VSX35T	2.44	2.67	3.03	ns
		XC5VSX50T	2.46	2.69	3.05	ns
		XC5VSX95T	N/A	2.64	3.00	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 59: **Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode.						
$T_{ICKOFDCM\_0}$	Global Clock and OUTFF *with* DCM	XC5VLX30	3.45	3.71	4.15	ns
		XC5VLX30T	3.45	3.71	4.15	ns
		XC5VLX50	3.47	3.73	4.17	ns
		XC5VLX50T	3.47	3.73	4.17	ns
		XC5VLX85	3.60	3.86	4.29	ns
		XC5VLX85T	3.60	3.86	4.29	ns
		XC5VLX110	3.65	3.92	4.36	ns
		XC5VLX110T	3.65	3.92	4.36	ns
		XC5VLX220	N/A	4.41	4.85	ns
		XC5VLX220T	N/A	4.41	4.85	ns
		XC5VLX330	N/A	4.58	5.04	ns
		XC5VLX330T	N/A	4.58	5.04	ns
		XC5VSX35T	3.63	3.89	4.33	ns
		XC5VSX50T	3.65	3.91	4.35	ns
		XC5VSX95T	N/A	4.16	4.59	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 60: **Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in System-Synchronous Mode.						
$T_{ICKOFPLL}$	Global Clock and OUTFF *with* PLL	XC5VLX30	2.03	2.12	2.41	ns
		XC5VLX30T	2.03	2.12	2.41	ns
		XC5VLX50	2.05	2.14	2.43	ns
		XC5VLX50T	2.05	2.14	2.43	ns
		XC5VLX85	2.10	2.18	2.47	ns
		XC5VLX85T	2.10	2.18	2.47	ns
		XC5VLX110	2.16	2.24	2.54	ns
		XC5VLX110T	2.16	2.24	2.54	ns
		XC5VLX220	N/A	2.58	2.86	ns
		XC5VLX220T	N/A	2.58	2.86	ns
		XC5VLX330	N/A	2.75	3.05	ns
		XC5VLX330T	N/A	2.75	3.05	ns
		XC5VSX35T	2.14	2.22	2.51	ns
		XC5VSX50T	2.16	2.24	2.53	ns
		XC5VSX95T	N/A	2.32	2.60	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 61: **Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in Source-Synchronous Mode.						
$T_{ICKOFPLL\_0}$	Global Clock and OUTFF *with* PLL	XC5VLX30	3.98	4.33	4.82	ns
		XC5VLX30T	3.98	4.33	4.82	ns
		XC5VLX50	4.01	4.35	4.84	ns
		XC5VLX50T	4.01	4.35	4.84	ns
		XC5VLX85	4.13	4.47	4.96	ns
		XC5VLX85T	4.13	4.47	4.96	ns
		XC5VLX110	4.19	4.53	5.03	ns
		XC5VLX110T	4.19	4.53	5.03	ns
		XC5VLX220	N/A	5.03	5.53	ns
		XC5VLX220T	N/A	5.03	5.53	ns
		XC5VLX330	N/A	5.20	5.71	ns
		XC5VLX330T	N/A	5.20	5.71	ns
		XC5VSX35T	4.16	4.51	5.00	ns
		XC5VSX50T	4.19	4.53	5.02	ns
		XC5VSX95T	N/A	4.77	5.27	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 62: **Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in System-Synchronous Mode.						
$T_{ICKOFDCM\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC5VLX30	2.47	2.70	3.06	ns
		XC5VLX30T	2.47	2.70	3.06	ns
		XC5VLX50	2.49	2.72	3.08	ns
		XC5VLX50T	2.49	2.72	3.08	ns
		XC5VLX85	2.55	2.77	3.13	ns
		XC5VLX85T	2.55	2.77	3.13	ns
		XC5VLX110	2.60	2.83	3.19	ns
		XC5VLX110T	2.60	2.83	3.19	ns
		XC5VLX220	N/A	2.97	3.31	ns
		XC5VLX220T	N/A	2.97	3.31	ns
		XC5VLX330	N/A	3.14	3.49	ns
		XC5VLX330T	N/A	3.14	3.49	ns
		XC5VSX35T	2.58	2.81	3.16	ns
		XC5VSX50T	2.60	2.83	3.18	ns
		XC5VSX95T	N/A	2.78	3.13	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 63: **Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in Source-Synchronous Mode.						
$T_{ICKOFDCM0\_PLL}$	Global Clock and OUTFF with DCM and PLL	XC5VLX30	3.59	3.85	4.27	ns
		XC5VLX30T	3.59	3.85	4.27	ns
		XC5VLX50	3.61	3.87	4.29	ns
		XC5VLX50T	3.61	3.87	4.29	ns
		XC5VLX85	3.74	4.00	4.42	ns
		XC5VLX85T	3.74	4.00	4.42	ns
		XC5VLX110	3.79	4.06	4.48	ns
		XC5VLX110T	3.79	4.06	4.48	ns
		XC5VLX220	N/A	4.55	4.98	ns
		XC5VLX220T	N/A	4.55	4.98	ns
		XC5VLX330	N/A	4.72	5.17	ns
		XC5VLX330T	N/A	4.72	5.17	ns
		XC5VSX35T	3.77	4.03	4.45	ns
		XC5VSX50T	3.79	4.05	4.48	ns
		XC5VSX95T	N/A	4.30	4.72	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Virtex-5 Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 65. Values are expressed in nanoseconds unless otherwise noted.

Table 64: **Global Clock Setup and Hold Without DCM or PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock and IFF(2) without DCM or PLL	XC5VLX30	1.49 –0.35	1.60 –0.35	1.77 –0.35	ns
		XC5VLX30T	1.49 –0.35	1.60 –0.35	1.76 –0.35	ns
		XC5VLX50	1.48 –0.30	1.59 –0.30	1.76 –0.30	ns
		XC5VLX50T	1.48 –0.30	1.59 –0.30	1.76 –0.30	ns
		XC5VLX85	1.75 –0.49	1.89 –0.49	2.09 –0.49	ns
		XC5VLX85T	1.75 –0.49	1.89 –0.49	2.09 –0.49	ns
		XC5VLX110	1.74 –0.43	1.88 –0.43	2.09 –0.43	ns
		XC5VLX110T	1.73 –0.43	1.88 –0.43	2.09 –0.43	ns
		XC5VLX220	N/A	2.57 –0.74	2.86 –0.74	ns
		XC5VLX220T	N/A	2.57 –0.74	2.86 –0.74	ns
		XC5VLX330	N/A	2.55 –0.56	2.85 –0.56	ns
		XC5VLX330T	N/A	2.57 –0.56	2.86 –0.56	ns
		XC5VSX35T	1.47 –0.16	1.59 –0.16	1.76 –0.16	ns
		XC5VSX50T	1.62 –0.31	1.74 –0.31	1.93 –0.31	ns
		XC5VSX95T	N/A	2.10 –0.44	2.32 –0.44	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 65: **Global Clock Setup and Hold With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
T_{PSDCM}/ T_{PHDCM}	No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode	XC5VLX30	1.53 –0.50	1.70 –0.50	1.88 –0.50	ns
		XC5VLX30T	1.53 –0.50	1.70 –0.50	1.88 –0.50	ns
		XC5VLX50	1.52 –0.48	1.68 –0.48	1.86 –0.48	ns
		XC5VLX50T	1.52 –0.48	1.68 –0.48	1.86 –0.48	ns
		XC5VLX85	1.58 –0.43	1.76 –0.43	1.95 –0.43	ns
		XC5VLX85T	1.57 –0.43	1.76 –0.43	1.95 –0.43	ns
		XC5VLX110	1.58 –0.37	1.76 –0.37	1.95 –0.37	ns
		XC5VLX110T	1.58 –0.37	1.76 –0.37	1.95 –0.37	ns
		XC5VLX220	N/A	2.17 –0.27	2.44 –0.27	ns
		XC5VLX220T	N/A	2.17 –0.27	2.44 –0.27	ns
		XC5VLX330	N/A	2.17 –0.10	2.44 –0.10	ns
		XC5VLX330T	N/A	2.17 –0.10	2.44 –0.10	ns
		XC5VSX35T	1.60 –0.39	1.78 –0.39	1.98 –0.39	ns
		XC5VSX50T	1.58 –0.37	1.76 –0.37	1.95 –0.37	ns
		XC5VSX95T	N/A	2.10 –0.41	2.35 –0.41	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLK0, DCM, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 66: **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
T_{PSDCM0}/ T_{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XC5VLX30	0.27 0.62	0.27 0.62	0.27 0.66	ns
		XC5VLX30T	0.27 0.62	0.27 0.62	0.27 0.66	ns
		XC5VLX50	0.26 0.64	0.26 0.64	0.26 0.68	ns
		XC5VLX50T	0.25 0.64	0.26 0.64	0.26 0.68	ns
		XC5VLX85	0.23 0.76	0.24 0.76	0.24 0.80	ns
		XC5VLX85T	0.23 0.76	0.24 0.76	0.24 0.80	ns
		XC5VLX110	0.23 0.82	0.24 0.82	0.24 0.87	ns
		XC5VLX110T	0.23 0.82	0.24 0.82	0.24 0.87	ns
		XC5VLX220	N/A	0.21 1.31	0.22 1.36	ns
		XC5VLX220T	N/A	0.21 1.31	0.22 1.36	ns
		XC5VLX330	N/A	0.21 1.48	0.22 1.55	ns
		XC5VLX330T	N/A	0.21 1.48	0.22 1.55	ns
		XC5VSX35T	0.25 0.80	0.27 0.80	0.27 0.84	ns
		XC5VSX50T	0.24 0.82	0.25 0.82	0.25 0.86	ns
		XC5VSX95T	N/A	0.24 1.06	0.24 1.11	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLK0, DCM, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 67: **Global Clock Setup and Hold With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XC5VLX30	1.51 –0.81	1.67 –0.81	1.91 –0.81	ns
		XC5VLX30T	1.51 –0.81	1.67 –0.81	1.91 –0.81	ns
		XC5VLX50	1.49 –0.79	1.65 –0.79	1.88 –0.79	ns
		XC5VLX50T	1.49 –0.79	1.65 –0.79	1.88 –0.79	ns
		XC5VLX85	1.52 –0.74	1.70 –0.74	1.95 –0.74	ns
		XC5VLX85T	1.52 –0.74	1.70 –0.74	1.95 –0.74	ns
		XC5VLX110	1.51 –0.68	1.69 –0.68	1.95 –0.68	ns
		XC5VLX110T	1.51 –0.68	1.69 –0.68	1.95 –0.68	ns
		XC5VLX220	N/A	1.77 –0.52	2.08 –0.52	ns
		XC5VLX220T	N/A	1.77 –0.52	2.08 –0.52	ns
		XC5VLX330	N/A	1.75 –0.35	2.07 –0.35	ns
		XC5VLX330T	N/A	1.77 –0.35	2.08 –0.35	ns
		XC5VSX35T	1.56 –0.70	1.73 –0.70	1.98 –0.70	ns
		XC5VSX50T	1.54 –0.68	1.71 –0.68	1.96 –0.68	ns
		XC5VSX95T	N/A	1.83 –0.58	2.11 –0.58	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLKOUT0, PLL, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 68: **Global Clock Setup and Hold With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
T_{PSPLL0}/ T_{PHPLL0}	No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode	XC5VLX30	–0.21 1.15	–0.21 1.23	–0.21 1.33	ns
		XC5VLX30T	–0.21 1.15	–0.21 1.23	–0.21 1.33	ns
		XC5VLX50	–0.22 1.17	–0.22 1.25	–0.22 1.35	ns
		XC5VLX50T	–0.22 1.17	–0.22 1.25	–0.22 1.35	ns
		XC5VLX85	–0.24 1.29	–0.24 1.37	–0.24 1.48	ns
		XC5VLX85T	–0.24 1.29	–0.24 1.37	–0.24 1.48	ns
		XC5VLX110	–0.24 1.35	–0.24 1.43	–0.24 1.54	ns
		XC5VLX110T	–0.24 1.35	–0.24 1.43	–0.24 1.54	ns
		XC5VLX220	N/A	–0.31 1.93	–0.31 2.04	ns
		XC5VLX220T	N/A	–0.32 1.93	–0.32 2.04	ns
		XC5VLX330	N/A	–0.31 2.10	–0.31 2.22	ns
		XC5VLX330T	N/A	–0.32 2.10	–0.32 2.22	ns
		XC5VSX35T	–0.22 1.33	–0.22 1.41	–0.22 1.51	ns
		XC5VSX50T	–0.24 1.35	–0.24 1.43	–0.24 1.53	ns
		XC5VSX95T	N/A	–0.26 1.67	–0.26 1.78	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLKOUT0, PLL, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 69: **Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)						
$T_{PSDCMPLL}$/ $T_{PHDCMPLL}$	No Delay Global Clock and IFF(2) with DCM and PLL in System-Synchronous Mode	XC5VLX30	1.66 –0.37	1.83 –0.37	2.00 –0.37	ns
		XC5VLX30T	1.65 –0.37	1.83 –0.37	2.00 –0.37	ns
		XC5VLX50	1.63 –0.34	1.80 –0.34	1.98 –0.34	ns
		XC5VLX50T	1.63 –0.34	1.80 –0.34	1.98 –0.34	ns
		XC5VLX85	1.68 –0.29	1.87 –0.29	2.07 –0.29	ns
		XC5VLX85T	1.68 –0.29	1.87 –0.29	2.07 –0.29	ns
		XC5VLX110	1.67 –0.23	1.87 –0.23	2.07 –0.23	ns
		XC5VLX110T	1.66 –0.23	1.86 –0.23	2.06 –0.23	ns
		XC5VLX220	N/A	2.26 –0.13	2.55 –0.13	ns
		XC5VLX220T	N/A	2.25 –0.13	2.55 –0.13	ns
		XC5VLX330	N/A	2.23 0.04	2.53 0.04	ns
		XC5VLX330T	N/A	2.25 0.04	2.54 0.04	ns
		XC5VSX35T	1.72 –0.26	1.91 –0.26	2.10 –0.26	ns
		XC5VSX50T	1.70 –0.23	1.88 –0.23	2.07 –0.23	ns
		XC5VSX95T	N/A	2.22 –0.27	2.47 –0.27	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLK0, DCM, CLKOUT0, PLL, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 70: **Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM, PLL, and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in **IOB Switching Characteristics**, page 23.						
$T_{PSDCMPLL\_0}$/ $T_{PHDCMPLL\_0}$	No Delay Global Clock and IFF(2) with DCM and PLL in Source-Synchronous Mode	XC5VLX30	0.39 0.75	0.40 0.75	0.40 0.79	ns
		XC5VLX30T	0.39 0.75	0.40 0.75	0.40 0.79	ns
		XC5VLX50	0.37 0.78	0.38 0.78	0.38 0.81	ns
		XC5VLX50T	0.37 0.78	0.38 0.78	0.38 0.81	ns
		XC5VLX85	0.34 0.90	0.36 0.90	0.36 0.93	ns
		XC5VLX85T	0.33 0.90	0.36 0.90	0.36 0.93	ns
		XC5VLX110	0.32 0.96	0.35 0.96	0.35 1.00	ns
		XC5VLX110T	0.32 0.96	0.35 0.96	0.35 1.00	ns
		XC5VLX220	N/A	0.30 1.45	0.32 1.49	ns
		XC5VLX220T	N/A	0.30 1.45	0.32 1.49	ns
		XC5VLX330	N/A	0.28 1.62	0.31 1.68	ns
		XC5VLX330T	N/A	0.30 1.62	0.32 1.68	ns
		XC5VSX35T	0.38 0.93	0.39 0.93	0.39 0.97	ns
		XC5VSX50T	0.35 0.96	0.37 0.96	0.37 0.99	ns
		XC5VSX95T	N/A	0.35 1.20	0.35 1.24	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CLK0, DCM, CLKOUT0, PLL, and jitter. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

ChipSync™ Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-5 source-synchronous transmitter and receiver data-valid windows.

Table 71: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion (1)	All	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew (2)	XC5VLX30	0.21	0.22	0.22	ns
		XC5VLX30T	0.21	0.22	0.22	ns
		XC5VLX50	0.26	0.27	0.28	ns
		XC5VLX50T	0.26	0.27	0.28	ns
		XC5VLX85	0.42	0.43	0.45	ns
		XC5VLX85T	0.42	0.43	0.45	ns
		XC5VLX110	0.48	0.50	0.51	ns
		XC5VLX110T	0.48	0.50	0.51	ns
		XC5VLX220	N/A	1.07	1.10	ns
		XC5VLX220T	N/A	1.07	1.10	ns
		XC5VLX330	N/A	1.25	1.29	ns
		XC5VLX330T	N/A	1.25	1.29	ns
		XC5VSX35T	0.38	0.39	0.39	ns
		XC5VSX50T	0.43	0.44	0.45	ns
		XC5VSX95T	N/A	0.72	0.74	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.10	0.10	0.10	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.07	0.07	0.08	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.25	0.25	0.25	ns

Notes:
1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 72: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC5VLX30	FF324	80	ps
			FF676	142	ps
		XC5VLX30T	FF665	93	ps
		XC5VLX50	FF324	80	ps
			FF676	142	ps
			FF1153	175	ps
		XC5VLX50T	FF665	93	ps
			FF1136	162	ps
		XC5VLX85	FF676	142	ps
			FF1153	174	ps
		XC5VLX85T	FF1136	164	ps
		XC5VLX110	FF676	142	ps
			FF1153	173	ps
			FF1760	190	ps
		XC5VLX110T	FF1136	163	ps
			FF1738	171	ps
		XC5VLX220	FF1760	178	ps
		XC5VLX220T	FF1738	156	ps
		XC5VLX330	FF1760	177	ps
		XC5VLX330T	FF1738	155	ps
		XC5VSX35T	FF665	103	ps
		XC5VSX50T	FF665	103	ps
			FF1136	157	ps
		XC5VSX95T	FF1136	176	ps

Notes:
1. These values represent the worst-case skew between any two SelectMap I/Os in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 73: **Sample Window**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	450	500	550	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	350	400	450	ps

Notes:
1. This parameter indicates the total sampling error of Virtex-5 DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-5 DDR input registers across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: **ChipSync Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO					
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.56 1.59	–0.54 1.72	–0.54 1.91	ns
Pin-to-Pin Clock-to-Out Using BUFIO					
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	4.42	4.82	5.40	ns

Notice of Disclaimer

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/06	1.0	Initial Xilinx release.
05/12/06	1.1	• First version posted to the Xilinx website. Minor typograpical edits. Revised design software version on page 21. • Revised $T_{IDELAYRESOLUTION}$ in Table 38, page 35. • Revised TDSPCKO in Table 43, page 40.
05/24/06	1.2	• Added register-to-register parameters to Table 26.
08/04/06	1.3	• Added V_{DRINT}, V_{DRI}, and C_{IN} values to Table 3. • Added HSTL_I_12 and LVCMOS12 to Table 7 and renumbered the notes. • Removed pin-to-pin performance (Table 12). Updated and added values to register-register performance Table 26 (was Table 13). • Added values to Table 27. • Updated the speed specification version above Table 28. • Added to Table 30 the I/O standards: HSTL_II_T_DCI, HSTL_II_T_DCI_18, SSTL2_II_T_DCI, and SSTL18_II_T_DCI. • Revised F_{MAX} values in Table 42, and RDWR_B Setup/Hold values in Table 44. • In Table 48, changed F_{VCOMAX}, removed $T_{LOCKMIN}$, and revised $T_{LOCKMAX}$ values, also removed note pointing to Architecture Wizard. • Removed Note 2 on Table 61.
09/06/06	2.0	• Added new sections for LXT devices and added LXT devices to the appropriate tables. The addition of the **RocketIO GTP Transceiver Specifications** required the tables to be renumbered. • Changed maximum V_{IN} values in Table 1 and Table 2. • Updated values and added T_j = 85°C to Table 4, page 3. • Revised the cascade block RAM **Memory**, page 19 section in Table 26 to 64K with new I/O delays. • Revised the setup and hold times in Table 34, page 31. • Added $F_{MAX\_CASCADE}$ to Table 42, page 38. • Revised $F_{FXLFMSMAX}$ and $F_{CLKINLFFXMSMAX}$ in Table 49, page 47.
10/13/06	2.1	• Added System Monitor parameters. Added XC5VLX85T to appropriate tables. • Revised Table 16 including notes. Added Table 17, and Figure 3 and Figure 4. • Added Table 19, page 14: RocketIO CRC block. • Revised design software version and Table 28 on page 21. • Updated **ILOGIC Switching Characteristics**, page 31 • Updated F_{MAX_ECC} in Table 42, page 38. • Changed hold times for T_{SMDCCK}/ T_{SMCCKD} and T_{BPIDCC}/T_{BPICCD} in Table 44, page 43. • Revised $T_{FBDELAY}$, F_{OUTMIN}, F_{OUTMAX}, and $F_{INJITTER}$ Table 48, page 46. • Revised Table 49, page 47.

Date	Version	Revision
01/05/07	2.2	• Added I_{IN} to Table 2. Added XC5VLX220T to appropriate tables. • Added LVDCI33, LVDCI25, LVDCI18, LVDCI15 to Table 7. • Update the symbols in the GTP Transceiver Table 12, Table 13, and Table 14. • Add values for -1 speed grade in Table 18, page 14. • Added SFI-4.1 values to Table 27, page 20. • Removed -3 speed grade from available LX220 device list in Table 28, page 21. • Added maximum frequency to Table 46 and Table 47, page 45. • In Table 49, page 47 changed the all the CLKDV, CLKFX, and CLKFX180 Min values and the CLKIN Min values in the Input Clocks (High Frequency Mode) section. • Added values to Table 52 and Table 53, page 50.
02/02/07	3.0	• Added XC5VSX35T, XC5VSX50T, and SX5VSX95T devices to appropriate tables. • Revised the I_{RPU} values in Table 3, page 2. • Revised the I_{CCAUXQ} values in Table 4, page 3. • Added values to Table 5, page 4. • Minor added notes and changed descriptions in Table 13, page 9 and Table 14, page 9. • Revised the SFI-4.1 (SDR LVDS Interface) -1 values in Table 27, page 20. • Revised gain error, bipolar gain error, and event conversion time in Table 25, page 17 • Changed the design software version that matches this datasheet above Table 28 on page 21. • In **Switching Characteristics**, the following values are revised: - LVCMOS25, Fast, 12 mA in Table 30, page 23. - Setup and Hold and T_{ICKQ} in Table 34, page 31. - T_{OCKQ} in Table 35, page 32. - Sequential delay values in Table 37, page 34. - T_{CXB}, T_{CEO}, and T_{DICK} in Table 39, page 35. - T_{RCKO_DO}, $T_{RCKO\_POINTERS}$, T_{RCKO_ECCR}, T_{RCKO_ECC}, T_{RCCK_ADDR}, T_{RDCK_DI}, $T_{RDCK\_DI\_ECC}$, T_{RCCK_WREN}, and T_{RCO_FLAGS} in Table 42, page 38. - T_{DSPDCK_CC}, $T_{DSPCCK\_\{RSTAA, RSTBB\}}$, $T_{DSPCKO\_\{PP, CRYOUTP\}}$, $F_{MAX\_MULT\_NOMREG}$ and $F_{MAX\_MULT\_NOMREG\_PATDET}$ in Table 43, page 40. - T_{BCCKO_O}, and T_{BGCKO_O} in Table 45, page 45. - $T_{BUFIOCKO\_O}$ and F_{MAX} in Table 46, page 45. - T_{BRCKO_O} and $T_{BRCKO\_O\_BYP}$ in Table 47, page 45. - Parameters in Table 48, page 46 including notes. • In **Virtex-5 Pin-to-Pin Output Parameter Guidelines**: - Revised values in Table 57, Table 58, and Table 59. • In **Virtex-5 Pin-to-Pin Input Parameter Guidelines**: - Clarified description in Table 64, page 59. - Revised values in Table 64, Table 65, and Table 66. - Removed duplicate $T_{BUFR\_MAX\_FREQ}$ and $T_{BUFIO\_MAX\_FREQ}$ from Table 71. • Revised values in Table 74, page 68.

Date	Version	Revision
05/18/07	3.1	• Added typical values for n and r in Table 3. • Revised and added values to Table 4. • Revised standard I/O levels in Table 7. • Additions and updates to Table 14, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, and Table 23. • Added **Ethernet MAC Switching Characteristics**, page 16. • Changed the design software version that matches this datasheet above Table 28 on page 21. • Added new section: **I/O Standard Adjustment Measurement Methodology**, page 28. • In **Switching Characteristics**, the following values are revised: - LVTTL, Slow and Fast, 2 mA, 4 mA, and 6 mA (Table 30). - LVCMOS33, Slow and Fast, 2 mA, 4 mA, and 6 mA (Table 30). - LVCMOS25, Slow and Fast, 2 mA and 4 mA, and Fast 12 mA (Table 30). - LVCMOS18, Slow and Fast, 2 mA, 4 mA, and 6 mA (Table 30). - LVCMOS15 and LVCMOS12, Slow and Fast, 2 mA (Table 30). - T_{IDOCK} and T_{IDOCKD} in Table 34. - Setup/Hold for Control Lines and Data Lines in Table 36. - Add $T_{IDELAYPAT\_JIT}$ and revised $T_{IDELAYRESOLUTION}$ in Table 38, page 35 and added Notes 1 and 2. - Revised T_{RCK} page 36 and removed T_{CKSR} Table 39, page 35. - Replaced T_{TWC} with T_{MCP} symbol in Table 40, page 37. - Revised T_{CECK} in Table 41. - Revised T_{RCKO_FLAGS} and $T_{RDCK\_DI\_ECC}$ encode only in Table 42. - Revised Hold Times of Data/Control Pins to the Input Register Clock. Setup/Hold times of {PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK. Hold times of some of the CE pins. Hold times of some of the RST pins. Hold times of {A, B} input to {P, CARRYOUT} output using multiplier and {ACIN, BCIN} input to {P, CARRYOUT} output using multiplier, CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier, in Table 43. - Updated and added values to Table 44, page 43. • Revised -1 speed F_{MAX} value in Table 46, page 45. • Added Note 4 to $T_{LOCKMAX}$ and revised F_{INDUTY}, F_{INMAX},and F_{VCOMAX} in Table 48, page 46. • Added ± values to Table 52 and Table 53. Changed T_{OUT_OFFSET} in Table 53. • In **Virtex-5 Pin-to-Pin Output Parameter Guidelines**: - Revised values in Table 57 through Table 63. • In **Virtex-5 Pin-to-Pin Input Parameter Guidelines**: - Revised values in Table 64 through Table 70. • In **ChipSync™ Source-Synchronous Switching Characteristics**: - Revised values in Table 71, page 66. - Added package skew values to Table 72, page 67. - Revised values in Table 74, page 68.

Date	Version	Revision
06/15/07	3.2	• Updated T_{STG} in Table 1. • Corrected V_{OH}/V_{OL} in Table 9 and Table 10, page 7. • Changed the design software version that matches this data sheet above Table 28 on page 21. • Added "Production Silicon and ISE Software Status," page 22. • Added $T_{IODELAY\_CLK\_MAX}$ and revised T_{CKSR} in Table 38, page 35. • In **Virtex-5 Pin-to-Pin Output Parameter Guidelines**: Revised values in Table 58 through Table 63. • In **Virtex-5 Pin-to-Pin Input Parameter Guidelines**: Revised values in Table 65 through Table 70. • Corrected units to ns in Table 71, page 66.
06/26/07	3.3	• Added conditions to DV_{PPIN} in Table 16, page 12. • Changed the F_{GTXMAX} symbol name to F_{GTPMAX}. • Updated GTP maximum line rates to 3.75 Gb/s in Table 18, page 14. • Updated maximum frequencies in Table 21, page 15. • Added 3.75 Gb/s condition and changed maximum value of F_{GTX} in Table 22, page 15. • Added 3.75 Gb/s sinusoidal jitter specification and changed maximum value of F_{GRX} in Table 23, page 16. • Changed analog input common mode ranges in Table 25, page 17. • Changed $T_{PKGSKEW}$ values in Table 72, page 67.
07/26/07	3.4	• Added maximum value of I_{REF} to Table 3, page 2. • Revised Table 28 and changed the design software version in Table 29 for production devices. • In Table 38, page 35, added High Performance Mode to Note 2. • In Table 44, page 43, revised description of T_{SMDCCK}/T_{SMCCKD}. • Added Note 4 to $T_{DUTYCYCRANGE\_200\_400}$ frequency range in Table 51, page 49. • In **Virtex-5 Pin-to-Pin Input Parameter Guidelines**: Revised note 1 in Table 64 through Table 69.
09/27/07	3.5	• Added I_{BATT} value and Note 2 to Table 3. • Added **DRP Clock Frequency** and Note 4 to Table 25. Revised the typical and maximum values and units for gain error and bipolar gain error. • Removed unsupported XC5VSX95T -3 speed grade from Table 28 and Table 29. • Removed unsupported I/O standards (LVDS_33, LVDSEXT_33, and ULVDS_25) from Table 25. Also updated LVDSEXT, 2.5V in Table 33. • Added values to **Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK** in Table 44. • In **Virtex-5 Pin-to-Pin Input Parameter Guidelines**: Revised note 1 in Table 64 through Table 70.
11/05/07	3.6	• Removed note 1 from Table 26, page 19. F_{MAX} of clock is not an applicable limitation. • Revised DDR2 memory interface performance in Table 27, page 20. • Revised Table 29 to add ISE 9.2i SP3 where applicable. • Removed XC5VSX95T -3 speed grade support from applicable tables. • Removed unsupported I/O standard (LVPECL_33) from Table 32 and added LVPECL_25. • Added T_{SMCO} and T_{SMCKBY} to Table 44, page 43. • Revised note 3 in Table 49, page 47 and Table 50, page 48. • Clarified notes in Table 60 to Table 63, and Table 67 to Table 70. • Revised note 1 in Table 72.