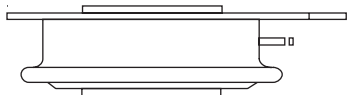


Inverter Grade Thyristors (Hockey PUK Version), 390 A



TO-200AB (A-PUK)

FEATURES

- Metal case with ceramic insulator
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- International standard case TO-200AB (A-PUK)
- Guaranteed high dI/dt
- High surge current capability
- Low thermal impedance
- High speed performance
- Lead (Pb)-free



RoHS
COMPLIANT

PRODUCT SUMMERY

$I_{T(AV)}$	390 A
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TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

MAJOR RATINGS AND CHARACTERISTICS

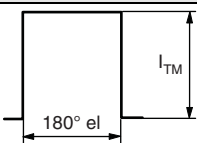
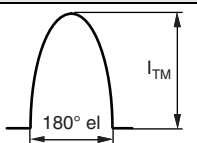
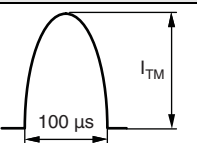
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		390	A
	T_{hs}	55	°C
$I_{T(RMS)}$		745	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	5850	A
	60 Hz	6130	
I^2t	50 Hz	171	kA ² s
	60 Hz	156	
V_{DRM}/V_{RRM}		400 to 800	V
t_q	Range	10 to 30	μs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST223C..C	04	400	500	40
	08	800	900	

CURRENT CARRYING CAPABILITY

FREQUENCY							UNITS
50 Hz	930	800	1430	1220	5870	5240	A
400 Hz	910	770	1490	1300	3120	2740	
1000 Hz	780	650	1430	1260	1880	1640	
2500 Hz	490	400	1070	920	1000	860	
Recovery voltage V_r	50		50		50		V
Voltage before turn-on V_d	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50		-		-		A/ μ s
Heatsink temperature	40	55	40	55	40	55	$^{\circ}$ C
Equivalent values for RC circuit	47/0.22		47/0.22		47/0.22		Ω/μ F

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum average on-state current at heatsink temperature	I _{T(AV)}	180° conduction, half sine wave Double side (single side) cooled			390 (150)	A	
					55 (85)	°C	
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C heatsink temperature double side cooled			745	A	
Maximum peak, one half cycle, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	5850		
		t = 8.3 ms			6130		
		t = 10 ms	100 % V _{RRM} reapplied		4920		
		t = 8.3 ms			5150		
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		171	kA ² s	
		t = 8.3 ms			156		
		t = 10 ms	100 % V _{RRM} reapplied		121		
		t = 8.3 ms			110		
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			1710	kA ² √s	
Maximum peak on-state voltage	V _{TM}	I _{TM} = 600 A, T _J = T _J maximum, t _p = 10 ms sine wave pulse			1.58	V	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.05		
High level value of threshold voltage	V _{T(TO)2}	I > π × I _{T(AV)} , T _J = T _J maximum			1.09		
Low level value of forward slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.88	mΩ	
High level value of forward slope resistance	r _{t2}	I > π × I _{T(AV)} , T _J = T _J maximum			0.82		
Maximum holding current	I _H	T _J = 25 °C, I _T > 30 A			600	mA	
Typical latching current	I _L	T _J = 25 °C, V _A = 12 V, R _a = 6 Ω, I _G = 1 A			1000		

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS
			MIN.	MAX.	
Maximum non-repetitive rate of rise of turned on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$, $I_{TM} = 2 \times di/dt$	1000		A/ μ s
Typical delay time	t_d	$T_J = 25$ $^{\circ}$ C, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μ s Resistive load, gate pulse: 10 V, 5 Ω source	0.78		μ s
Maximum turn-off time	t_q	$T_J = T_J$ maximum, $I_{TM} = 300$ A, commutating $di/dt = 20$ A/ μ s $V_R = 50$ V, $t_p = 500$ μ s, dV/dt : See table in device code	10	30	

**BLOCKING**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	40	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	+ V_{GM}		20	V
Maximum peak negative gate voltage	- V_{GM}		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.17	K/W
		DC operation double side cooled	0.08	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.033	
		DC operation double side cooled	0.017	
Mounting force, ± 10 %			4900 (500)	N (kg)
Approximate weight			50	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (A-PUK)	

 ΔR_{thJ-hs} CONDUCTION

CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.015	0.017	0.011	0.011	$T_J = T_J$ maximum	K/W
120°	0.019	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.037		
30°	0.060	0.060	0.060	0.061		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

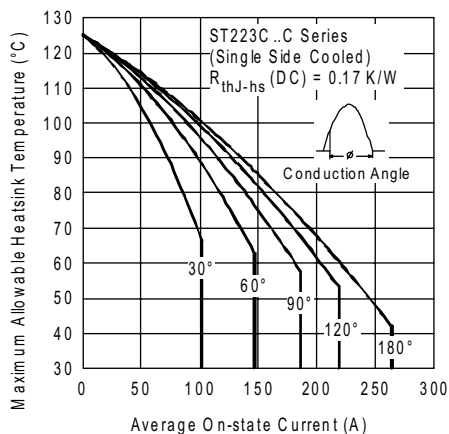


Fig. 1 - Current Ratings Characteristics

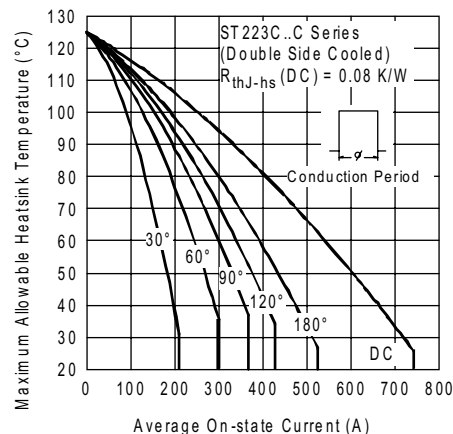


Fig. 4 - Current Ratings Characteristics

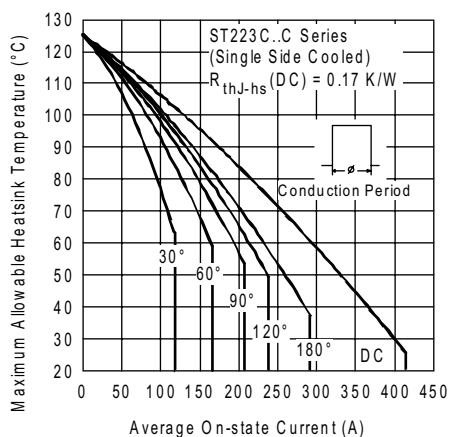


Fig. 2 - Current Ratings Characteristics

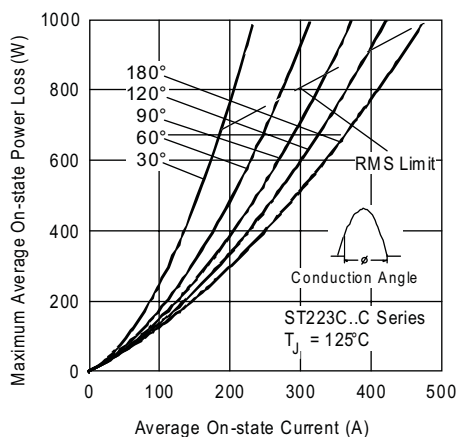


Fig. 5 - On-State Power Loss Characteristics

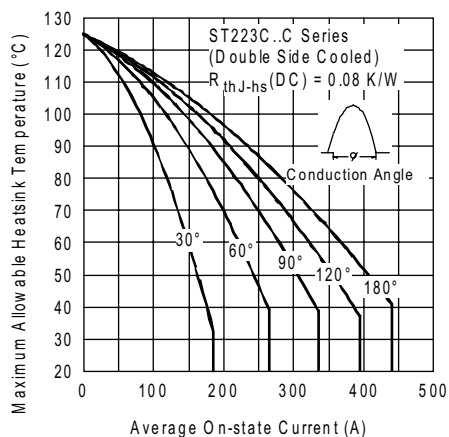


Fig. 3 - Current Ratings Characteristics

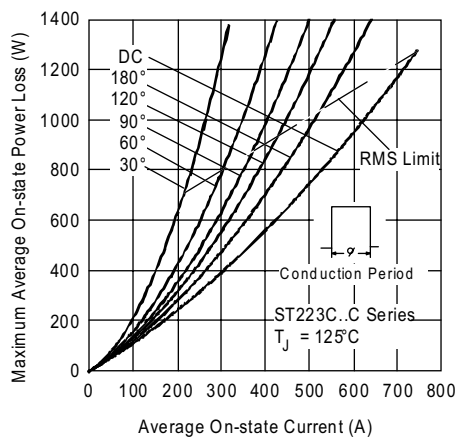


Fig. 6 - On-State Power Loss Characteristics

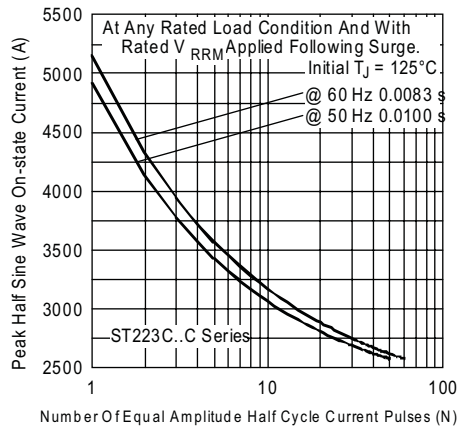


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

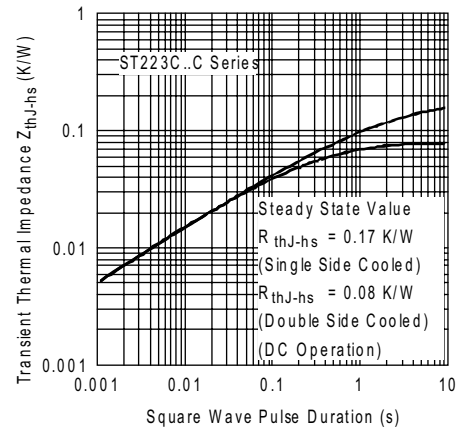


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

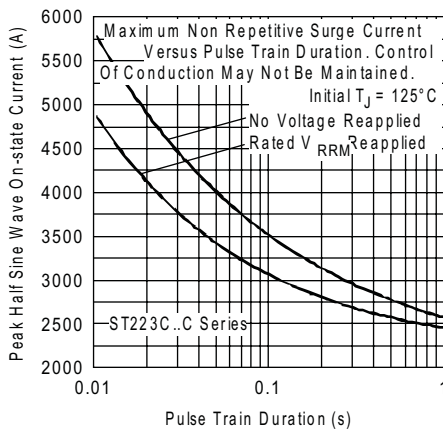


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

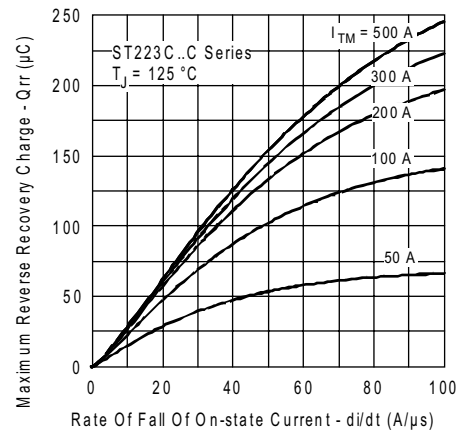


Fig. 11 - Reverse Recovered Charge Characteristics

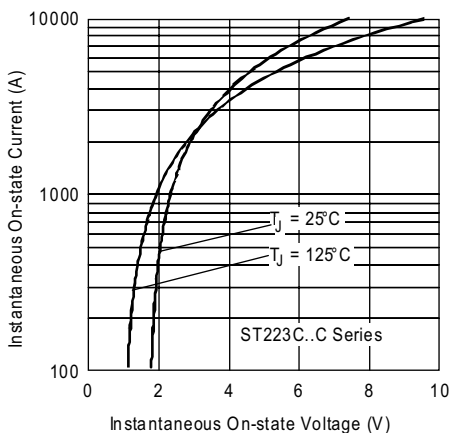


Fig. 9 - On-State Voltage Drop Characteristics

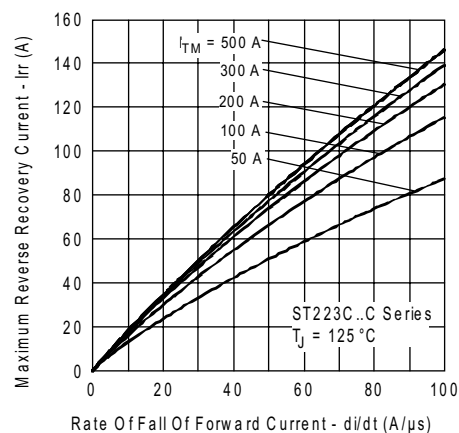


Fig. 12 - Reverse Recovered Current Characteristics

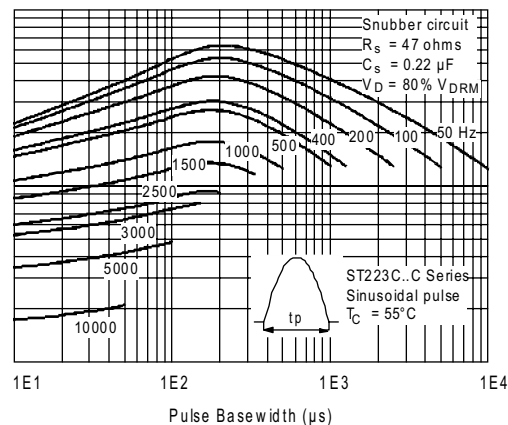
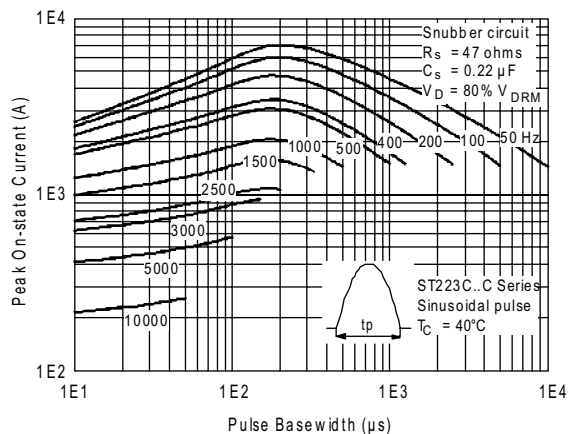


Fig. 13 - Frequency Characteristics

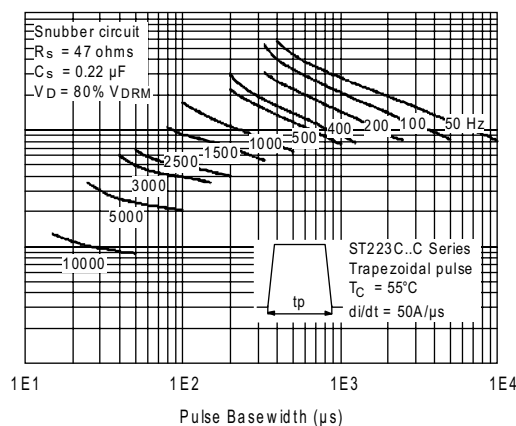
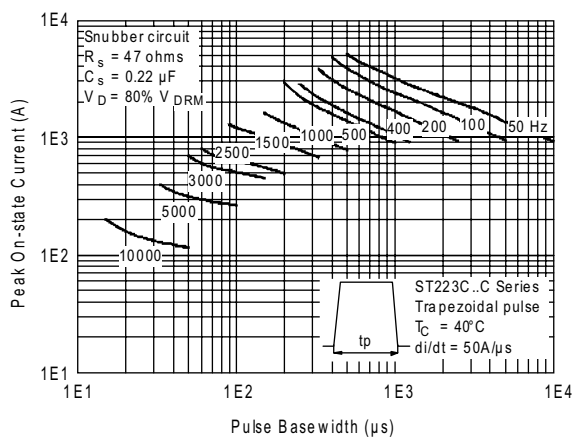


Fig. 14 - Frequency Characteristics

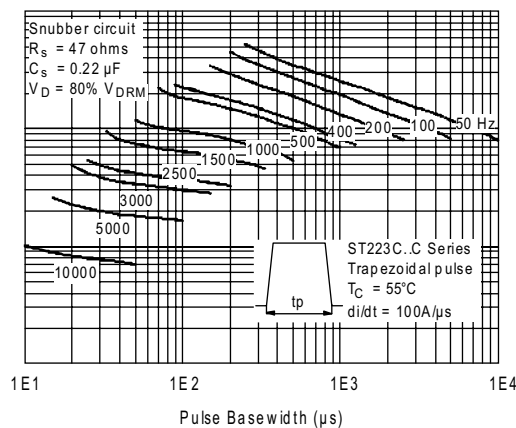
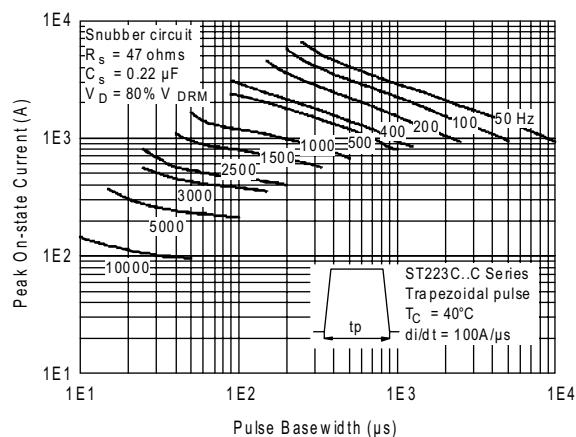


Fig. 15 - Frequency Characteristics

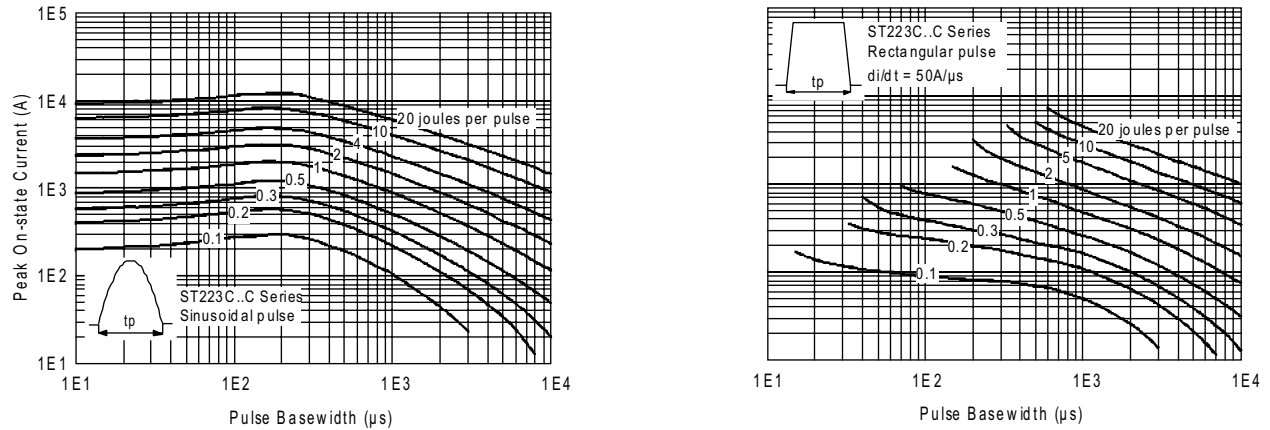


Fig. 16 - Maximum On-State Energy Power Loss Characteristics

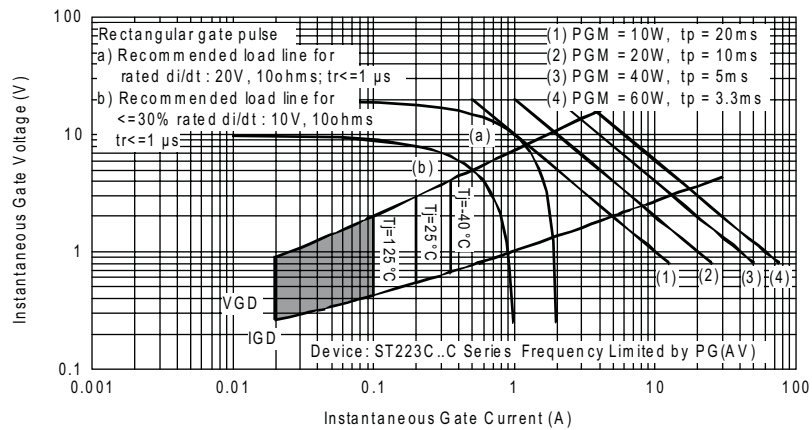


Fig. 17 - Gate Characteristics

ST223C..C Series

Vishay High Power Products Inverter Grade Thyristors
(Hockey PUK Version), 390 A



ORDERING INFORMATION TABLE

Device code	ST	22	3	C	08	C	H	K	1	-
	1	2	3	4	5	6	7	8	9	10

- 1** - Thyristor
- 2** - Essential part number
- 3** - 3 = Fast turn off
- 4** - C = Ceramic PUK
- 5** - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- 6** - C = PUK case TO-200AB (A-PUK)
- 7** - Reapplied dV/dt code (for t_q test condition)
- 8** - t_q code
- 9** - 0 = Eyelet term.
(gate and aux. cathode unsoldered leads)
1 = Fast-on term.
(gate and aux. cathode unsoldered leads)
2 = Eyelet term.
(gate and aux. cathode soldered leads)
3 = Fast-on term.
(gate and aux. cathode soldered leads)
- 10** - Critical dV/dt:
 - None = 500 V/ μ s (standard value)
 - L = 1000 V/ μ s (special selection)

dV/dt - t_q combinations available					
dV/dt (V/ μ s)	20	50	100	200	400
10	CN	DN	EN	FN*	--
12	CM	DM	EM	FM	--
15	CL	DL	EL	FL*	HL
18	CP	DP	EP	FP	HP
20	CK	DK	EK	FK	HK
25	--	--	--	--	HJ
30	--	--	--	--	HH

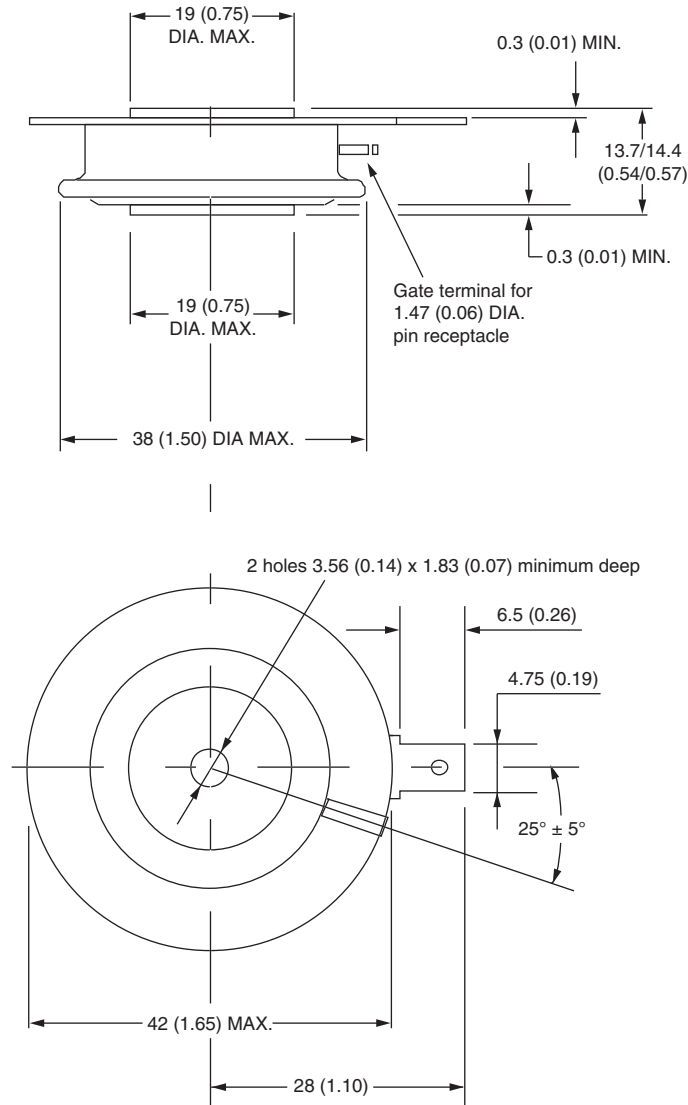
* Standard part number.
All other types available only on request.

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95074

TO-200AB (A-PUK)

DIMENSIONS in millimeters (inches)

Anode to gate
Creepage distance: 7.62 (0.30) minimum
Strike distance: 7.12 (0.28) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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