# S71NS-P Memory Subsystem Solutions

## MirrorBit® 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode Multiplexed pSRAM

**512 Mb / 256 Mb / 128 Mb (32M / 16M / 8M x 16-bit) Flash**
**128 Mb / 64 Mb / 32 Mb (8M / 4M / 2M x 16-bit) pSRAM**

***Data Sheet*** *(Preliminary)*

**Notice to Readers:** This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

**Publication Number** S71NS-P_00 **Revision** 09 **Issue Date** July 8, 2010

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## Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

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When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or $V_{IO}$ range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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# S71NS-P Memory Subsystem Solutions

## MirrorBit® 1.8 Volt-only Simultaneous Read/Write, Burst Mode Multiplexed Flash Memory and Burst Mode Multiplexed pSRAM

### 512 Mb / 256 Mb / 128 Mb (32M / 16M / 8M x 16-bit) Flash
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***Data Sheet*** *(Preliminary)*

## Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speed (Flash and pSRAM): 66 MHz, 83 MHz**
- **MCP BGA Package**
  – 56 ball, 9.2 x 8.0 mm, 0.5 mm ball pitch
- **Operating Temperature**
  – Wireless, –25°C to +85°C

## General Description

The S71NS-P Series is a product line of stacked Multi-Chip Package (MCP) memory solutions and consists of the following items:

- One or more S29NS-P flash memory die
- Multiplexed pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual data sheet for further details.

| | pSRAM | | | |
|---|---|---|---|---|
| | **Density** | **32 Mb** | **64 Mb** | **128 Mb** |
| Flash | 128 Mb | S71NS128PB0 | S71NS128PC0 | - |
| | 256 Mb | S71NS256PB0 | S71NS256PC0 | - |
| | 512 Mb | - | - | S71NS512PD0 |

For detailed specifications, please refer to the individual data sheets:

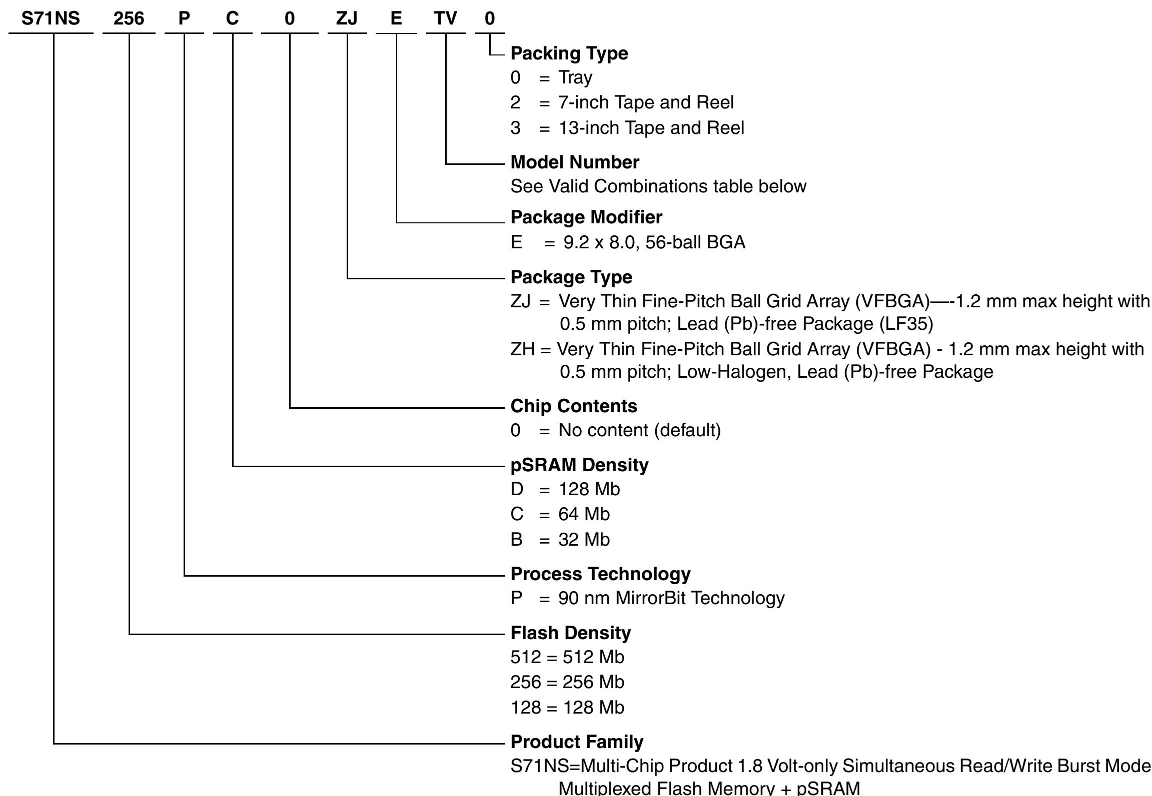
| Document | Publication Identification Number |
|---|---|
| S29NS-P | S29NS-P_00 |
| 32M Multiplexed pSRAM Type 3 | muxpsram_10 |
| 64M Multiplexed pSRAM Type 3 | muxpsram_01 |
| 128 Mb CellularRAM AD-MUX | SWM128D108M1R |

**Publication Number** S71NS-P_00 **Revision** 09 **Issue Date** July 8, 2010

This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications.

# 1. Ordering Information

The order number is formed by a valid combinations of the following:




## 1.1 Valid Combinations

| Valid Combinations | | | | | | |
|---|---|---|---|---|---|---|
| **Product Family** | **Code Flash Density (Mb)** | **Process Technology** | **pSRAM Density (Mb)** | **Package Type/ Material** | **Model Number** | **Packing Type** |
| S71NS | 128 | P | B0, C0 | ZJE, ZHE | TV, JR, TW, TS (Note 4) | 0, 2, 3 (Note 1) |
| | 256 | | | | | |
| | 512 | | D0 | ZHE | UR | |

***Notes:***

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*
3. *Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to availability of specific valid combinations and to check on newly released combinations.*
4. *Model Numbers TW and TS indicate products intended for use with MediaTek chipsets. Model numbers TV and JR are not intended for use with MediaTek chipsets.*

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## 1.2 Product Selector Guide

<table>
<tr><th>Device OPN</th><th>Flash Density</th><th>pSRAM Density</th><th>MCP Speed (MHz)</th><th>pSRAM Supplier</th><th>Package</th></tr>
<tr><td>S71NS128PB0ZJETV</td><td rowspan="9">128 Mb</td><td rowspan="4">32 Mb</td><td rowspan="2">66</td><td rowspan="18">Type 3</td><td rowspan="19">9.2 x 8.0 mm,<br>56-ball MCP</td></tr>
<tr><td>S71NS128PB0ZJETW</td></tr>
<tr><td>S71NS128PB0ZJEJR</td><td rowspan="2">83</td></tr>
<tr><td>S71NS128PB0ZJETS</td></tr>
<tr><td>S71NS128PC0ZHETV</td><td rowspan="5">64 Mb</td><td rowspan="3">66</td></tr>
<tr><td>S71NS128PC0ZJETV</td></tr>
<tr><td>S71NS128PC0ZHETW</td></tr>
<tr><td>S71NS128PC0ZJEJR</td><td rowspan="2">83</td></tr>
<tr><td>S71NS128PC0ZHETS</td></tr>
<tr><td>S71NS256PB0ZJETV</td><td rowspan="9">256 Mb</td><td rowspan="4">32 Mb</td><td rowspan="2">66</td></tr>
<tr><td>S71NS256PB0ZJETW</td></tr>
<tr><td>S71NS256PB0ZJEJR</td><td rowspan="2">83</td></tr>
<tr><td>S71NS256PB0ZJETS</td></tr>
<tr><td>S71NS256PC0ZHETV</td><td rowspan="5">64 Mb</td><td rowspan="3">66</td></tr>
<tr><td>S71NS256PC0ZHETW</td></tr>
<tr><td>S71NS256PC0ZJETV</td></tr>
<tr><td>S71NS256PC0ZJEJR</td><td rowspan="2">83</td></tr>
<tr><td>S71NS256PC0ZHETS</td></tr>
<tr><td>S71NS512PD0ZHEUR</td><td>512 Mb</td><td>128 Mb</td><td>83</td><td>SWM128D108M1R</td></tr>
</table>

# 2. Input/Output Descriptions

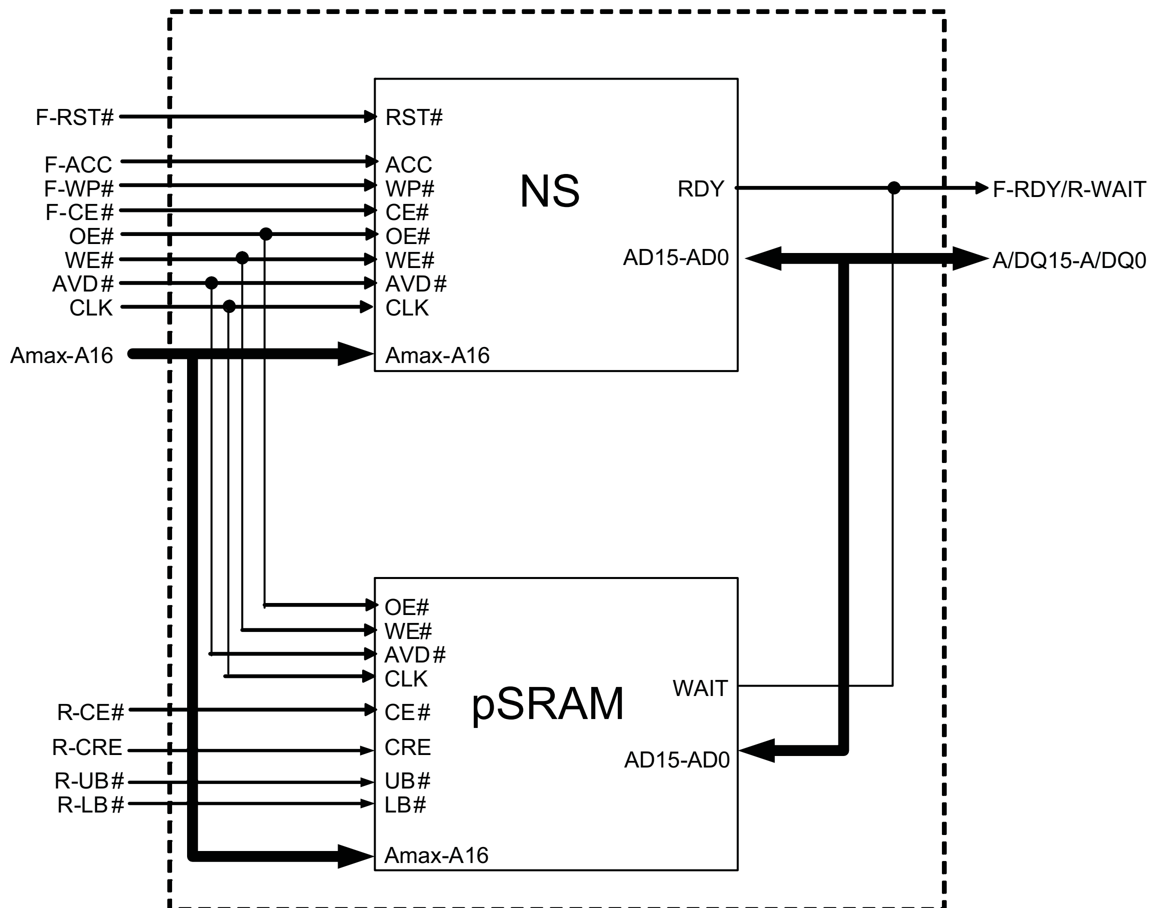
Table 2.1 identifies the input and output package connections provided on the device.

**Table 2.1** Input/Output Descriptions

| Symbol | Description | Flash | RAM |
|---|---|---|---|
| AMAX – A16 | Address inputs | X | X |
| A/DQ15-A/DQ0 | Multiplexed Address/Data | X | X |
| OE# | Output Enable input. Asynchronous relative to CLK for the Burst mode. | X | X |
| WE# | Write Enable input. | X | X |
| $V_{SS}$ | Ground | X | X |
| NC | Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). | X | X |
| F-RDY/R-WAIT | Ready output; indicates the status of the Burst read.<br>Flash Memory RDY (using default “Active HIGH” configuration)<br>$V_{OL}$ = data invalid<br>$V_{OH}$ = data valid<br>Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal.<br>pSRAM WAIT (using default “Active HIGH” configuration)<br>$V_{OL}$ = data valid<br>$V_{OH}$ = data invalid<br>To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY) | X | X |
| CLK | Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at $V_{IL}$ or $V_{IH}$ while in asynchronous mode | X | X |
| AVD# | Address Valid input. Indicates to device that the valid address is present on the address inputs.<br>Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.<br>High = device ignores address inputs | X | X |
| F-RST# | Hardware reset input. Low = device resets and returns to reading array data | X | |
| F-WP# | Hardware write protect input. At $V_{IL}$, disables program and erase functions in the four outermost sectors. Should be at $V_{IH}$ for all other conditions. | X | |
| F-ACC/F-VPP | Accelerated input. At $V_{HH}$, accelerates programming; automatically places device in unlock bypass mode. At $V_{IL}$, disables all program and erase functions. Should be at $V_{IH}$ for all other conditions. | X | |
| R-CE# | Chip-enable input for pSRAM. | | X |
| F-CE# | Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode. | X | |
| R-CRE | Control Register Enable (pSRAM). | | X |
| F-VCC | Flash 1.8 Volt-only single power supply. | X | |
| R-VCC | pSRAM Power Supply. | | X |
| R-UB# | Upper Byte Control (pSRAM). | | X |
| R-LB# | Lower Byte Control (pSRAM) | | X |
| DNU | Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at $V_{IL}$. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to $V_{SS}$. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections. | | |
| RFU | Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices. | | |

# 3. MCP Block Diagram

**Figure 3.1** MCP Block Diagram for S71NS128P and S71NS256P



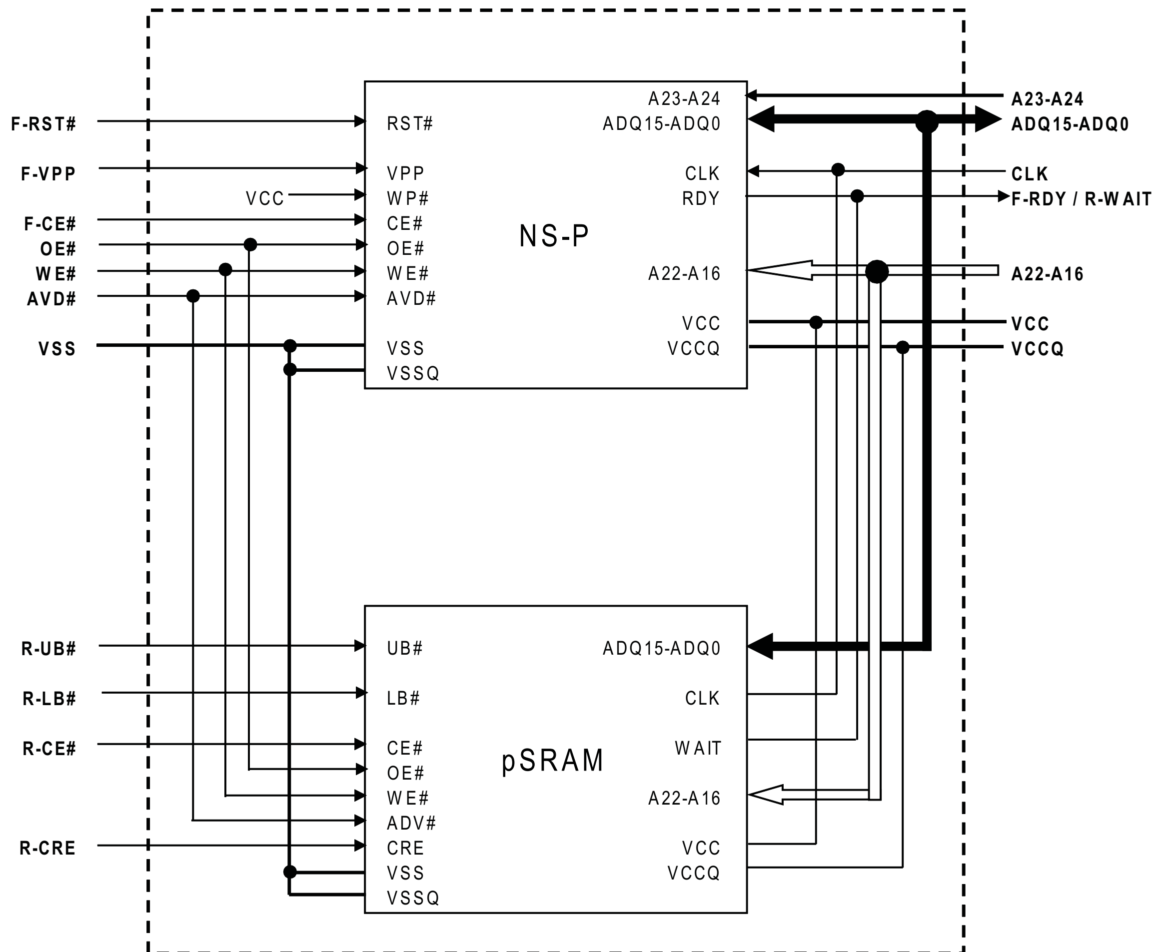



**Figure 3.2** MCP Block Diagram for S71NS512P

# 4. Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71NS-P.

## 4.1 Special Handling Instructions for FBGA Packages

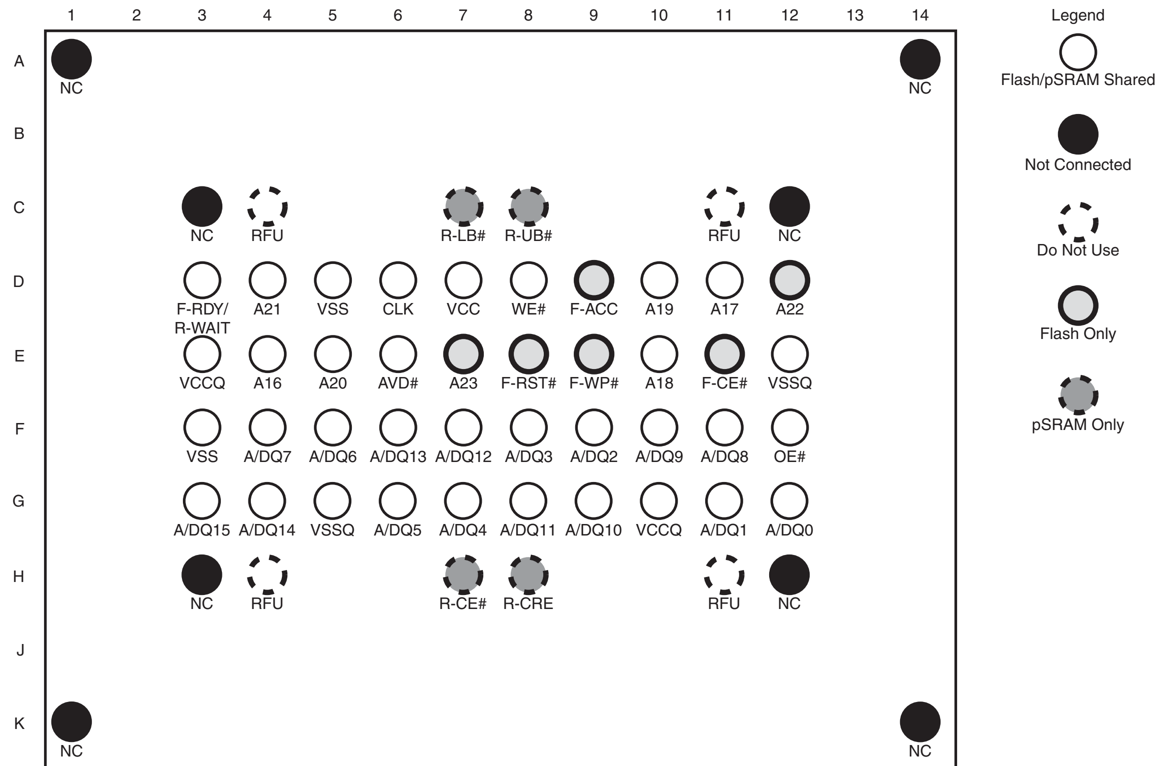
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

## 4.2 Connection Diagrams

**Figure 4.1** 56-ball Fine-Pitch Ball Grid Array (S71NS128P and S71NS256P)

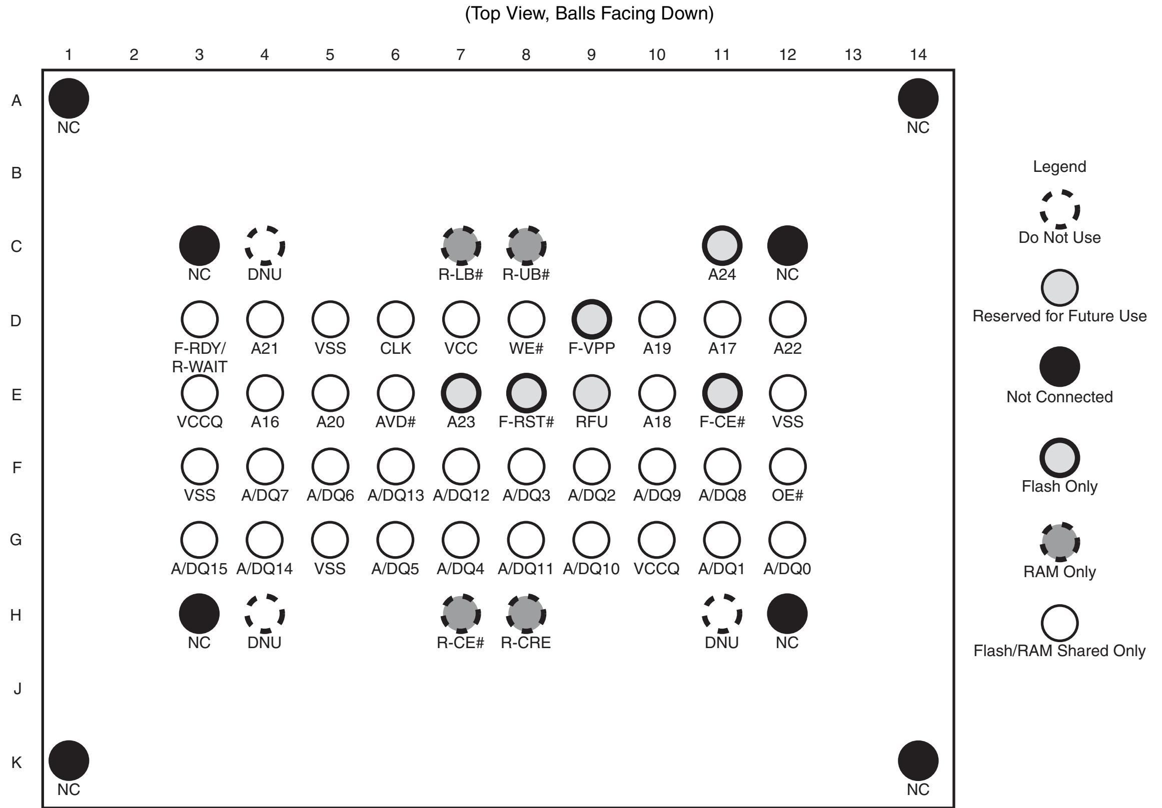
(Top View, Balls Facing Down)




***Note:***
*Addresses are shared between Flash and RAM depending on the density of the pSRAM.*

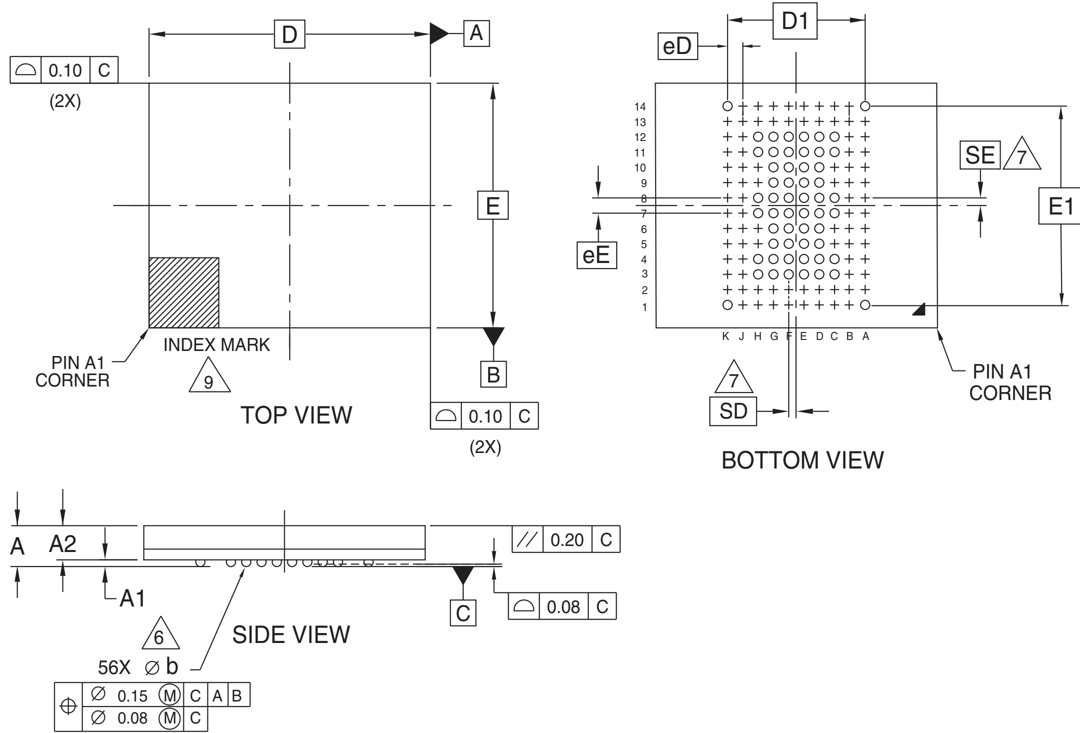
| MCP | Flash-Only Addresses | Shared Addresses | Shared ADQ Pins |
|---|---|---|---|
| S71NS128PB0 | A22-A21 | A20-A16 | A/DQ15-A/DQ0 |
| S71NS128PC0 | A22 | A21-A16 | |
| S71NS256PB0 | A23-A21 | A20-A16 | |
| S71NS256PC0 | A23-A22 | A21-A16 | |

**Figure 4.2** 56-ball Fine-Pitch Ball Grid Array for S71NS512P



## 4.3 Physical Dimensions

**Figure 4.3** NLB056—56-ball VFBGA 9.2 x 8.0 mm




| PACKAGE | NLB 056 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D x E | 9.20 mm x 8.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.20 | PROFILE |
| A1 | 0.20 | --- | --- | BALL HEIGHT |
| A2 | 0.85 | --- | 0.97 | BODY THICKNESS |
| D | | 9.20 BSC. | | BODY SIZE |
| E | | 8.00 BSC. | | BODY SIZE |
| D1 | | 4.50 BSC. | | MATRIX FOOTPRINT |
| E1 | | 6.50 BSC. | | MATRIX FOOTPRINT |
| MD | | 10 | | MATRIX SIZE D DIRECTION |
| ME | | 14 | | MATRIX SIZE E DIRECTION |
| n | | 56 | | BALL COUNT |
| Øb | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | | 0.50 BSC. | | BALL PITCH |
| eD | | 0.50 BSC | | BALL PITCH |
| SD / SE | | 0.25 BSC. | | SOLDER BALL PLACEMENT |
| | | A2 ~ A13,B1 ~ B14<br>C1,C2,C5,C6,C9,C10,C13,C14<br>D1,D2,D13,D14,E1,E2,E13,E14,F1,F2,F13,F14<br>G1,G2,G13,G14,H1,H2,H5,H6,H9,H10,H13,H14<br>J1 ~ J14, K2 ~ K13 | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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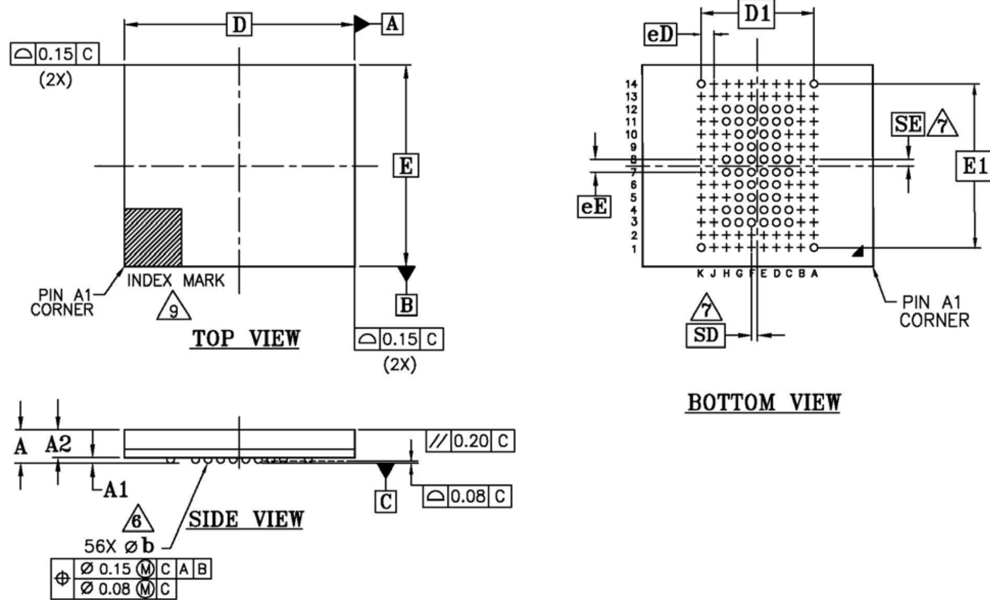
**Figure 4.4** NSB056—56-ball VFBGA 9.2 x 8.0 mm




| PACKAGE | NSB 056 | | | NOTE |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D X E | 9.20 mm x 8.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | |
| A | --- | --- | 1.20 | PROFILE |
| A1 | 0.20 | --- | --- | BALL HEIGHT |
| A2 | 0.85 | --- | 0.97 | BODY THICKNESS |
| D | 9.20 BSC. | | | BODY SIZE |
| E | 8.00 BSC. | | | BODY SIZE |
| D1 | 4.50 BSC. | | | MATRIX FOOTPRINT |
| E1 | 6.50 BSC | | | MATRIX FOOTPRINT |
| MD | 10 | | | MATRIX SIZE D DIRECTION |
| ME | 14 | | | MATRIX SIZE E DIRECTION |
| n | 56 | | | BALL COUNT |
| Ø b | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | 0.50 BSC. | | | BALL PITCH |
| eD | 0.50 BSC. | | | BALL PITCH |
| SE SD | 0.25 BSC. | | | SOLDER BALL PLACEMENT |
| | A2- A13,B1-B14,C1, C2,C5,C6,C9,C10,C13, C14, D1,D2,D13,D14,E1,E2, E13,E14,F1,F2,F13,F14,G1 ,G2,G13,G14,H1,H2, H5,H6,H9,H10,H13,H14, J1-J14, K2-K13 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

NSB056 \ 16.038.22 \ 9.25.7

# 5. Revision History

| Section | Description |
| --- | --- |
| **Revision 01 (October 12, 2006)** | |
| | Initial release |
| **Revision 02 (December 8, 2006)** | |
| Global | Added S71NS128PC0 |
| **Revision 03 (September 10, 2007)** | |
| Global | Added product details including ordering information for S71NS256PB0 |
| **Revision 04 (September 26, 2007)** | |
| Physical Dimension | Added mechanical drawing for the NSB056 package |
| **Revision 05 (December 13, 2007)** | |
| Global | Added product information for 83 MHz MCPs, including ordering part numbers and valid combinations |
| **Revision 06 (May 2, 2008)** | |
| General Description | Changed 32 M Multiplexed pSRAM Type 3 Publication Identification Number to muxpsram_10 |
| Ordering Information | Added Low-Halogen package option<br>Removed height and ball pitch information from Package Modifier description<br>Removed Character Position Descriptions table<br>Updated Valid Combinations table<br>Added Product Selector Guide table |
| **Revision 07 (March 30, 2010)** | |
| Ordering Information | Added model numbers TW and TS to indicate products intended for MediaTek chipsets. |
| **Revision 08 (May 27, 2010)** | |
| Product Selector Guide | Corrected package type combinations for 128+32 and 256+32 TW and TS model OPNs. |
| **Revision 09 (July 8, 2010)** | |
| Global | Added S71NS512PD0ZHEUR and its block and pinout diagrams.<br>Removed 112-ball Lookahead diagram.<br>Refreshed NC, DNU, RFU descriptions. |

***Colophon***

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