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Jameco Part Number 1390856

M24C16, M24C08
M24C04, M24C02, M24C01

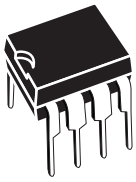
16Kbit, 8Kbit, 4Kbit, 2Kbit and 1Kbit Serial I²C bus EEPROM

Feature summary

- Two-wire I²C serial interface
  Supports 400kHz protocol
- Single supply voltage:
  - 2.5 to 5.5V for M24Cxx-W
  - 1.8 to 5.5V for M24Cxx-R
- Write Control input
- Byte and Page Write (up to 16 Bytes)
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)

Table 1. Product list

Reference	Part Number
M24C16	M24C16-W
	M24C16-R
M24C08	M24C08-W
	M24C08-R
M24C04	M24C04-W
	M24C04-R
M24C02	M24C02-W
	M24C02-R
M24C01	M24C01-W
	M24C01-R



PDIP8 (BN)

SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

TSSOP8 (DS)
3x3mm² body size

UFDFPN8 (MB)
2x3mm² (MLP)

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1 Summary description

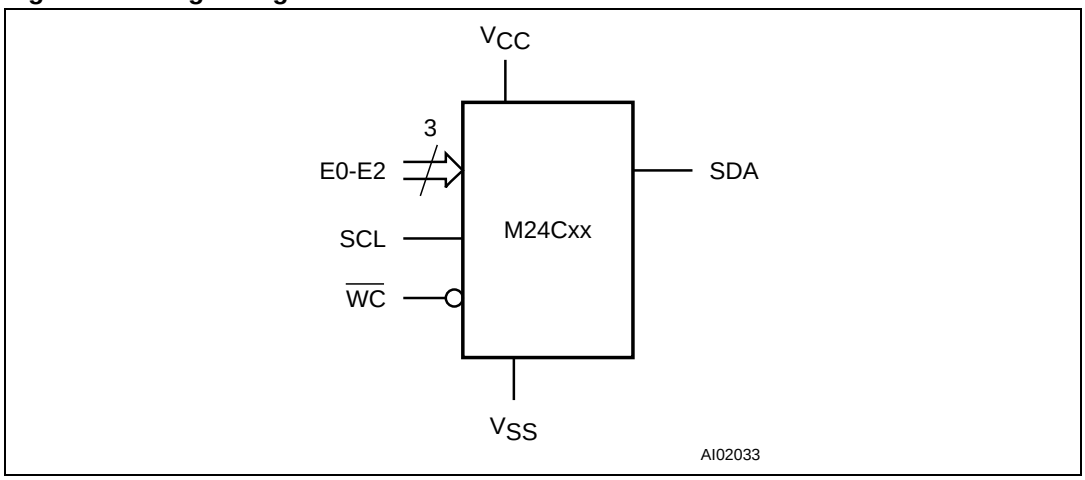
These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 2048/1024/512/256/128 x 8 (M24C16, M24C08, M24C04, M24C02 and M24C01).

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages.

ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 1. Logic diagram



I²C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I²C bus definition.

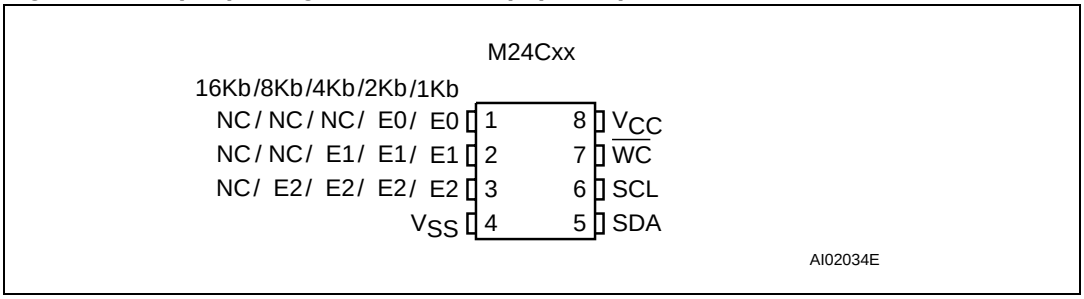
The device behaves as a slave in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$) (as described in *Table 3*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Table 2. Signal names

E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{\text{WC}}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. 8-pin package connections (top view)



1. NC = Not Connected
2. See *Section 7: Package mechanical* for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{CC}. (*Figure 4* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

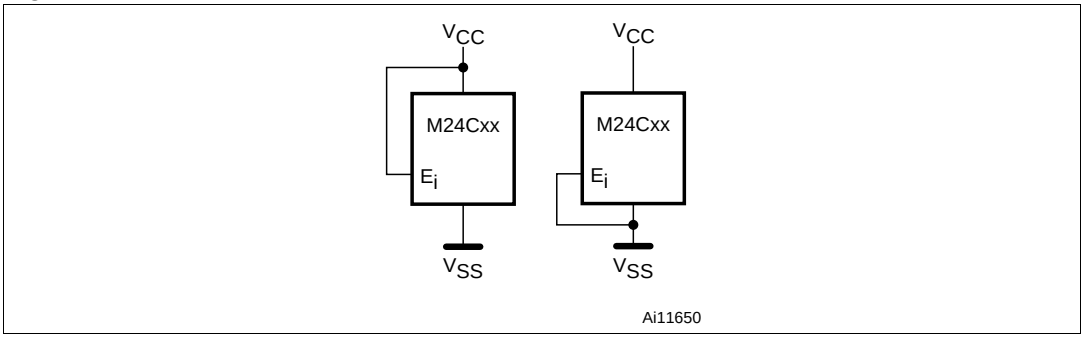
2.2 Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 4* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs must be tied to V_{CC} or V_{SS}, to establish the Device Select Code as shown in *Figure 3*.

Figure 3. Device select code



2.3.1 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven High, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

2.4 Supply voltage (V_{CC})

2.4.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 6* and *Table 7*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10nF to 100nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

The V_{CC} rise time must not vary faster than 1V/µs

2.4.2 Power-up and device Reset

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the Power On Reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 6* and *Table 7*).

When V_{CC} has passed the POR threshold, the device is reset and in Standby Power mode.

2.4.3 Power-down

At Power-down (where V_{CC} decreases continuously), as soon as V_{CC} drops from the operating voltage range to below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

During Power-down, the device must be deselected and in the Standby Power mode (that is there should be no internal Write cycle in progress).

Figure 4. Maximum R_P value versus bus parasitic capacitance (C) for an I²C bus

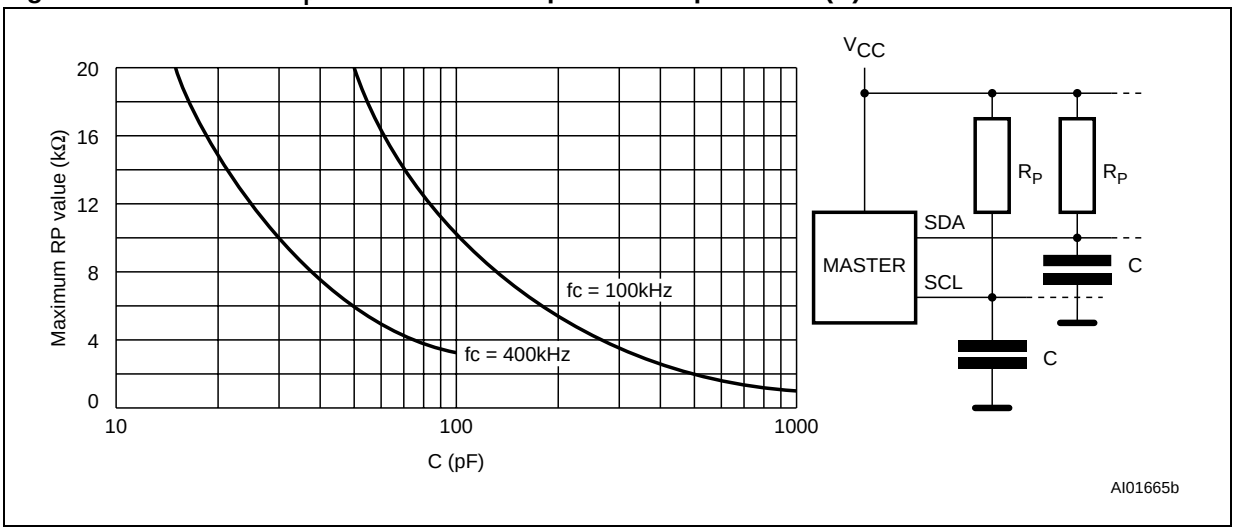


Figure 5. I²C bus protocol

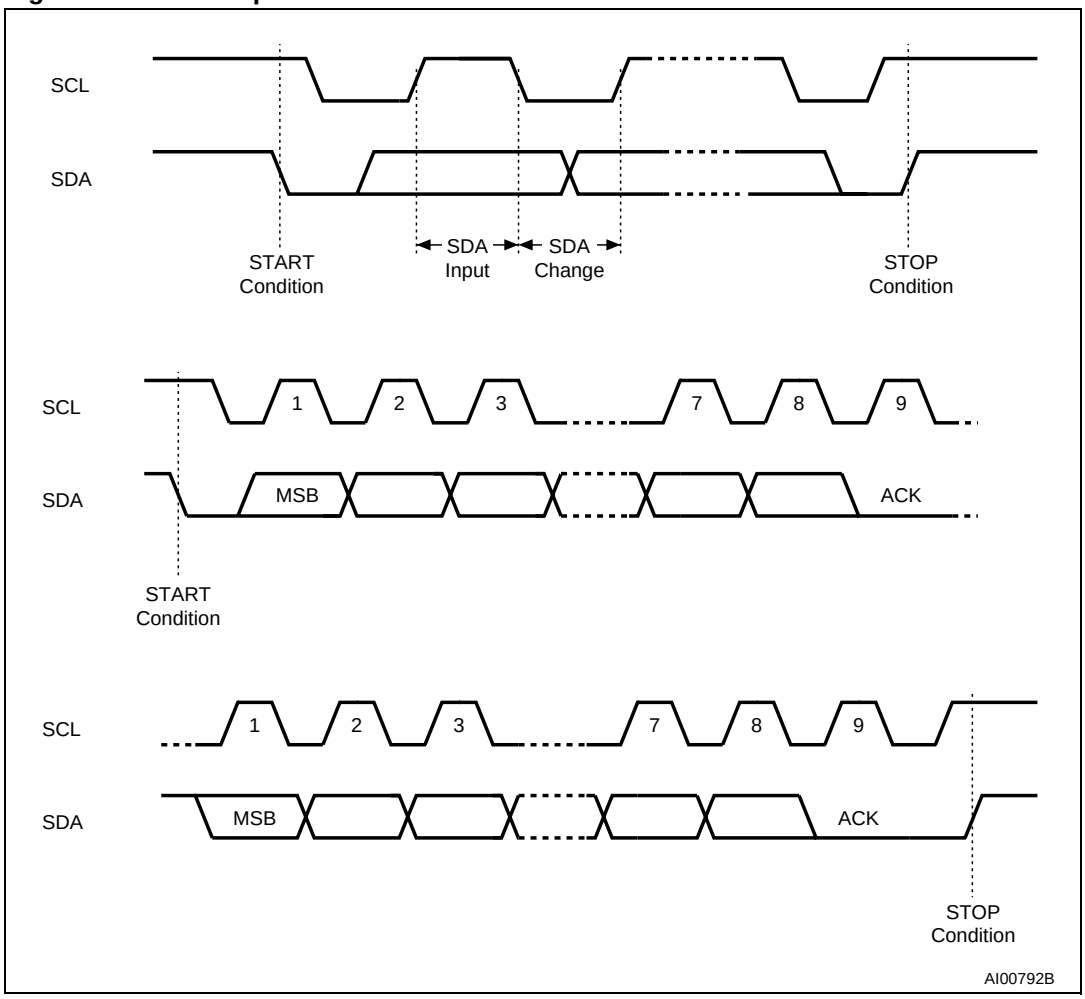


Table 3. Device select code

	Device Type Identifier(1)				Chip Enable(2),(3)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
M24C01 Select Code	1	0	1	0	E2	E1	E0	R$\overline{W}$
M24C02 Select Code	1	0	1	0	E2	E1	E0	R$\overline{W}$
M24C04 Select Code	1	0	1	0	E2	E1	A8	R$\overline{W}$
M24C08 Select Code	1	0	1	0	E2	A9	A8	R$\overline{W}$
M24C16 Select Code	1	0	1	0	A10	A9	A8	R$\overline{W}$

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.
3. A10, A9 and A8 represent most significant bits of the address.

3 Device operation

The device supports the I²C protocol. This is summarized in *Figure 5*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24Cxx device is always a slave in all communication.

3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal Write cycle.

3.3 Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

3.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in *Table 3* (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

Each device is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs. However, those devices with larger memory capacities (the M24C16, M24C08 and M24C04) need more address bits. E0 is not available for use on devices that need to use address line A8; E1 is not available for devices that need to use address line A9, and E2 is not available for devices that need to use address line A10 (see *Figure 2* and *Table 3* for details). Using the E0, E1 and E2 inputs, up to eight M24C02 (or M24C01), four M24C04, two M24C08 or one M24C16 devices can be connected to one I²C bus. In each case, and in the hybrid cases, this gives a total memory capacity of 16 Kbits, 2 KBytes (except where M24C01 devices are used).

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

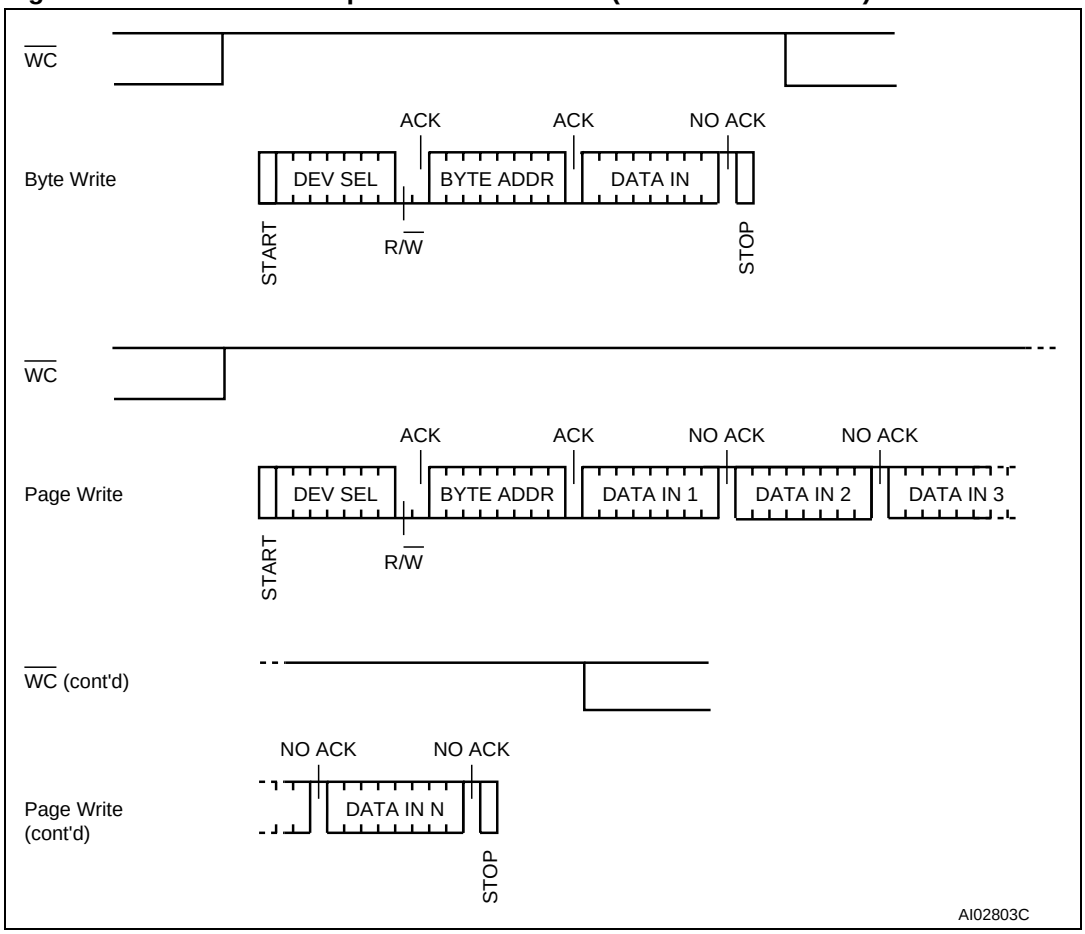
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Table 4. Operating modes

Mode	$\overline{\text{RW}}$ bit	$\overline{\text{WC}}$(1)	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, $\overline{\text{RW}}$ = 1
Random Address Read	0	X	1	START, Device Select, $\overline{\text{RW}}$ = 0, Address
	1	X		reSTART, Device Select, $\overline{\text{RW}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, $\overline{\text{RW}}$ = 0
Page Write	0	V_{IL}	≤16	START, Device Select, $\overline{\text{RW}}$ = 0

1. X = V_{IH} or V_{IL}.

Figure 6. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



3.6 Write operations

Following a Start condition the bus master sends a Device Select Code with the Read/$\overline{Write}$ bit ($R\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 7*, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

3.6.1 Byte Write

After the Device Select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High (during the period from the Start condition until the end of the address byte), the device replies to the data byte with NoAck, as shown in *Figure 6*, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 7*.

3.6.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as ‘roll-over’ occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is Low. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High (during the period from the Start condition until the end of the address byte), the device replies to the data bytes with NoAck, as shown in *Figure 6*, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)

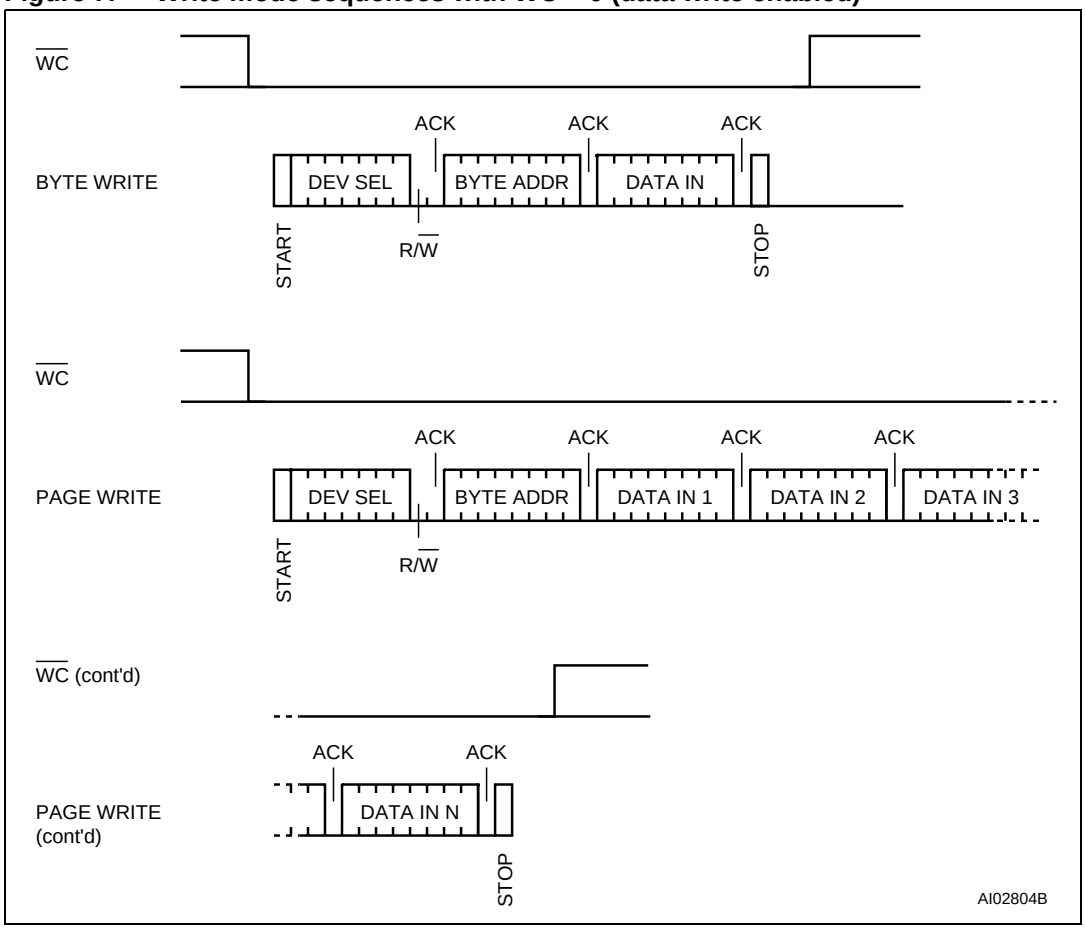
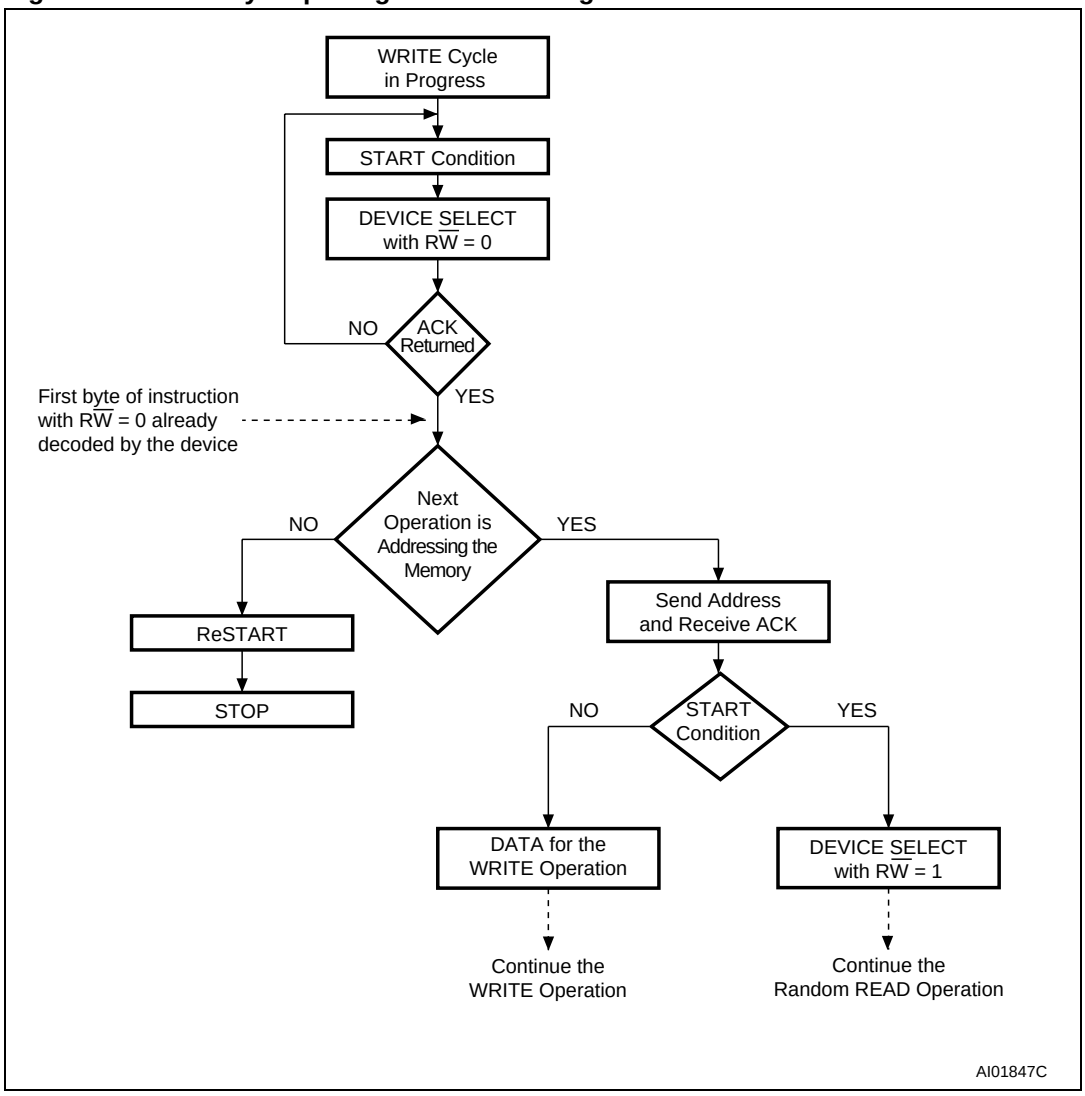


Figure 8. Write cycle polling flowchart using ACK



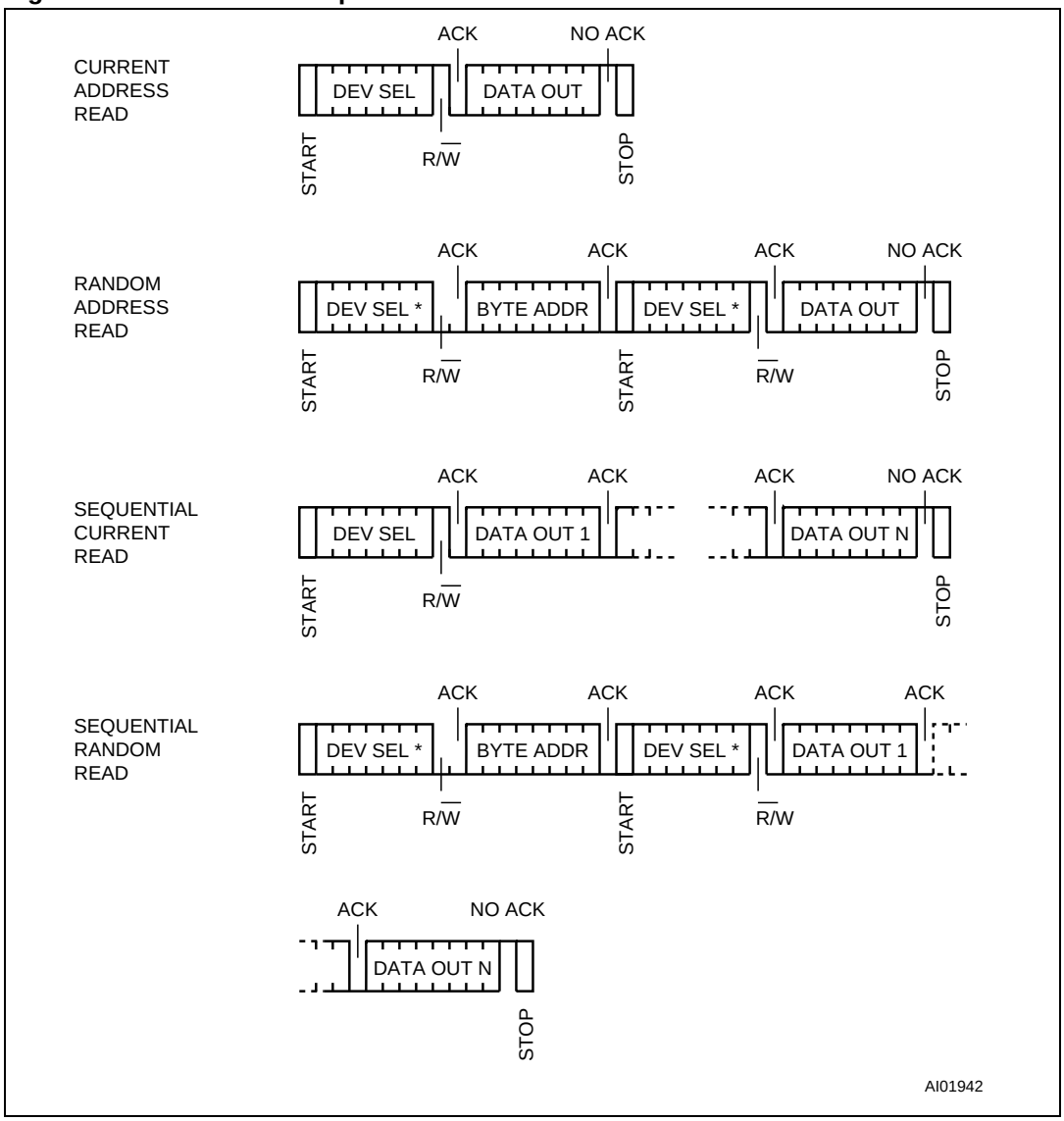
3.6.3 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 13* and *Table 14*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 9. Read mode sequences



1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

3.7 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

The device has an internal address counter which is incremented each time a byte is read.

3.7.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 9*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the Read/$\overline{Write}$ bit ($R\overline{W}$) set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

3.7.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the Read/Write bit ($\overline{RW}$) set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

3.7.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

3.7.4 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9^{th} bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Stand-by mode.

4 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

5 Maximum rating

Stressing the device outside the ratings listed in *Table 5* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–40	130	°C
T_{STG}	Storage Temperature	–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	see note (1)		°C
	PDIP-Specific Lead Temperature during Soldering		260(2)	°C
V_{IO}	Input or Output range	–0.50	6.5	V
V_{CC}	Supply Voltage	–0.50	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. T_{LEAD} max must not be applied for more than 10s.

1. T_{LEAD} max must not be applied for more than 10s.
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500Ω, R2=500Ω).

6 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 6. Operating conditions (M24Cxx-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature (Device Grade 6)	–40	85	°C
	Ambient Operating Temperature (Device Grade 3)	–40	125	°C

Table 7. Operating conditions (M24Cxx-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 8. DC characteristics (M24Cxx-W, Device Grade 6)

Symbol	Parameter	Test Condition (in addition to those in *Table 6*)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0, E1,and E2)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC}, for 2.5V < V_{CC} = < 5.5V		1	µA
V_{IL}	Input Low Voltage (1)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input High Voltage (1)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA when V_{CC} = 2.5V or I_{OL} = 3mA when V_{CC} = 5.5V		0.4	V

1. The voltage source driving only E0, E1 and E2 inputs must provide an impedance of less than 1kΩ

Table 9. DC characteristics (M24Cxx-W, Device Grade 3)

Symbol	Parameter	Test Condition (in addition to those in *Table 6*)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0, E1,and E2)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_C=400kHz (rise/fall time < 30ns)		3	mA
		V_{CC} =2.5V, f_C=400kHz (rise/fall time < 30ns)		3	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5 V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
V_{IL}	Input Low Voltage(1)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input High Voltage(1)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA when V_{CC} = 2.5V or I_{OL} = 3mA when V_{CC} = 5.5V		0.4	V

1. The voltage source driving only E0, E1 and E2 inputs must provide an impedance of less than 1kΩ

Table 10. DC characteristics (M24Cxx-R)

Symbol	Parameter	Test Condition (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0, E1,and E2)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =1.8V, f_c=400kHz (rise/fall time < 30ns)		0.8	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC}, 1.8V < V_{CC} < 2.5V		1	µA
V_{IL}	Input Low Voltage (1)	2.5 V ≤V_{CC}	–0.45	0.3 V_{CC}	V
		1.8 V ≤V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input High Voltage (1)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 0.7 mA, V_{CC} = 1.8 V		0.2	V

1. The voltage source driving only E0, E1 and E2 inputs must provide an impedance of less than 1kΩ

Table 11. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 10. AC measurement I/O waveform

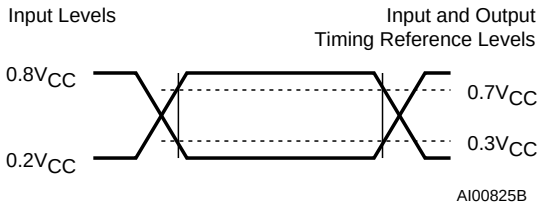


Table 12. Input parameters

Symbol	Parameter(1),(2)	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} < 0.3$ V	15	70	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

1. $T_A = 25°C$, f = 400kHz
2. Sampled only, not 100% tested.

Table 13. AC characteristics (M24Cxx-W)

Test conditions specified in *Table 6* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{DL1DL2}(1)	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV}(2)	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX}(3)	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W(4)	t_{WR}	Write Time		5	ms

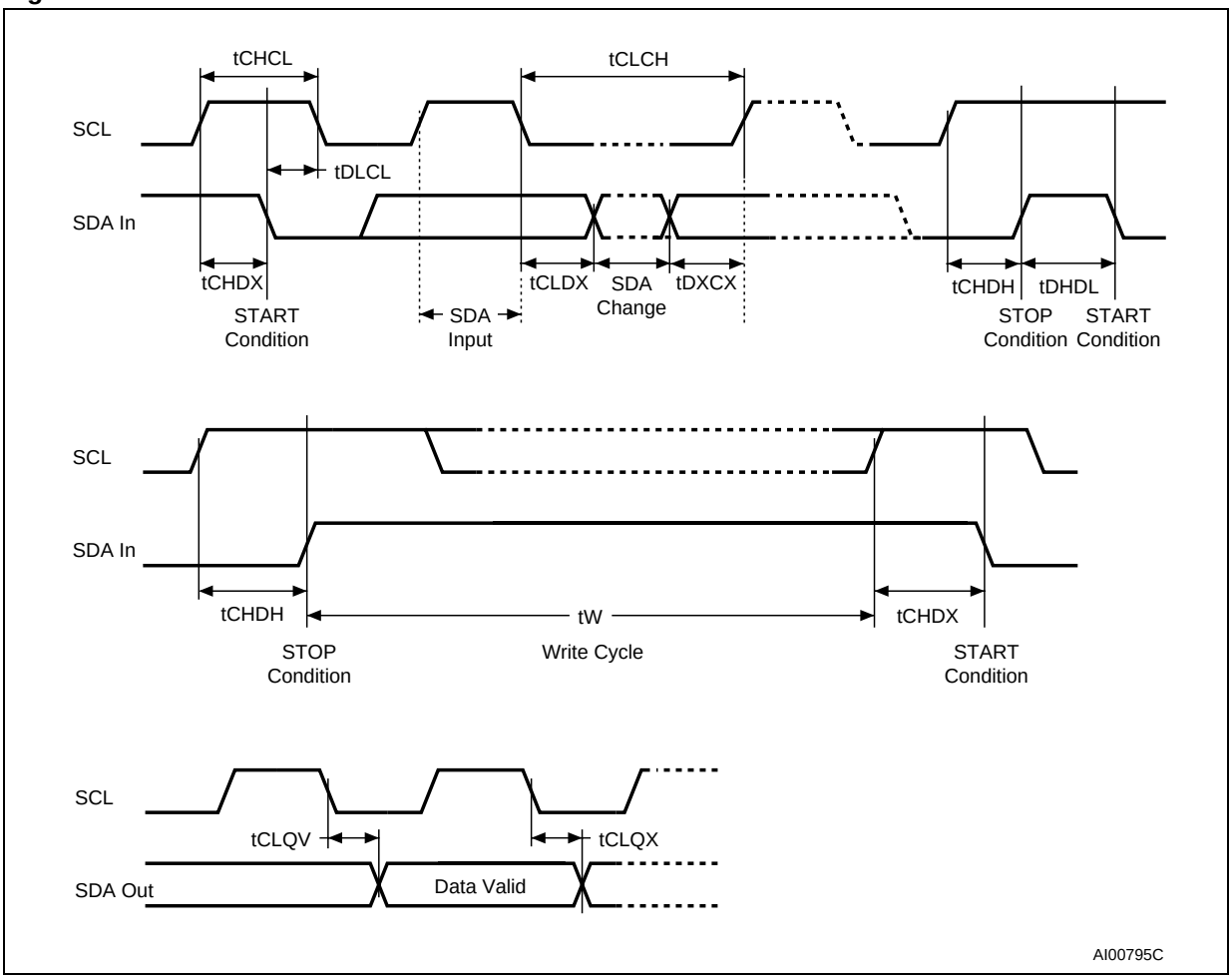
1. Sampled only, not 100% tested.
2. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
3. For a reSTART condition, or following a Write cycle.
4. Previous devices bearing the process letter “L” in the package marking guarantee a maximum write time of 10ms. For more information about these devices and their device identification, please ask your ST Sales Office for Process Change Notices PCN MPG/EE/0061 and 0062 (PCEE0061 and PCEE0062).

Table 14. AC characteristics (M24Cxx-R)

Test conditions specified in *Table 7* and *Table 10*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{DL1DL2}(1)	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV}(2)	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX}(3)	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		10	ms

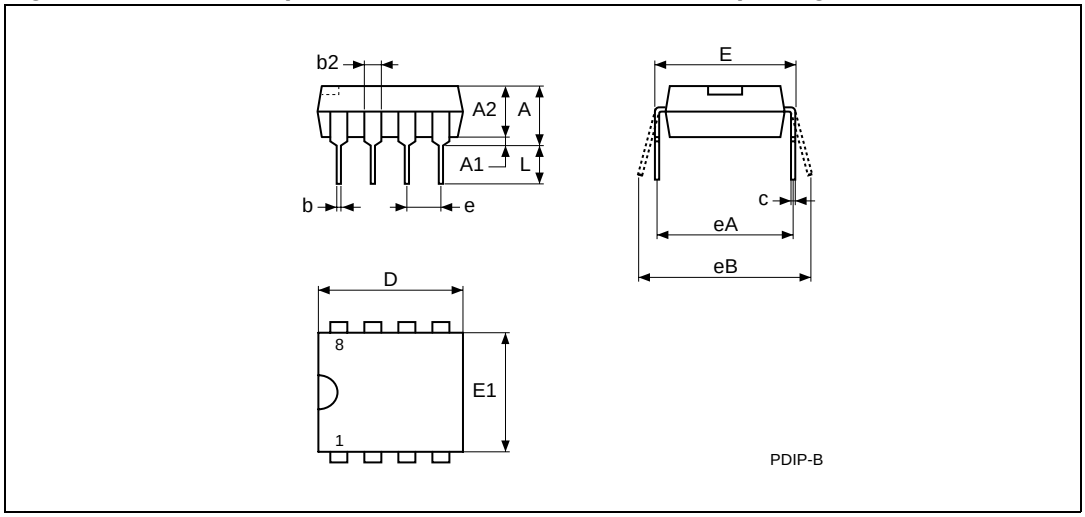
1. Sampled only, not 100% tested.
2. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
3. For a reSTART condition, or following a Write cycle.

Figure 11. AC waveforms



7 Package mechanical

Figure 12. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, package outline

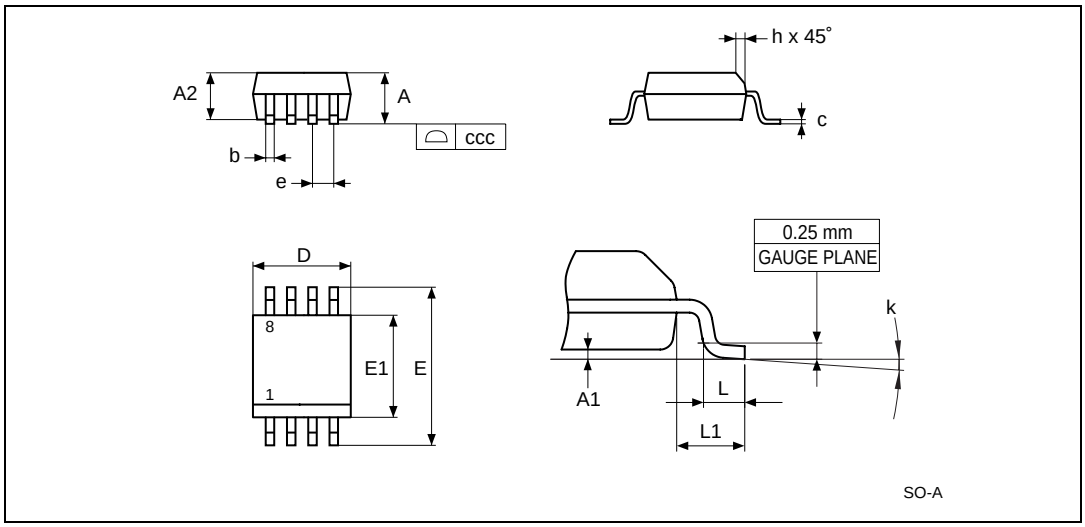


1. Drawing is not to scale.

Table 15. PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, package mechanical data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

Figure 13. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, package outline

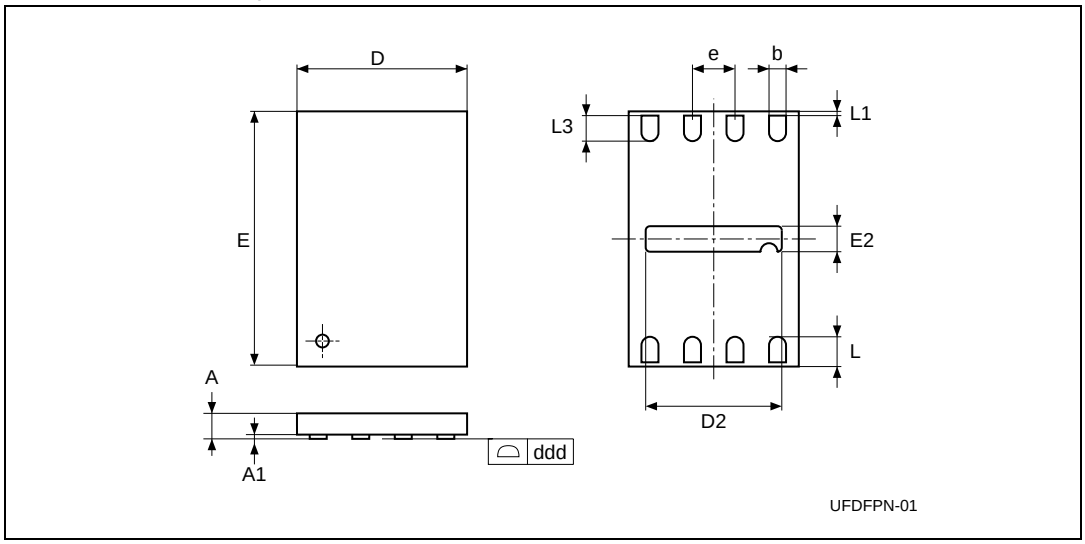


1. Drawing is not to scale.
2. The ‘1’ that appears in the top view of the package shows the position of pin 1 and the ‘N’ indicates the total number of pins.

Table 16. SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 14. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², outline

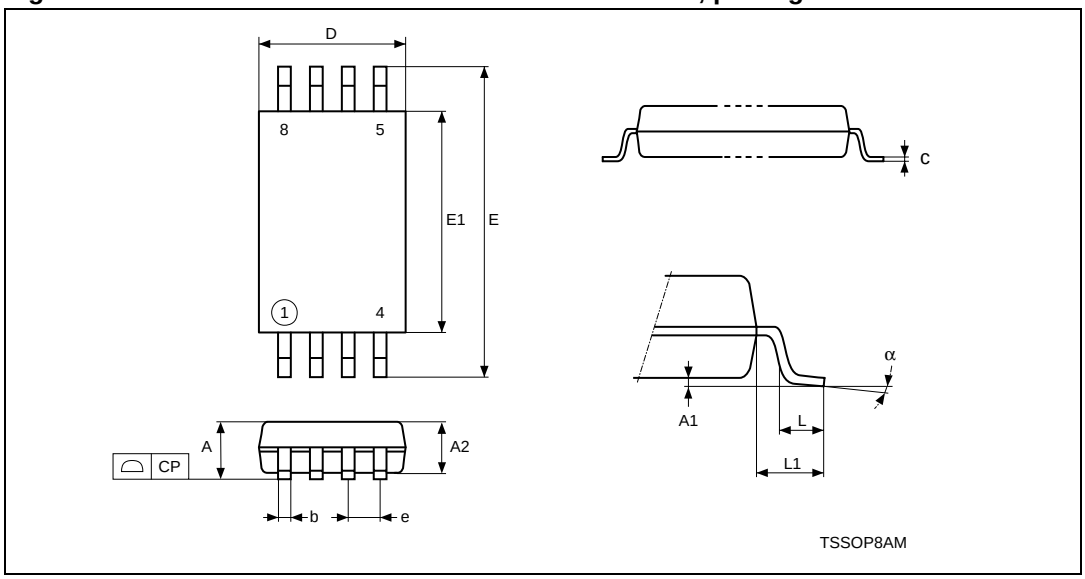


1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is pulled, internally, to V_{SS}. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.
3. The circle in the top view of the package indicates the position of pin 1.

Table 17. UFDFPN8 (MLP8) 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3mm², data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.50	0.60	0.022	0.020	0.024
A1	0.02	0.00	0.05	0.001	0.000	0.002
b	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00	1.90	2.10	0.079	0.075	0.083
D2	1.60	1.50	1.70	0.063	0.059	0.067
ddd			0.08			0.003
E	3.00	2.90	3.10	0.118	0.114	0.122
E2	0.20	0.10	0.30	0.008	0.004	0.012
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	

Figure 15. TSSOP8 – 8 lead Thin Shrink Small Outline, package outline

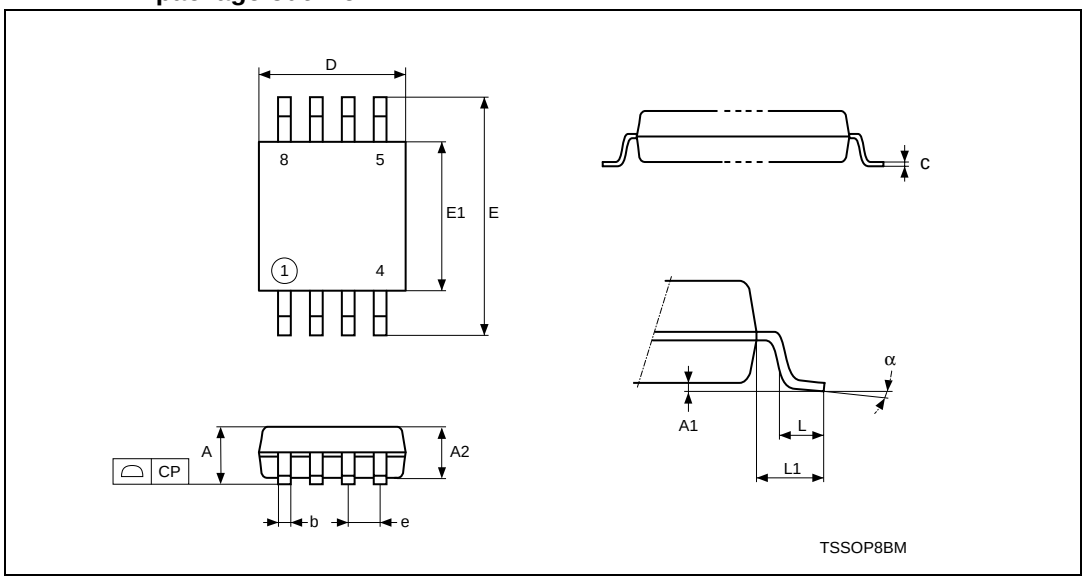


1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

Table 18. TSSOP8 – 8 lead Thin Shrink Small Outline, package mechanical data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

Figure 16. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, package outline



1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

Table 19. TSSOP8 3x3mm² – 8 lead Thin Shrink Small Outline, 3x3mm² body size, mechanical data

Symbol	millimeters			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.100			0.0433
A1		0.050	0.150		0.0020	0.0059
A2	0.850	0.750	0.950	0.0335	0.0295	0.0374
b		0.250	0.400		0.0098	0.0157
c		0.130	0.230		0.0051	0.0091
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
E	4.900	4.650	5.150	0.1929	0.1831	0.2028
E1	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
CP			0.100			0.0039
L	0.550	0.400	0.700	0.0217	0.0157	0.0276
L1	0.950			0.0374		
α		0°	6°		0°	6°

8 Part numbering

Table 20. Ordering information scheme

Example: M24C16 – W DW 3 T P /W

Device Type
M24 = I²C serial access EEPROM

Device Function
16 = 16 Kbit (2048 x 8)
08 = 8 Kbit (1024 x 8)
04 = 4 Kbit (512 x 8)
02 = 2 Kbit (256 x 8)
01 = 1 Kbit (128 x 8)

Operating Voltage
W = V_{CC} = 2.5 to 5.5V (400 kHz)
R = V_{CC} = 1.8 to 5.5V (400 kHz)

Package
BN = PDIP8
MN = SO8 (150 mil width)
MB = UDFDFPN8 (MLP8)
DW = TSSOP8 (169 mil width)
DS = TSSOP8 (3x3mm² body size, MSOP8)(1)

Device Grade
6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow
3 = Device tested with High Reliability Certified Flow(2).
Automotive temperature range (–40 to 125 °C)

Option
T = Tape and Reel Packing

Plating Technology
blank = Standard SnPb plating
P or G = ECOPACK® (RoHS compliant)

Process(3)
/W or /S = F6SP36%

1. Products sold in this package are Not Recommended for New Design.
2. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
3. Used only for Device Grade 3.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

9 Revision history

Table 21. Document revision history

Date	Version	Changes
10-Dec-1999	2.4	TSSOP8 Turned-Die package removed (p 2 and order information) Lead temperature added for TSSOP8 in table 2
18-Apr-2000	2.5	Labelling change to Fig-2D, correction of values for 'E' and main caption for Tab-13
05-May-2000	2.6	Extra labelling to Fig-2D
23-Nov-2000	3.0	SBGA package information removed to an annex document -R range changed to being the -S range, and the new -R range added
19-Feb-2001	3.1	SBGA package information put back in this document Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP changed to PDIP and Package Mechanical data updated Wording brought in to line with standard glossary
20-Apr-2001	3.2	Revision of DC and AC characteristics for the -S series
08-Oct-2001	3.3	Ball numbers added to the SBGA connections and package mechanical illustrations
09-Nov-2001	3.4	Specification of Test Condition for Leakage Currents in the DC Characteristics table improved
30-Jul-2002	3.5	Document reformatted using new template. SBGA5 package removed TSSOP8 (3x3mm² body size) package (MSOP8) added. -L voltage range added
04-Feb-2003	3.6	Document title spelt out more fully. "W"-marked devices with tw=5ms added.
05-May-2003	3.7	-R voltage range upgraded to 400kHz working, and no longer preliminary data. 5V voltage range at temperature range 3 (-xx3) no longer preliminary data. -S voltage range removed. -Wxx3 voltage+temp ranged added as preliminary data.
07-Oct-2003	4.0	Table of contents, and Pb-free options added. Minor wording changes in Summary Description, Power-On Reset, Memory Addressing, Read Operations. V_{IL}(min) improved to -0.45V. t_W(max) value for -R voltage range corrected.
17-Mar-2004	5.0	MLP package added. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) changed. Soldering temperature information clarified for RoHS compliant devices. Device grade information clarified. Process identification letter "G" information added. 2.2-5.5V range is removed, and 4.5-5.5V range is now Not for New Design

Table 21. Document revision history

Date	Version	Changes
7-Oct-2005	6.0	Product List summary table added. AEC-Q100-002 compliance. Device Grade information clarified. Updated Device internal reset section, *Figure 3*, *Figure 4*, *Table 14* and *Table 20* Added Ecopack® information. Updated tW=5ms for the M24Cxx-W.
17-Jan-2006	7.0	Pin numbers removed from silhouettes (see *on page 1*). *Internal Device Reset* paragraph moved to below *Section 2.4: Supply voltage (VCC)*. *Section 2.4: Supply voltage (VCC)* added below *Section 2: Signal description*. Test conditions for V_{OL} updated in *Table 8* and *Table 9* SO8N package specifications updated (see *Table 16*) New definition of I_{CC1} over the whole V_{CC} range (see Tables *8*, *9* and *10*).
19-Sep-2006	8	Document converted to new ST template. SO8 and UFDFPN8 package specifications updated (see *Section 7: Package mechanical*). *Section 2.4: Supply voltage (VCC)* clarified. I_{LI} value given with the device in Standby mode in Tables *8*, *9* and *10*. Information given in *Table 14: AC characteristics (M24Cxx-R)* are no longer preliminary data.

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