

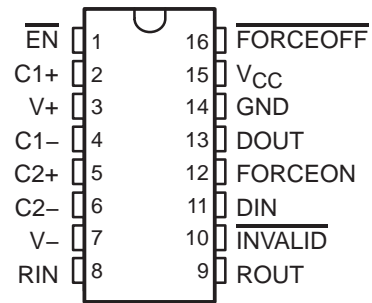
SN65C3221, SN75C3221

3-V TO 5.5-V SINGLE-CHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS351E – APRIL 2002 – REVISED OCTOBER 2004

- Operate With 3-V to 5.5-V V_{CC} Supply
- Operate Up To 1 Mbit/s
- Low Standby Current . . . 1 μ A Typ
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Auto-Powerdown Feature Automatically Disables Drivers for Power Savings
- Applications
 - Battery-Powered, Hand-Held, and Portable Equipment
 - PDAs and Palmtop PCs
 - Notebooks, Sub-Notebooks, and Laptops
 - Digital Cameras
 - Mobile Phones and Wireless Devices

DB OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN65C3221 and SN75C3221 consist of one line driver, one line receiver, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). These devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. These devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ μ s to 150 V/ μ s.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the devices do not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If FORCEOFF is set low and EN is high, both the driver and receiver are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The INVALID output notifies the user if an RS-232 signal is present at the receiver input. INVALID is high (valid data) if the receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 5 for receiver input levels.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|--------------|-----------------------|------------------|
| -0°C to 70°C | SSOP (DB) | Reel of 2000 | SN75C3221DBR | CA3221 |
| | TSSOP (PW) | Tube of 90 | SN75C3221PW | CA3221 |
| | | Reel of 2000 | SN75C3221PWR | |
| -40°C to 85°C | SSOP (DB) | Reel of 2000 | SN65C3221DBR | CB3221 |
| | TSSOP (PW) | Tube of 90 | SN65C3221PW | CB3221 |
| | | Reel of 2000 | SN65C3221PWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN65C3221, SN75C3221 3-V TO 5.5-V SINGLE-CHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

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Function Tables

EACH DRIVER

| INPUTS | | | VALID RIN RS-232 LEVEL | OUTPUT DOUT | DRIVER STATUS |
|--------|---------|----------|---------------------------|----------------|--|
| DIN | FORCEON | FORCEOFF | | | |
| X | X | L | X | Z | Powered off |
| L | H | H | X | H | Normal operation with auto-powerdown disabled |
| H | H | H | X | L | |
| L | L | H | Yes | H | Normal operation with auto-powerdown enabled |
| H | L | H | Yes | L | |
| L | L | H | No | Z | Powered off by auto-powerdown feature |
| H | L | H | No | Z | |

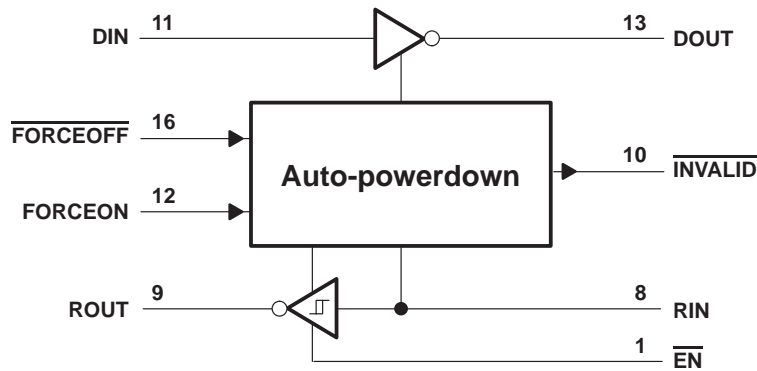
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

| INPUTS | | | VALID RIN RS-232 LEVEL | OUTPUT ROUT |
|--------|----|--|---------------------------|----------------|
| RIN | EN | | | |
| L | L | | X | H |
| H | L | | X | L |
| X | H | | X | Z |
| Open | L | | No | H |

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), Open = disconnected
input or connected driver off

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} (see Note 1) | –0.3 V to 6 V |
| Positive output supply voltage range, $V+$ (see Note 1) | –0.3 V to 7 V |
| Negative output supply voltage range, $V-$ (see Note 1) | 0.3 V to –7 V |
| Supply voltage difference, $V+ - V-$ (see Note 1) | 13 V |
| Input voltage range, V_I : Driver ($\overline{\text{FORCEOFF}}$, FORCEON , $\overline{\text{EN}}$) | –0.3 V to 6 V |
| Receiver | –25 V to 25 V |
| Output voltage range, V_O : Driver | –13.2 V to 13.2 V |
| Receiver (INVALID) | –0.3 V to $V_{CC} + 0.3$ V |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package | 82°C/W |
| PW package | 108°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to network GND.
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

| | | | MIN | NOM | MAX | UNIT |
|--|---|------------------|-----|-----|-----|------|
| Supply voltage | | $V_{CC} = 3.3$ V | 3 | 3.3 | 3.6 | V |
| | | $V_{CC} = 5$ V | 4.5 | 5 | 5.5 | |
| V_{IH} Driver and control high-level input voltage | DIN, $\overline{\text{FORCEOFF}}$, FORCEON , $\overline{\text{EN}}$ | $V_{CC} = 3.3$ V | 2 | | V | |
| | | $V_{CC} = 5$ V | 2.4 | | | |
| V_{IL} Driver and control low-level input voltage | DIN, $\overline{\text{FORCEOFF}}$, FORCEON , $\overline{\text{EN}}$ | | | 0.8 | V | |
| V_I Driver and control input voltage | DIN, $\overline{\text{FORCEOFF}}$, FORCEON | | 0 | 5.5 | V | |
| V_I Receiver input voltage | | | –25 | 25 | V | |
| T_A Operating free-air temperature | SN65C3221 | | –40 | 85 | °C | |
| | SN75C3221 | | 0 | 70 | | |

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT | |
|-----------|---|--|---|------------|---------|---------|---------|
| I_I | Input leakage current | $\overline{\text{FORCEOFF}}$, FORCEON , $\overline{\text{EN}}$ | | ± 0.01 | ± 1 | μ A | |
| I_{CC} | Supply current ($T_A = 25^\circ\text{C}$) | Auto-powerdown disabled | No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC} | | 0.3 | 1 | mA |
| | | Powered off | No load, $\overline{\text{FORCEOFF}}$ at GND | | 1 | 10 | |
| | | Auto-powerdown enabled | No load, $\overline{\text{FORCEOFF}}$ at V_{CC} , FORCEON at GND, All RIN are open or grounded | | 1 | 10 | μ A |

‡ All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.



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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|-------------------------------|--|--|-------|-----|------|
| V _{OH} | High-level output voltage | DOUT at R _L = 3 kΩ to GND, DIN = GND | 5 | 5.4 | | V |
| V _{OL} | Low-level output voltage | DOUT at R _L = 3 kΩ to GND, DIN = V _{CC} | -5 | -5.4 | | V |
| I _{IH} | High-level input current | V _I = V _{CC} | | ±0.01 | ±1 | μA |
| I _{IL} | Low-level input current | V _I at GND | | ±0.01 | ±1 | μA |
| I _{OS} | Short-circuit output current‡ | V _{CC} = 3.6 V, V _O = 0 V | | ±35 | ±60 | mA |
| | | V _{CC} = 5.5 V, V _O = 0 V | | ±35 | ±90 | |
| r _o | Output resistance | V _{CC} , V ₊ , and V ₋ = 0 V, V _O = ±2 V | 300 | 10M | | Ω |
| I _{off} | Output leakage current | FORCEOFF = GND | V _O = ±12 V, V _{CC} = 3 V to 3.6 V | | ±25 | μA |
| | | | V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V | | ±25 | |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-------------------------------------|---|--|------|------|-----|--------|
| Maximum data rate (see Figure 1) | R _L = 3 kΩ | C _L = 1000 pF | 250 | | | kbit/s |
| | | C _L = 250 pF, V _{CC} = 3 V to 4.5 V | 1000 | | | |
| | | C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V | 1000 | | | |
| t _{sk(p)} | Pulse skew§ | C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2 | 100 | | | ns |
| SR(tr) | Slew rate, transition region (see Figure 1) | V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ, C _L = 150 pF to 1000 pF | 18 | | 150 | V/μs |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

§ Pulse skew is defined as |t_{pLH} - t_{pHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

ESD protection

| TERMINAL | | TEST CONDITIONS | TYP | UNIT |
|----------|-----|-----------------|-----|------|
| NAME | NO. | | | |
| DOUT | 13 | HBM | ±15 | kV |



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|------------------|---|--------------------------------|-------------------------|-------------------------|-----|------|
| V _{OH} | High-level output voltage | I _{OH} = -1 mA | V _{CC} - 0.6 V | V _{CC} - 0.1 V | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{IT+} | Positive-going input threshold voltage | V _{CC} = 3.3 V | | 1.6 | 2.4 | V |
| | | V _{CC} = 5 V | | 1.9 | 2.4 | |
| V _{IT-} | Negative-going input threshold voltage | V _{CC} = 3.3 V | 0.6 | 1.1 | | V |
| | | V _{CC} = 5 V | 0.8 | 1.4 | | |
| V _{hys} | Input hysteresis (V _{IT+} - V _{IT-}) | | | 0.5 | | V |
| I _{off} | Output leakage current | FORCEOFF = 0 V | | ±0.05 | ±10 | μA |
| r _i | Input resistance | V _I = ±3 V to ±25 V | 3 | 5 | 7 | kΩ |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--------------------|---|--|-----|------|-----|------|
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 150 pF, See Figure 3 | | 150 | | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | C _L = 150 pF, See Figure 3 | | 150 | | ns |
| t _{en} | Output enable time | C _L = 150 pF, R _L = 3 kΩ, See Figure 4 | | 200 | | ns |
| t _{dis} | Output disable time | C _L = 150 pF, R _L = 3 kΩ, See Figure 4 | | 200 | | ns |
| t _{sk(p)} | Pulse skew‡ | See Figure 3 | | 50 | | ns |

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

ESD protection

| TERMINAL | | TEST CONDITIONS | TYP | UNIT |
|----------|-----|-----------------|-----|------|
| NAME | NO. | | | |
| RIN | 8 | HBM | ±15 | kV |



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AUTO-POWERDOWN SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------------------|--|--|--------------|-----|------|
| $V_{T+}(\text{valid})$ | Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage | FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$ | | 2.7 | V |
| $V_{T-}(\text{valid})$ | Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage | FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$ | -2.7 | | V |
| $V_{T}(\text{invalid})$ | Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage | FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$ | -0.3 | 0.3 | V |
| V_{OH} | $\overline{\text{INVALID}}$ high-level output voltage | $I_{OH} = -1 \text{ mA}$, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$ | $V_{CC}-0.6$ | | V |
| V_{OL} | $\overline{\text{INVALID}}$ low-level output voltage | $I_{OL} = 1.6 \text{ mA}$, FORCEON = GND, $\overline{\text{FORCEOFF}} = V_{CC}$ | | 0.4 | V |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | MIN | TYP† | MAX | UNIT |
|----------------------|---|-----|------|-----|---------------|
| t_{valid} | Propagation delay time, low- to high-level output | | 1 | | μs |
| t_{invalid} | Propagation delay time, high- to low-level output | | 30 | | μs |
| t_{en} | Supply enable time | | 100 | | μs |

† All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

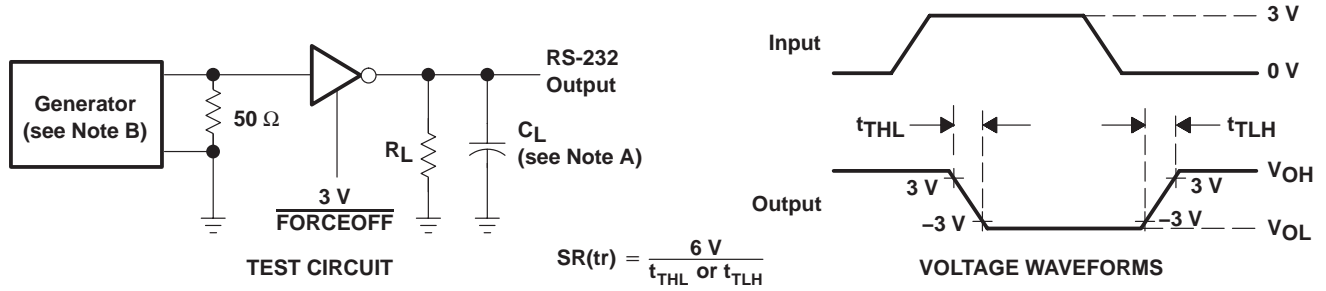


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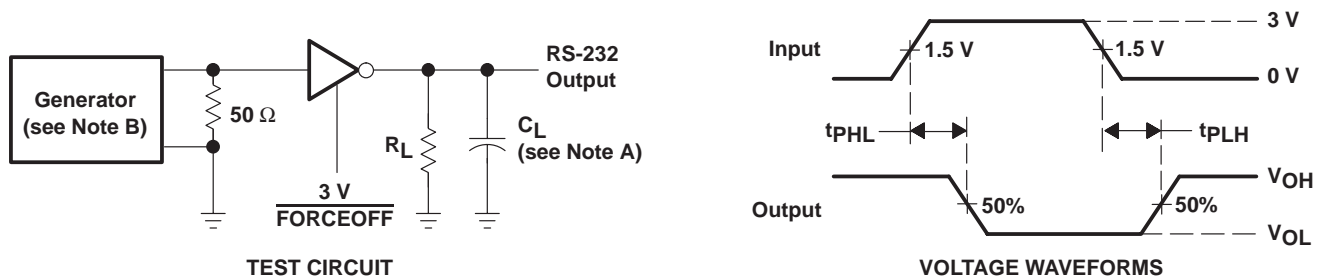
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PARAMETER MEASUREMENT INFORMATION



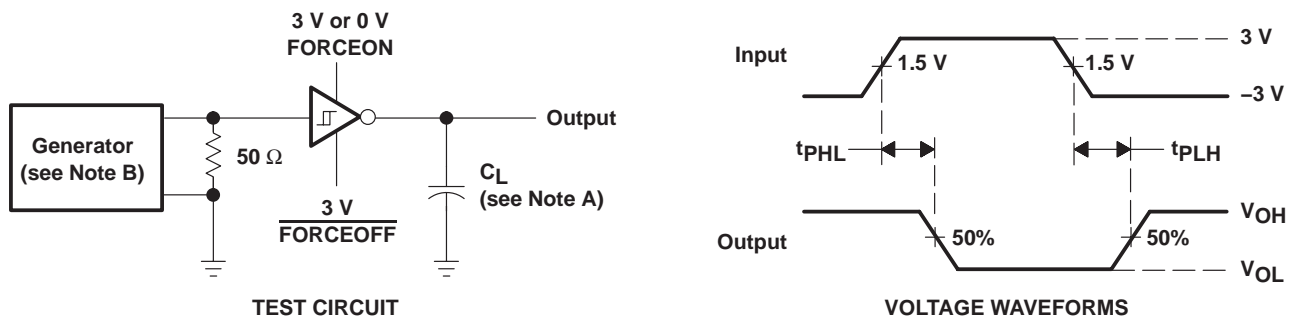
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 2. Driver Pulse Skew



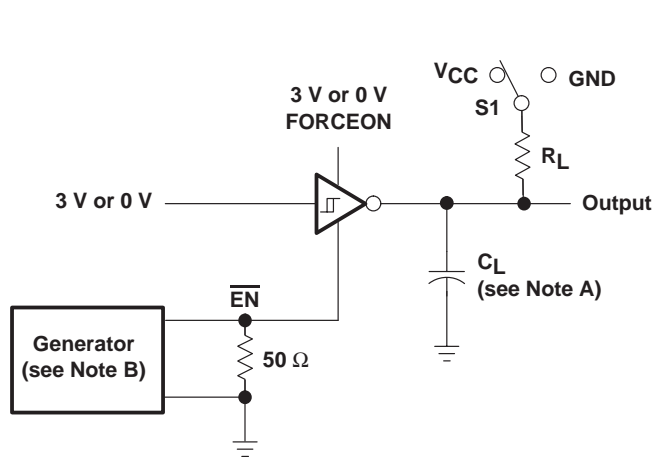
NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

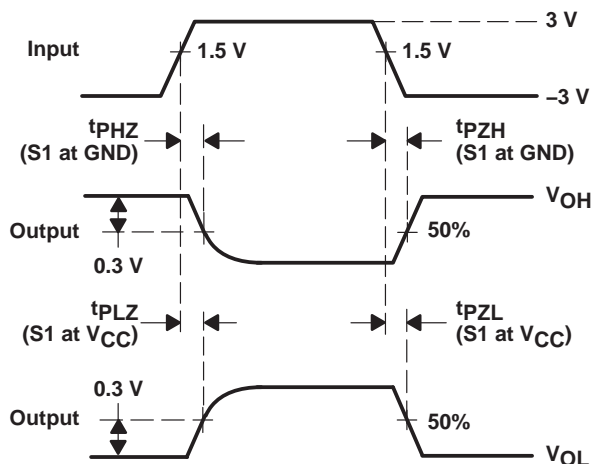
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

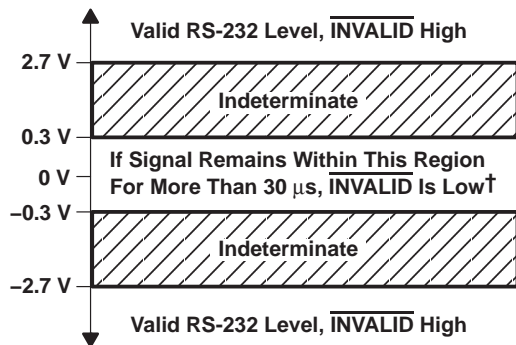
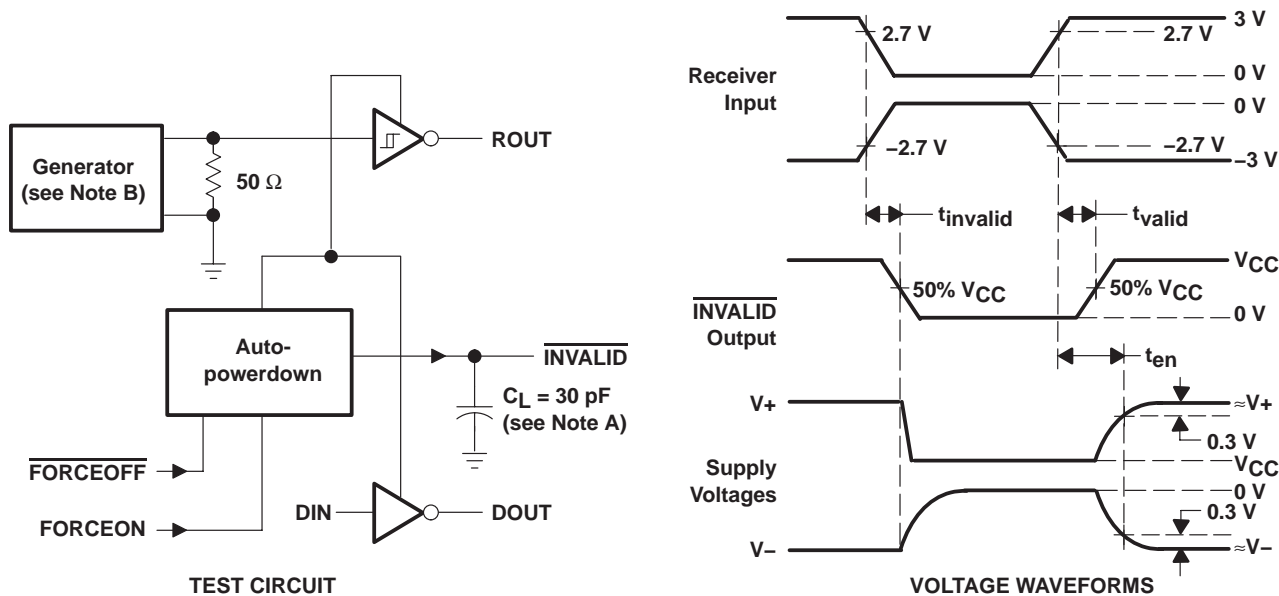


VOLTAGE WAVEFORMS

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
 - C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION



† Auto-powerdown disables drivers and reduces supply current to 1 μ A.

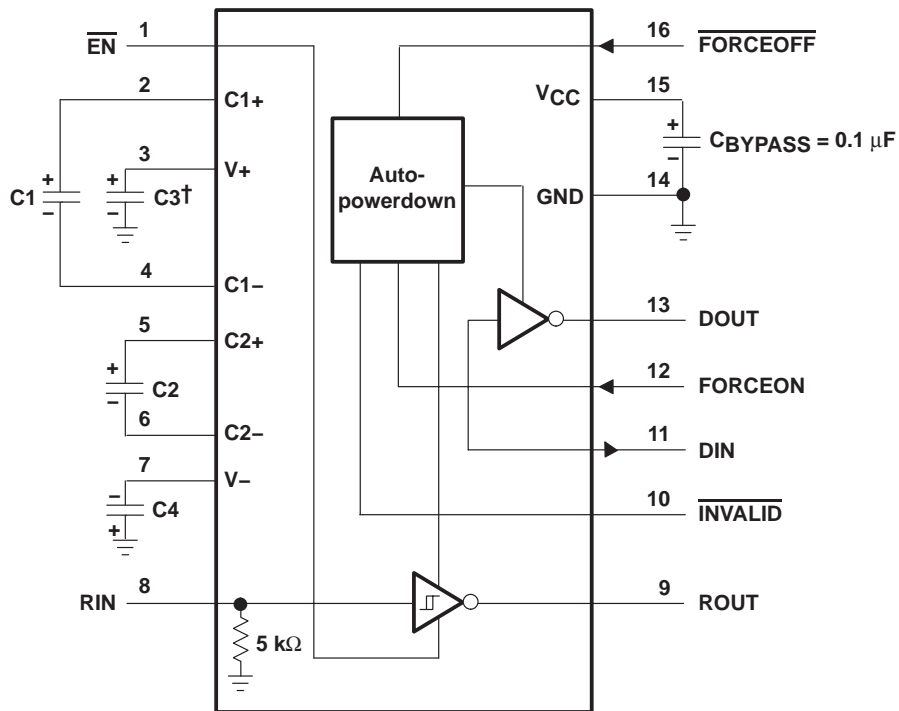
- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

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APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.
NOTE A: Resistor values shown are nominal.

V_{CC} vs CAPACITOR VALUES

| V _{CC} | C1 | C2, C3, and C4 |
|-----------------|----------|----------------|
| 3.3 V ± 0.3 V | 0.1 µF | 0.1 µF |
| 5 V ± 0.5 V | 0.047 µF | 0.33 µF |
| 3 V to 5.5 V | 0.1 µF | 0.47 µF |

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65C3221DB | ACTIVE | SSOP | DB | 16 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221DBE4 | ACTIVE | SSOP | DB | 16 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221DBG4 | ACTIVE | SSOP | DB | 16 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221DBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221DBG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN65C3221PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3221 | Samples |
| SN75C3221DBG4 | OBSOLETE | SSOP | DB | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN75C3221DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |
| SN75C3221DBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |
| SN75C3221DBG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |
| SN75C3221DW | PREVIEW | SOIC | DW | 16 | 40 | TBD | Call TI | Call TI | 0 to 70 | | |
| SN75C3221PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75C3221PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |
| SN75C3221PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |
| SN75C3221PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |
| SN75C3221PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |
| SN75C3221PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CA3221 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65C3221 :

- Automotive: [SN65C3221-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65C3221DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65C3221PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN75C3221DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN75C3221PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65C3221DBR | SSOP | DB | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN65C3221PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN75C3221DBR | SSOP | DB | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN75C3221PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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