

# AM26C32 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS104I – DECEMBER 1990 – REVISED SEPTEMBER 2004

- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11
- Low Power,  $I_{CC} = 10 \text{ mA Typ}$
- $\pm 7\text{-V}$  Common-Mode Range With  $\pm 200\text{-mV}$  Sensitivity
- Input Hysteresis . . . 60 mV Typ
- $t_{pd} = 17 \text{ ns Typ}$
- Operates From a Single 5-V Supply
- 3-State Outputs
- Input Fail-Safe Circuitry
- Improved Replacements for AM26LS32
- Available in Q-Temp Automotive
  - High Reliability Automotive Applications
  - Configuration Control/Print Support
  - Qualification to Automotive Standards

## description/ordering information

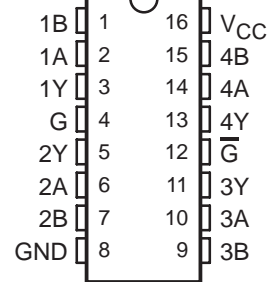
The AM26C32 is a quadruple differential line receiver for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design specifies that if the inputs are open, the outputs always are high.

The AM26C32 devices are manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32, while maintaining ac and dc performance.

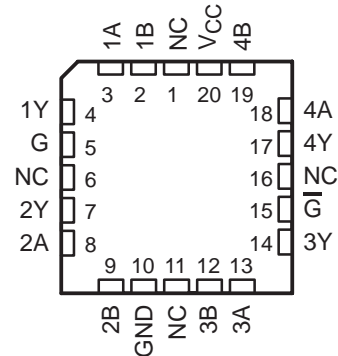
The AM26C32C is characterized for operation from 0°C to 70°C. The AM26C32I is characterized for operation from –40°C to 85°C. The AM26C32Q is characterized for operation from –40°C to 125°C. The AM26C32M is characterized for operation over the full military temperature range of –55°C to 125°C.

AM26C32C . . . D, N, OR NS PACKAGE  
AM26C32I . . . D, N, NS, OR PW PACKAGE  
AM26C32Q . . . D PACKAGE  
AM26C32M . . . J OR W PACKAGE

(TOP VIEW)



AM26C32M . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# AM26C32

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS104I – DECEMBER 1990 – REVISED SEPTEMBER 2004

### description/ordering information (continued)

#### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	AM26C32CN	AM26C32CN
	SOIC (D)	Tube of 40	AM26C32CD	AM26C32C
		Reel of 2500	AM26C32CDR	
	SOP (NS)	Reel of 2000	AM26C32CNSR	26C32
-40°C to 85°C	PDIP (N)	Tube of 25	AM26C32IN	AM26C32IN
	SOIC (D)	Tube of 40	AM26C32ID	AM26C32I
		Reel of 2500	AM26C32IDR	
	SOP (NS)	Reel of 2000	AM26C32INSR	26C32I
	TSSOP (PW)	Tube of 90	AM26C32IPW	26C32I
-40°C to 125°C	SOIC (D)	Tube of 40	AM26C32QD	AM26C32QD
-55°C to 125°C	CDIP (J)	Tube of 25	AM26C32MJ	AM26C32MJ
	CFP (W)	Tube of 150	AM26C32MW	AM26C32MW
	LCCC (FK)	Tube of 55	AM26C32MFK	AM26C32MFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE (each receiver)

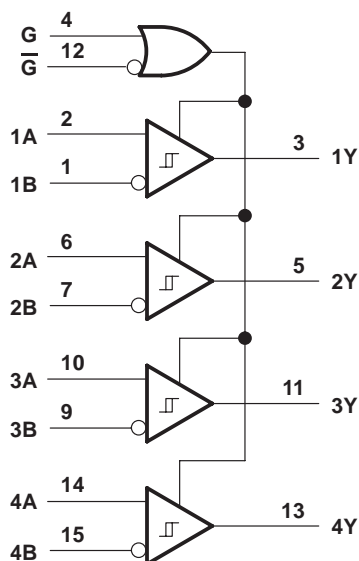
DIFFERENTIAL INPUT	ENABLES		OUTPUT Y
	G	$\bar{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

H = high level, L = low level, X = irrelevant  
Z = high impedance (off), ? = indeterminate

# AM26C32 QUADRUPLE DIFFERENTIAL LINE RECEIVER

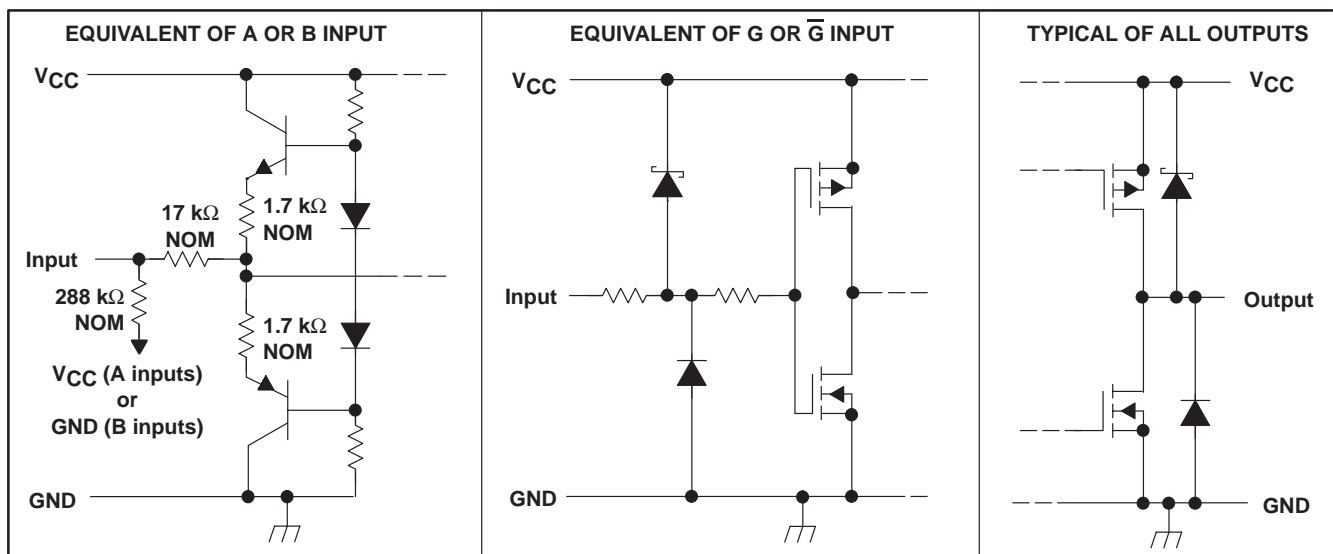
SLLS104I – DECEMBER 1990 – REVISED SEPTEMBER 2004

## logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

## schematics



# AM26C32

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS104I – DECEMBER 1990 – REVISED SEPTEMBER 2004

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage range, $V_I$ : A or B inputs .....	-11 V to 14 V
G or $\bar{G}$ inputs .....	-0.5 V to $V_{CC} + 0.5$ V
Differential input voltage range, $V_{ID}$ .....	-14 V to 14 V
Output voltage range, $V_O$ .....	-0.5 V to $V_{CC} + 0.5$ V
Output current, $I_O$ .....	$\pm 25$ mA
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3):	
D package .....	73°C/W
N package .....	67°C/W
NS package .....	64°C/W
PW package .....	108°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential output voltage,  $V_{OD}$ , are with respect to network GND. Currents into the device are positive and currents out of the device are negative.
2. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{IC}$	Common-mode input voltage			$\pm 7$	V
$I_{OH}$	High-level output current			-6	mA
$I_{OL}$	Low-level output current			6	mA
$T_A$	Operating free-air temperature	AM26C32C	0	70	°C
		AM26C32I	-40	85	
		AM26C32Q	-40	125	
		AM26C32M	-55	125	



# AM26C32

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS104I – DECEMBER 1990 – REVISED SEPTEMBER 2004

electrical characteristics over recommended ranges of  $V_{CC}$ ,  $V_{IC}$ , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IT+}$	Differential input high-threshold voltage	$V_O = V_{OH(min)}$ , $I_{OH} = -440 \mu A$	$V_{IC} = -7 V$ to $7 V$			0.2	V
			$V_{IC} = 0$ to $5.5 V$			0.1	
$V_{IT-}$	Differential input low-threshold voltage	$V_O = 0.45 V$ , $I_{OL} = 8 mA$	$V_{IC} = -7 V$ to $7 V$			$-0.2\ddagger$	V
			$V_{IC} = 0$ to $5.5 V$			$-0.1\ddagger$	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )				60		mV
$V_{IK}$	Enable input clamp voltage	$V_{CC} = 4.5 V$ ,	$I_I = -18 mA$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{ID} = 200 mV$ ,	$I_{OH} = -6 mA$	3.8			V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200 mV$ ,	$I_{OL} = 6 mA$		0.2	0.3	V
$I_{OZ}$	Off-state (high-impedance state) output current	$V_O = V_{CC}$ or GND			$\pm 0.5$	$\pm 5$	$\mu A$
$I_I$	Line input current	$V_I = 10 V$ ,	Other input at $0 V$			1.5	mA
		$V_I = -10 V$ ,	Other input at $0 V$			-2.5	
$I_{IH}$	High-level enable current	$V_I = 2.7 V$				20	$\mu A$
$I_{IL}$	Low-level enable current	$V_I = 0.4 V$				-100	$\mu A$
$r_i$	Input resistance	One input to ground		12	17		$k\Omega$
$I_{CC}$	Supply current	$V_{CC} = 5.5 V$			10	15	mA

† All typical values are at  $V_{CC} = 5 V$ ,  $V_{IC} = 0$ , and  $T_A = 25^\circ C$ .

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

switching characteristics over recommended ranges of operation conditions,  $C_L = 50 pF$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	AM26C32C AM26C32I			AM26C32Q AM26C32M			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 1	9	17	27	9	17	27	ns
$t_{PHL}$	Propagation delay time, high- to low-level output		9	17	27	9	17	27	
$t_{TLH}$	Output transition time, low- to high-level output	See Figure 1		4	9		4	10	ns
$t_{THL}$	Output transition time, high- to low-level output			4	9		4	9	
$t_{PZH}$	Output enable time to high level	See Figure 2		13	22		13	22	ns
$t_{PZL}$	Output enable time to low level			13	22		13	22	
$t_{PHZ}$	Output disable time from high level	See Figure 2		13	22		13	26	ns
$t_{PLZ}$	Output disable time from low level			13	22		13	25	

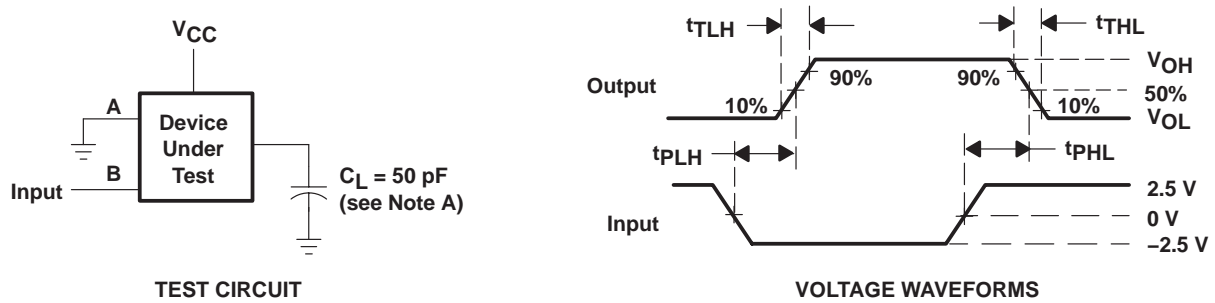
† All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .



# AM26C32 QUADRUPLE DIFFERENTIAL LINE RECEIVER

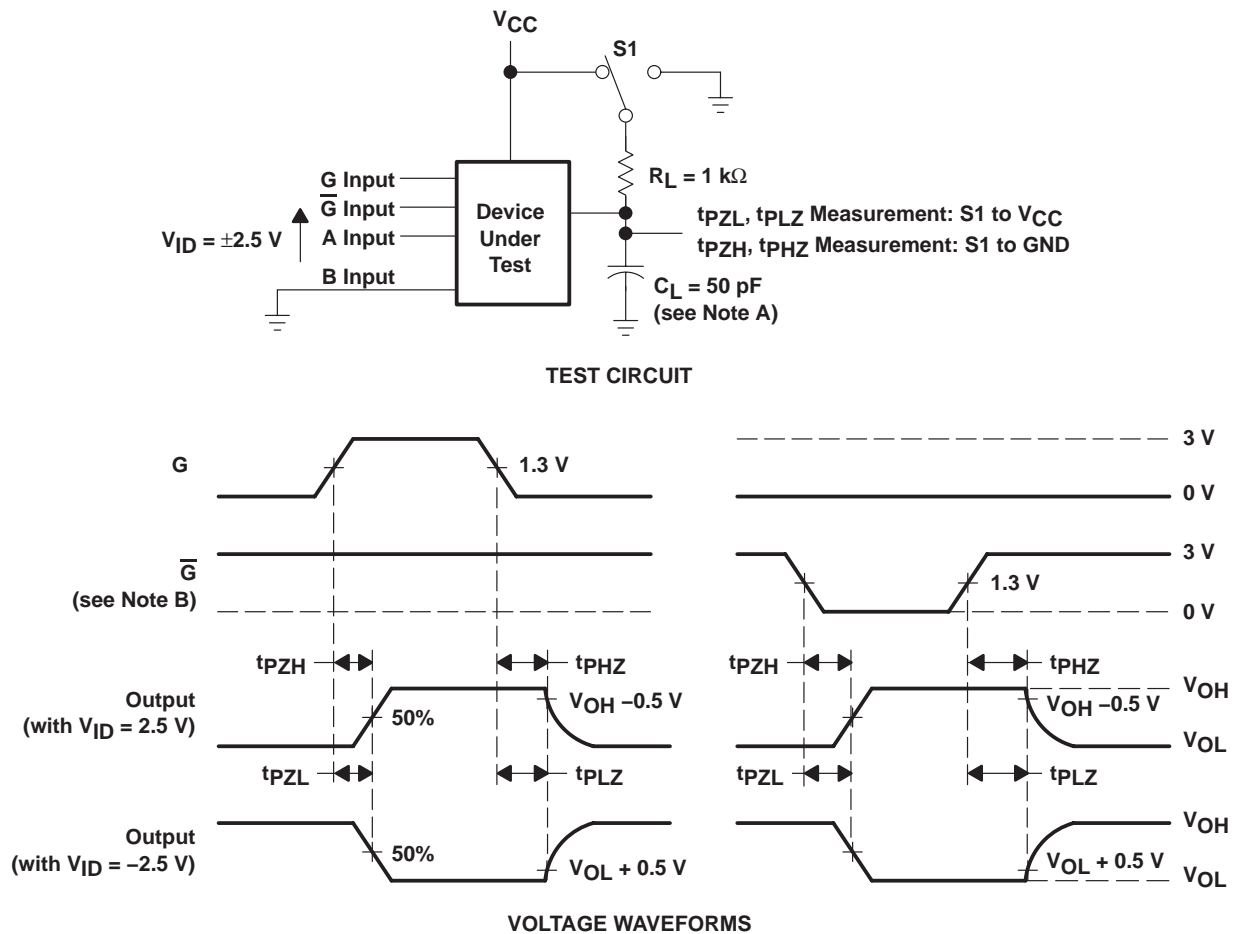
SLLS104I – DECEMBER 1990 – REVISED SEPTEMBER 2004

## PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 1. Switching Test Circuit and Voltage Waveforms



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle  $\leq$  50%,  $t_r = t_f = 6$  ns.

Figure 2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9164001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9164001Q2A AM26C32 MFKB	<a href="#">Samples</a>
5962-9164001QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QE A AM26C32MJB	<a href="#">Samples</a>
5962-9164001QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QF A AM26C32MWB	<a href="#">Samples</a>
AM26C32-W	ACTIVE	WAFERSALE	YS	0	3624	TBD	Call TI	Call TI			<a href="#">Samples</a>
AM26C32CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	<a href="#">Samples</a>
AM26C32CDBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	0 to 70		
AM26C32CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	<a href="#">Samples</a>
AM26C32CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	<a href="#">Samples</a>
AM26C32CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	<a href="#">Samples</a>
AM26C32CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	<a href="#">Samples</a>
AM26C32CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	<a href="#">Samples</a>
AM26C32CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	AM26C32CN	<a href="#">Samples</a>
AM26C32CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	AM26C32CN	<a href="#">Samples</a>
AM26C32CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	<a href="#">Samples</a>
AM26C32CNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	<a href="#">Samples</a>
AM26C32CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C32ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	<a href="#">Samples</a>
AM26C32IDBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85		
AM26C32IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	<a href="#">Samples</a>
AM26C32IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	<a href="#">Samples</a>
AM26C32IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	<a href="#">Samples</a>
AM26C32IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	<a href="#">Samples</a>
AM26C32IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	<a href="#">Samples</a>
AM26C32IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	AM26C32IN	<a href="#">Samples</a>
AM26C32INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	AM26C32IN	<a href="#">Samples</a>
AM26C32INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32INSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32INSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32IPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	<a href="#">Samples</a>
AM26C32MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										MFKB	
AM26C32MJB	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QE A AM26C32MJB	<a href="#">Samples</a>
AM26C32MWB	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QF A AM26C32MWB	<a href="#">Samples</a>
AM26C32QD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C32Q	<a href="#">Samples</a>
AM26C32QDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	26C32Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF AM26C32, AM26C32M :**

- Catalog: [AM26C32](#)
- Enhanced Product: [AM26C32-EP](#), [AM26C32-EP](#)
- Military: [AM26C32M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C32CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C32IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C32IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C32CDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26C32IDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26C32IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

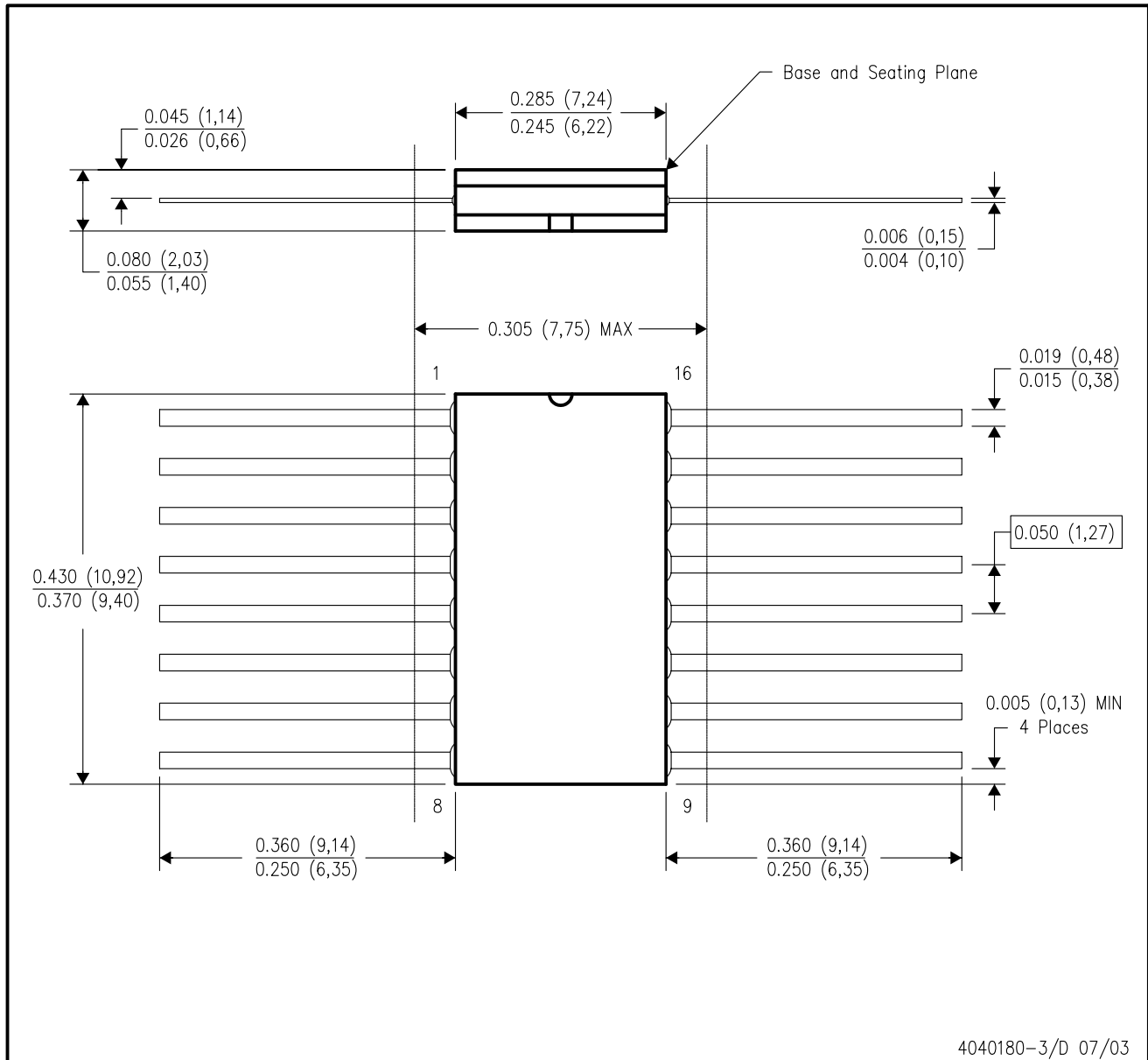


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

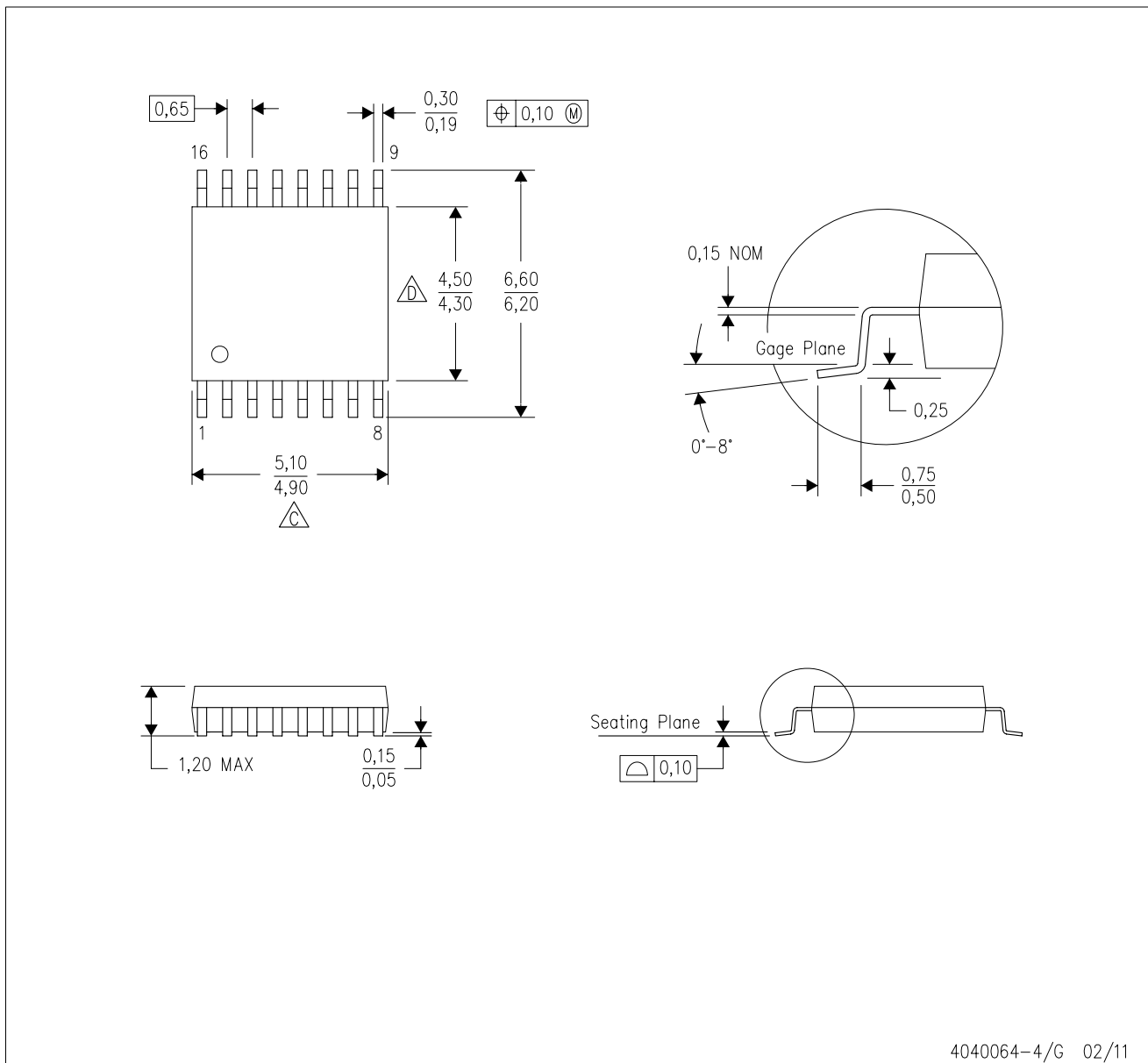
PLASTIC SMALL OUTLINE





- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

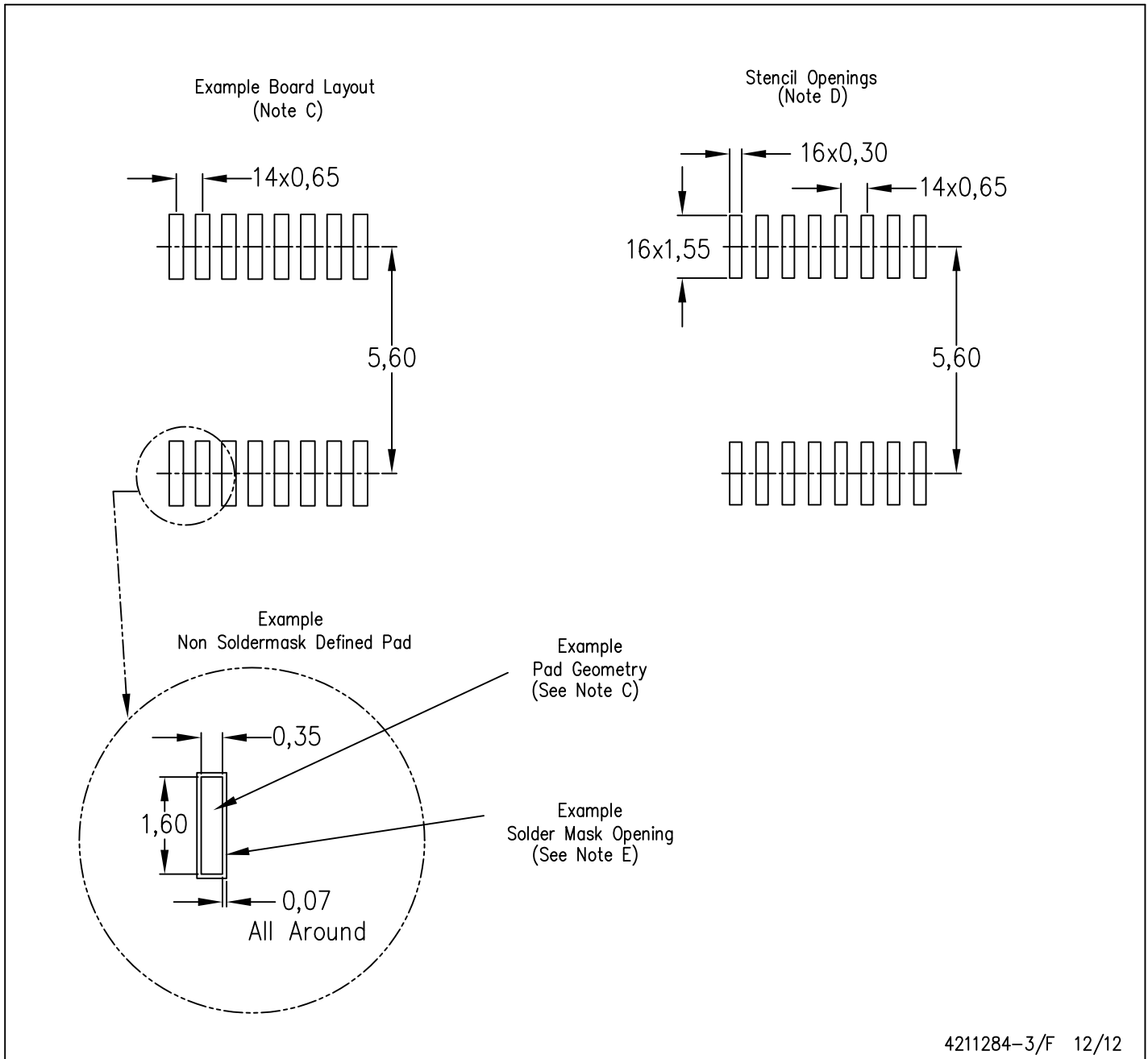


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)