TPS7A30-49EVM-567

This user's guide describes the characteristics, operation, and use of theTPS7A30-49EVM-567 Evaluation Module (EVM) as a reference design to facilitate engineering evaluation of the TPS7A3001 negative voltage low-dropout (LDO) regulator and/or the TPS7A4901 positive voltage LDO regulator for individual or split-rail applications. Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

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1 Introduction

The Texas Instruments TPS7A30-49EVM-567 EVM helps designers evaluate the operation and performance of the TPS7A3001 and/or the TPS7A4901 LDO regulator for possible use in their circuit applications. This particular EVM configuration is preconfigured to output –15 Vdc and +15 Vdc for ease of demonstration in certain standard industrial applications, e.g., requiring positive and negative voltages to power an operational amplifier-based, signal-conditioning circuitry. Alternatively, each LDO channel can be adjusted individually to any output voltage between 1.2 V and 33 V (negative and positive, respectively) as required by only changing a resistor value in accordance with the given equation. The TPS7A3001 can supply up to 200-mA-rated load current and the TPS7A4901 can supply up to 150 mA each using the MSOP-8, PowerPAD™ package. Both circuits have been optimized for ac performance including PSRR and load transient response using capacitors rated over the full voltage range of each regulator.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7A30-49EVM-567.

2.1 Negative Voltage Input/Output Connectors and Jumper Descriptions For TPS7A3001 LDO Circuit

- **J1 (–VIN)** – The negative input supply voltage connector. Twist the negative input lead and ground lead, and keep them as short as possible to minimize EMI transmission. Additional bulk aluminum electrolytic capacitance must be added/connected between J1 and J2 if the supply leads are greater than 6 inches. An additional 47-µF or greater capacitor improves the transient response and reduces parasitic ringing due to long wire connections.
- **J2 (GND)** – Ground-return connection for the negative input power supply.
- **J3 (EN)** – Negative voltage, output enable. To enable the negative voltage output, connect a jumper between ON, pin 1 to EN, pin 2. To disable the negative voltage output, connect the jumper between EN, center pin 2 and OFF, pin 3.
- **J4 (–VOUT)** – Negative voltage, output connector.
- **J5 (GND)** – Negative voltage output ground-return connector.

2.2 Positive Voltage Input/Output Connectors and Jumper Descriptions fo the TPS7A4901 LDO Circuit

- **J6 (+VIN)** – The positive input supply voltage connector. Twist the positive input lead and ground lead, and keep them as short as possible to minimize EMI transmission. Additional bulk aluminum electrolytic capacitance must be added/connected between J6 and J7 if the supply leads are greater than 6 inches. An additional 47-µF or greater capacitor improves the transient response and reduces parasitic ringing due to long wire connections.
- **J7 (GND)** – Ground-return connection for the positive input power supply.
- **J8 (EN)** – Positive voltage, output enable. To enable the positive voltage output, connect a jumper between ON, pin 1 to EN, pin 2. To disable the positive voltage output, connect the jumper between EN, center pin 2 and OFF, pin 3.
- **J9 (+VOUT)** – Negative voltage, output connector.
- **J10 (GND)** – Positive voltage output ground-return connector.

2.3 Soldering Guidelines

Any solder re-work to modify the EVM for the purpose of repair or other application reasons must be performed using a hot-air system to avoid damaging the integrated circuit (IC).

2.4 Equipment Interconnect

2.4.1 Negative Voltage LDO, TPS7A3001, Interconnect

- **Negative Input Supply Voltage:** Turn off the negative input power supply after verifying that its output voltage is greater than –35 V. Connect the negative voltage lead from the negative side of the supply to the J1 (–VIN) connector of the EVM. Connect the ground lead from the positive side of the power supply to J2 (GND) of the EVM.
- Connect a 0-mA to 200-mA load between the negative output, J4 (–VOUT) and the negative output return at J5 (GND).

2.4.2 Positive Voltage LDO, TPS7A4901, Interconnect

- **Positive Input Supply Voltage:** Turn off the positive input power supply after verifying that its output voltage is less than +35 V. Connect the positive voltage lead from the positive side of the supply to the J6 (+VIN) connector of the EVM. Connect the ground lead from the negative side of the power supply to J7 (GND) of the EVM.
- Connect a 0-mA to 150-mA load between the positive output, J9 (+VOUT), and the negative output return at J10 (GND).

3 Operation

- Turn on the negative voltage input power supply to J1 (–VIN). For initial operation, it is recommended that the negative input power supply be set to –18 V.
- Enable the negative output, –VOUT, as desired by connecting the J3 jumper between ON and EN.
- Vary the load and the voltage at –VIN as necessary for test purposes.
- Turn on the positive voltage input power supply to J6 (+VIN). For initial operation, it is recommended that the positive input power supply be set to +18 V.
- Enable the positive output, +VOUT, as desired by connecting the J8 jumper between ON and EN.
- Vary the load and the voltage at +VIN as necessary for test purposes.

4 Adjustable Operation

The nominal output voltage for the typical LDO circuit employing the TPS7A3001 or the TPS7A4901 is set by two external resistors, R1and R2, as illustrated in Figure 1. R1 and R2 can be calculated for any output voltage using the equation shown in Equation 1 and by finding the Vref voltage found in the respective data sheet in the Electrical Characteristics table.

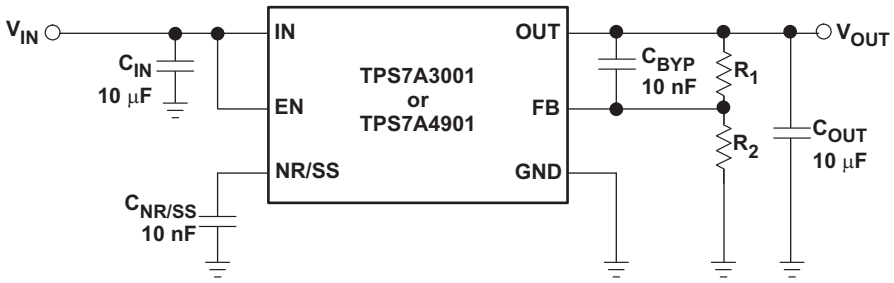


Figure 1. LDO Schematic Showing the R_1 and R_2 Adjustment Resistors

$$R_2 = R_1 \div [(V_{OUT}/V_{FB}) - 1] \qquad \text{Where } V_{OUT} / (R_1 + R_2) \geq 5\ \mu A \tag{1}$$

Once the resistor values have been calculated, the new resistors can be installed appropriately in the correct place using the printed-circuit board (PCB) and schematic diagrams of Figure 5 and Figure 8.

Suggestion: When recalculating the resistor values for a particular desired output voltage, change only the R_2 value in order to maintain that the frequency domain zero formed by R_1 and C_{BYP} are in accordance with Equation 2.

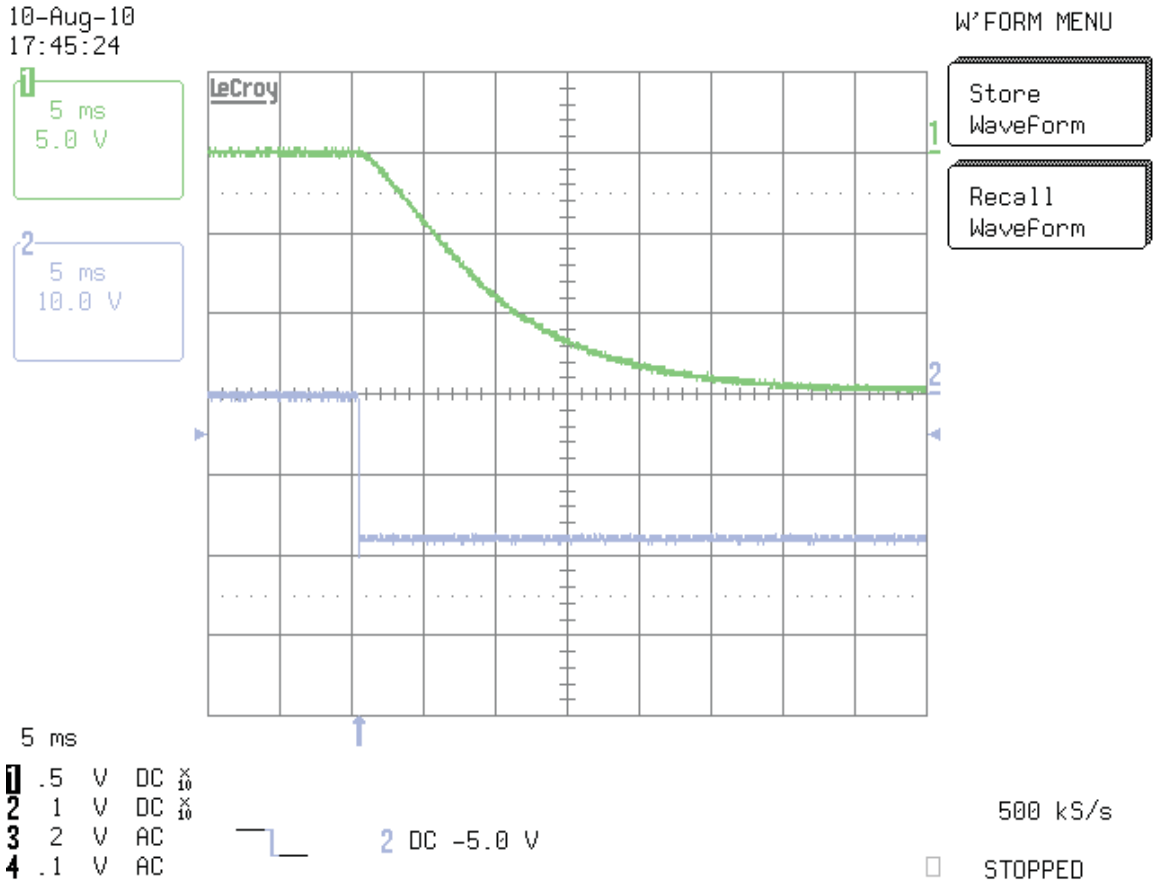
$$F_Z = 1/(2 \times \pi \times R_1 \times C_{BYP}) \tag{2}$$

5 Test Results

This section provides typical performance waveforms for the TLV710xxEVM PCB.

5.1 Turnon Output Ramp: Negative Voltage LDO, TPS7A3001 Circuit

Figure 2 shows the turnon waveforms where the Enable is connected to the –VIN. The –VIN turnon voltage steps down to –18 V (shown on Ch2 of the Figure 2 plot) followed by the –VOUT which ramps down –15 V. This negative-going turnon ramp represents the effects of both the soft-start capacitor, C_{SS}, as well as the soft-start effect contributed by the bypass capacitor, C_{BYP}, across the upper feedback resistor.

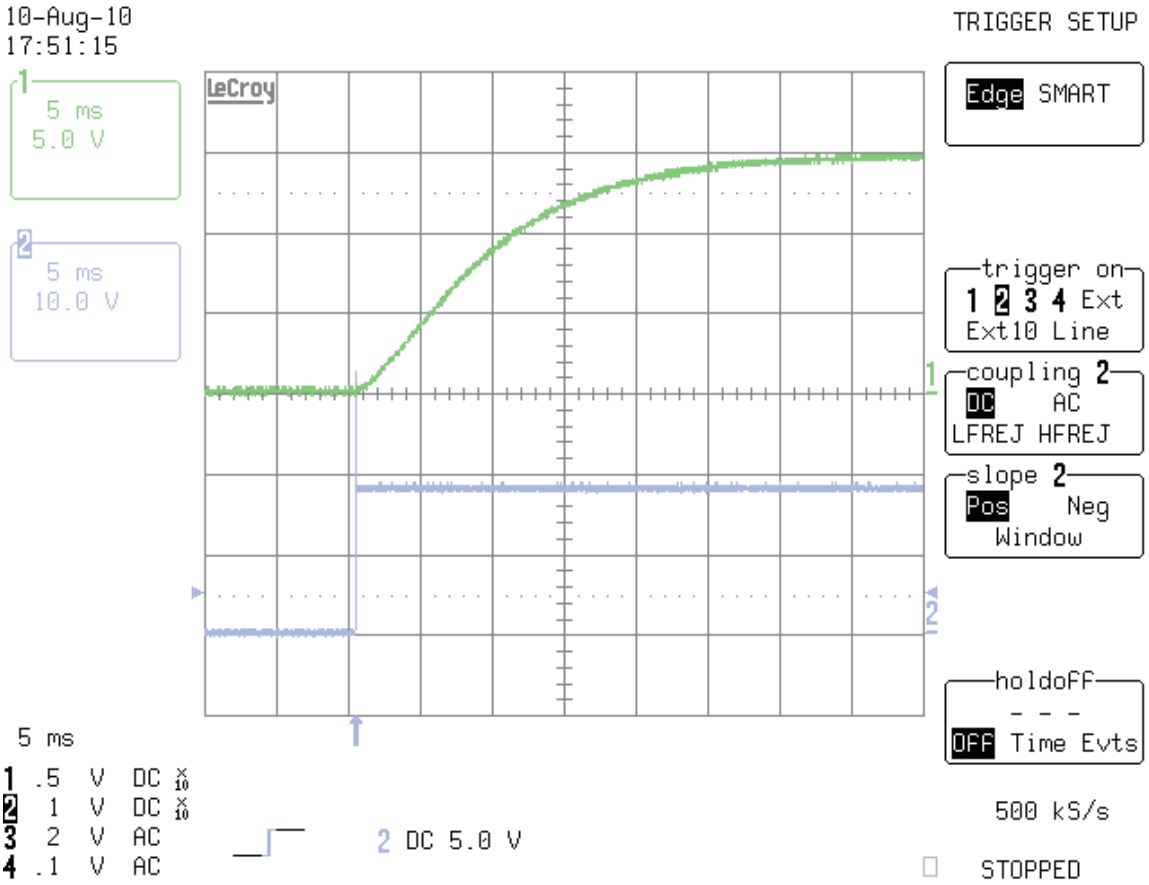


Ch1(–VOUT), Ramp Down to -15.V, and Ch2 (–VIN), Input Step Turnon Voltage to -18V.

Figure 2. TPS7A3001 –VOUT Ramp at Turnon

5.2 Turnon Output Ramp: Positive Voltage LDO, TPS7A4901 Circuit

Figure 3 shows the turnon waveforms where the Enable is connected to the +VIN. The +VIN turnon voltage steps to +18 V (shown on Ch2 of the Figure 2 plot) followed by the +VOUT ramp up to +15 V. This positive-going turnon ramp represents the effects of both the soft-start capacitor, C_{SS}, as well as the soft-start effect contributed by the bypass capacitor, C_{BYP}, across the upper feedback resistor.

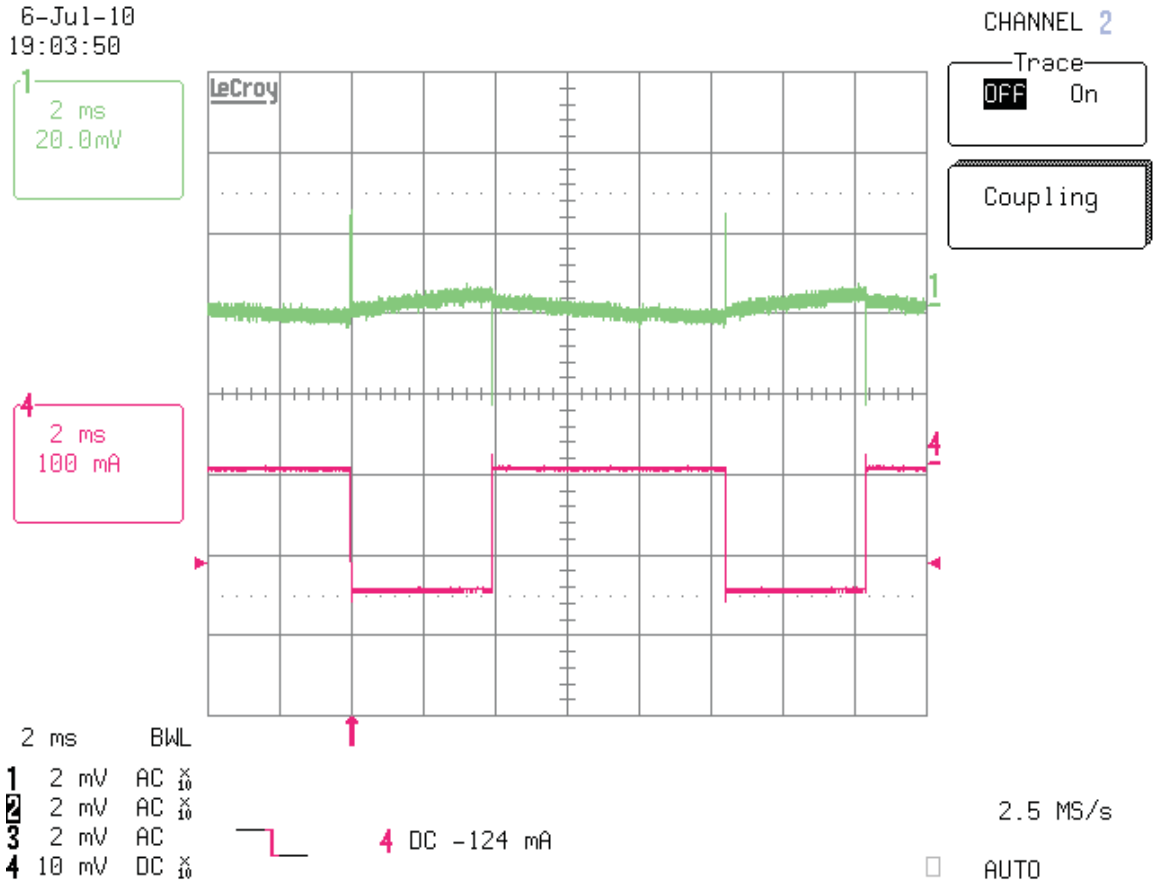


Ch1(+VOUT), Ramp Up to +15.V, and Ch2 (+VIN), Input Step Turnon Voltage to +18V

Figure 3. TPS7A4901 +VOUT Ramp at Turnon

5.3 –VOUT Load Transient Applied to the Negative LDO Circuit, TPS7A3001

Figure 4 shows the load transient response – oscilloscope channel 1 – for a 10-mA to 150-mA load transient applied to –VOUT (–15-V output). Oscilloscope channel 4 shows the load current transient.

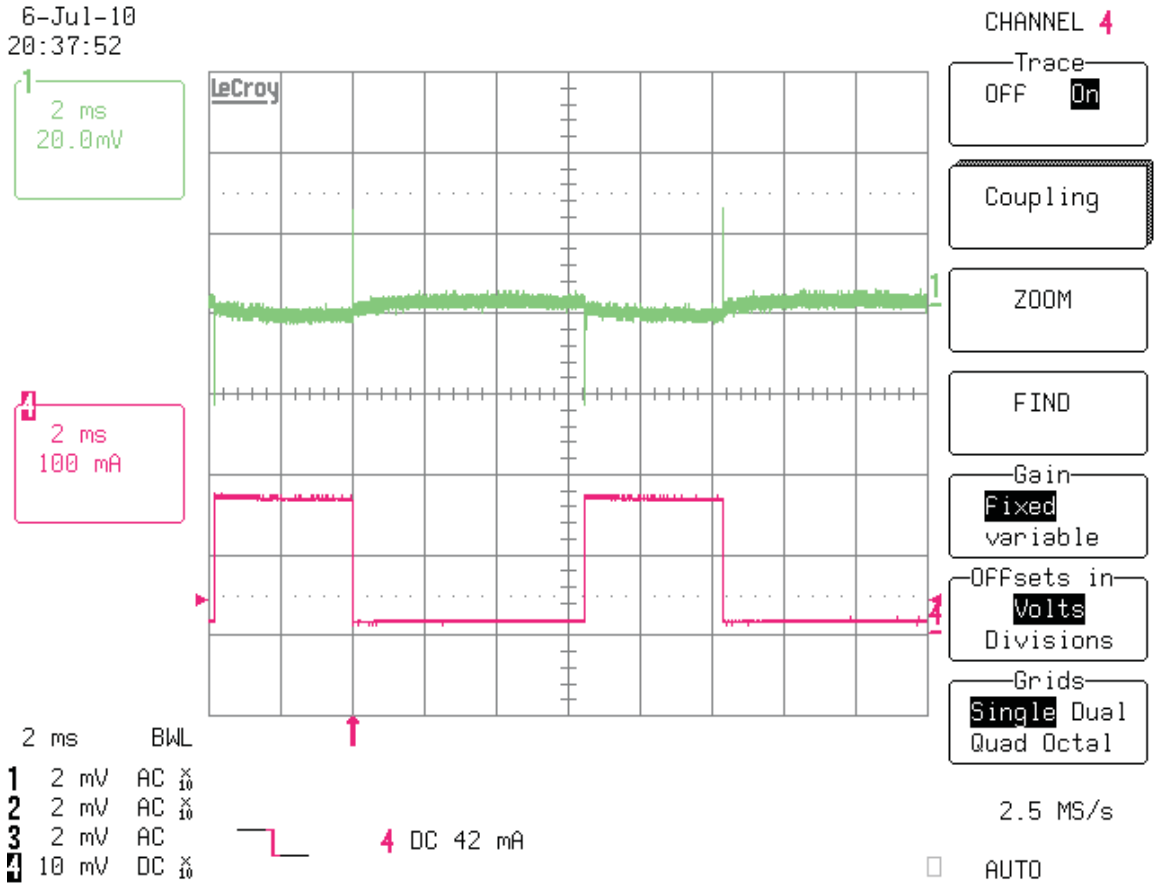


Ch 1 (-VOUT) Voltage Transient Response, Ch 2 Applied Current Step Transient (10mA – 150mA)

Figure 4. TPS7A3001 –VOUT Load Transient

5.4 +VOUT Load Transient Applied to the Positive LDO Circuit, TPS7A4901.

Figure 5 shows the load transient response – oscilloscope channel 1 – for a 10-mA to 150-mA load transient applied to +VOUT (+15-V output). Oscilloscope channel 4 shows the load current transient.



Ch 1 (+VOUT) Voltage Transient Response, Ch 2 Applied Current Step Transient (10mA – 150mA)

Figure 5. TPS7A4901 +VOUT Load Transient

6 Thermal Guidelines

Thermal management is a key component of design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

where T_J is the junction temperature, T_A is the ambient temperature, P_D is the power dissipation in the device, and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius. The maximum silicon junction temperature, T_J, must not be allowed to exceed 150°C. The layout design must make effective use of the copper trace and plane areas as thermal sinks. This prevents T_J from exceeding the absolute maximum rating under all temperature conditions and voltage conditions across the part.

The designer must carefully consider the thermal design of the PCB in the layout. It is difficult to calculate the thermal resistance for a custom layout employing some unique copper area attached to each pin of the IC. Table 1 repeats information from the Dissipation Ratings table of the TPS7A3001 and the TPS7A4901 data sheets for comparison with the thermal resistance, θ_{JA}, calculated for this EVM to show the variation in thermal resistances for given copper areas. The high-K value is determined using a standard JEDEC high-k (2s2p) board having a 3-inch × 30-inch dimension with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

Table 1. Thermal Resistance, θ_{JA}, and Maximum Power Dissipation

Board	Package	θ_{JA}	Max Dissipation (T_A = 25°C)	Max Dissipation (T_A = 70°C)
High-K	DGN	55.09°C/W	1.83 W	1.08 W
TPS7A30-49EVM-567	DGN	46.11°C/W	2.16 W	1.19 W

The thermal resistance for the TPS7A30-49EVM-567, θ_{JA}, is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the volume of copper volume connected to the package. Note that these measurements were made with only one LDO turned on.

7 Board Layout

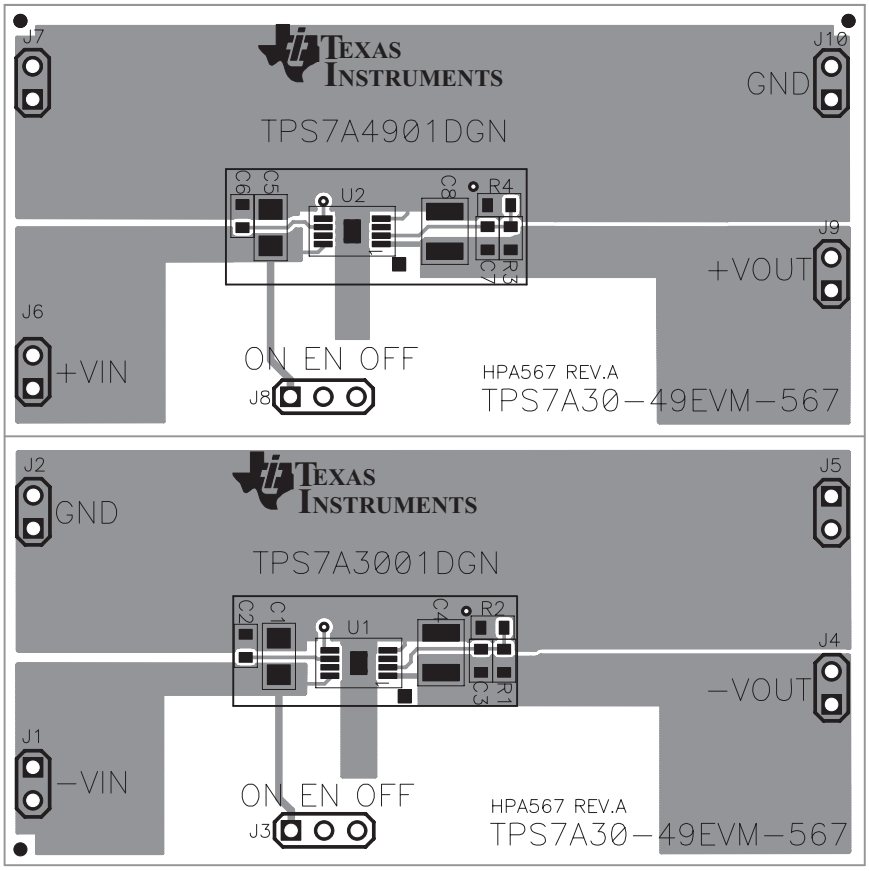


Figure 6. Assembly Layer

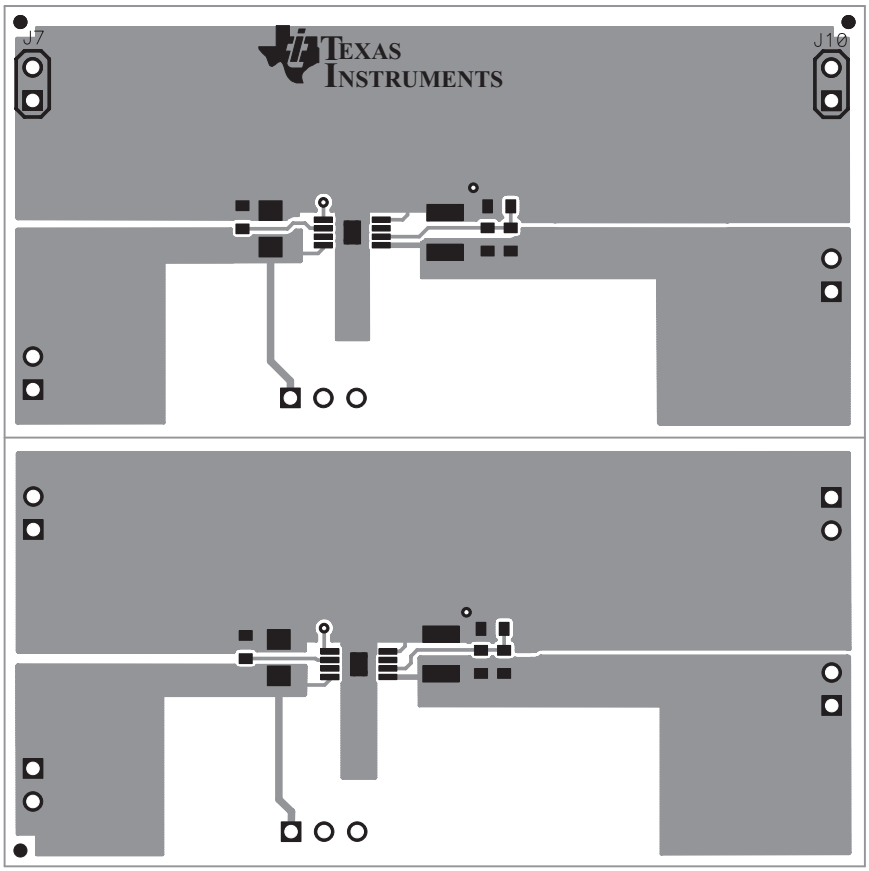


Figure 7. Top Layer Routing

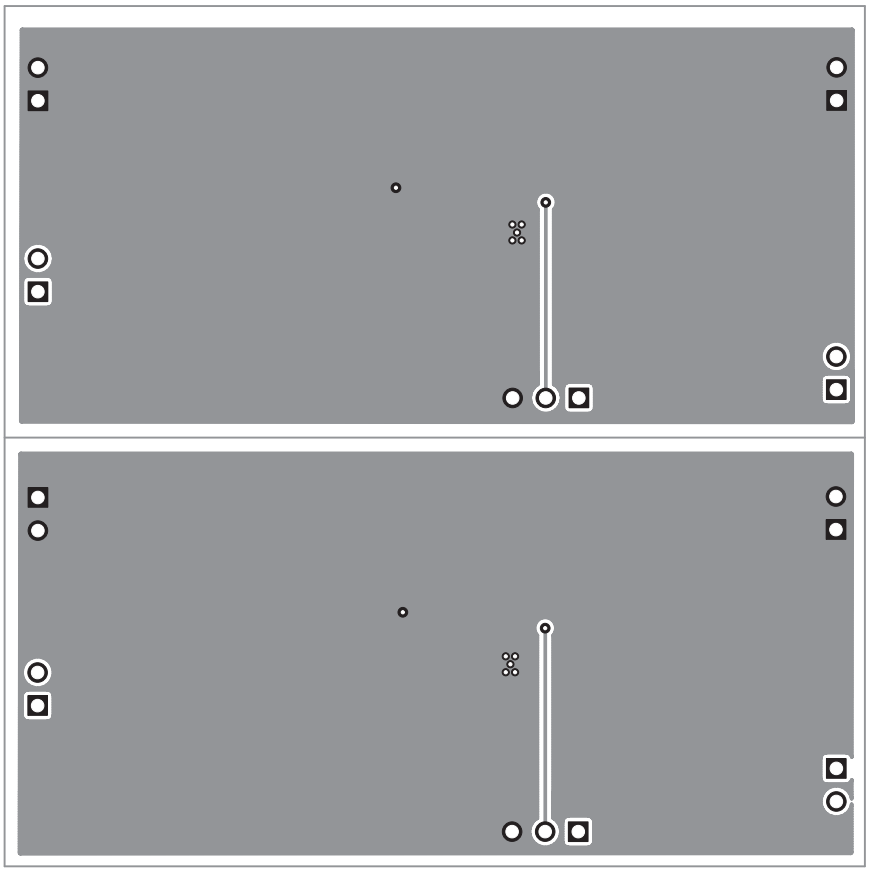


Figure 8. Bottom Layer Routing

8 Schematic and Bill of Materials

8.1 Schematic

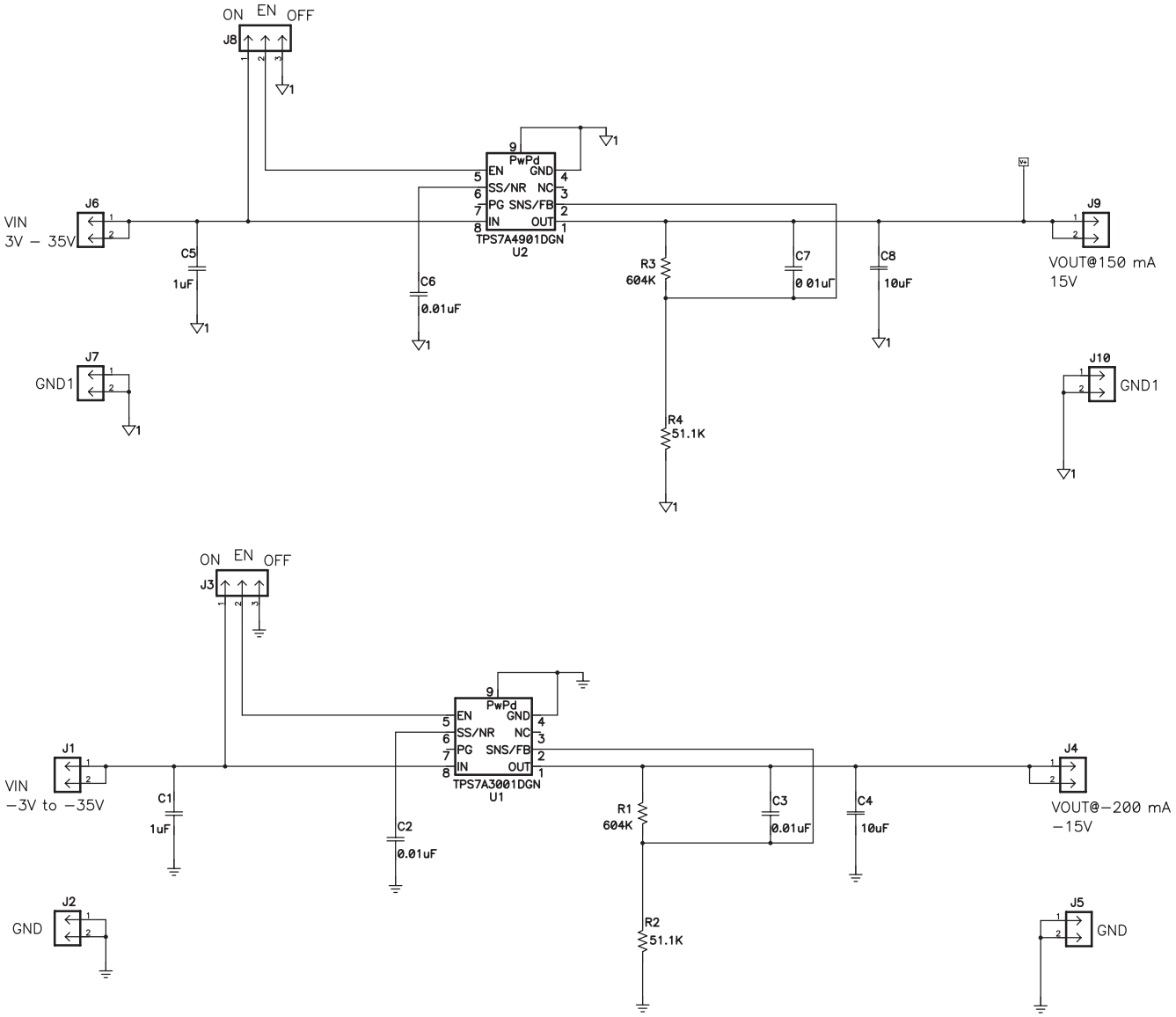


Figure 9. TPS7A30-49EVM-567 Schematic

8.2 Bill of Materials

Table 2. TPS7A30-49EVM-567 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C5	1 µF	Capacitor, Ceramic, 50V, X7R, 10%	1206	STD	STD
4	C2, C3, C6, C7	0.01 µF	Capacitor, Ceramic, Low Inductance,50V, X7R, 10%	0603	STD	STD
2	C4, C8	10 µF	Capacitor, Ceramic, 50V, X7R, 10%	1210	STD	STD
8	J1, J2, J4, J5, J6, J7, J9, J10	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
2	J3, J8	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
2	R1, R3	604K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
2	R2, R4	51.1K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	U1	TPS7A3001DGN	IC, –3V to –35V, –200mA, Ultralow Noise, High-PSRR LDO Neg Linear Reg	MSOP-8	TPS7A3001DGN	TI
1	U2	TPS7A4901DGN	IC, VIN 3V to 35V, 150mA, Ultralow Noise, High-PSRR, LDO Regulator	HTSSOP	TPS7A4901DGN	TI
1	-	HPA567A	2.6 x 2.6 x 0.062 PCB		HPA567A	Any
1		15-29-1025	Shunt, 2POs .100 Gold		15-29-1025	Molex

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. 2. These assemblies must be clean and free from flux and all contaminants.
   Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted.
   All other components can be substituted with equivalent MFG's components.
5. Do not separate PCB

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3 V to 35 V and the output voltage range of 1.212 V to 33 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100° C. The EVM is designed to operate properly with certain components above 100° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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