# USBUFxxW6

A. S. D.

EMI filter and line termination for USB upstream ports

## Application

EMI Filter and line termination for USB upstream ports on:

- USB Hubs
- PC peripherals

## Features

- Monolithic device with recommended line termination for USB upstream ports
- Integrated Rt series termination and Ct bypassing capacitors.
- Integrated ESD protection
- Small package size

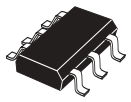
## Description

The USB specification requires upstream ports to be terminated with pull-up resistors from the D+ and D- lines to Vbus. On the implementation of USB systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of termination and EMC compatibility, the computing devices are required to be tested for ESD susceptibility.

The USBUFxxW6 provides the recommended line termination while implementing a low pass filter to limit EMI levels and providing ESD protection which exceeds IEC 61000-4-2 level 4 standard. The device is packaged in a SOT323-6L which is the smallest available lead frame package (50% smaller than the standard SOT23).

## Benefits

- EMI / RFI noise suppression
- Required line termination for USB upstream ports
- ESD protection exceeding IEC 61000-4-2 level 4
- High flexibility in the design of high density boards
- Tailored to meet USB 1.1 standard

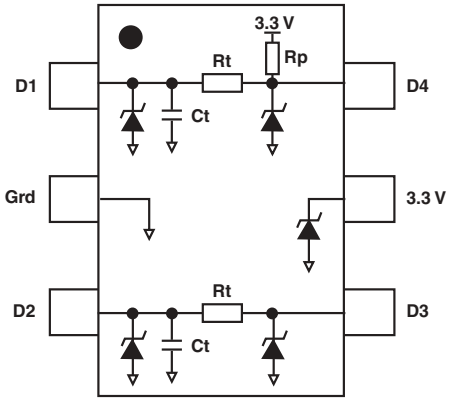


**SOTT323-6L**

**Table 1. Order Codes**

| Part Number | Marking |
|---|---|
| USBUF01W6 | UU1 |
| USBUF02W6 | UU2 |

**Figure 1. Functional diagram**




| | Rt | Rp | Ct |
|---|---|---|---|
| CODE 01 | 33 Ω | 1.5 kΩ | 47 pF |
| CODE 02 | 22 Ω | 1.5 kΩ | 47 pF |
| Tolerance | ± 10% | ± 10% | ± 20% |

### Complies with the following standards:

**IEC 61000-4-2, level 4** ± 15 kV (air discharge)
± 8 kV (contact discharge)

**MIL STD 883E, Method 3015-7**

Class 3 C = 100 pF R = 1500 Ω

3 positive strikes and 3 negative strikes (F = 1 Hz)

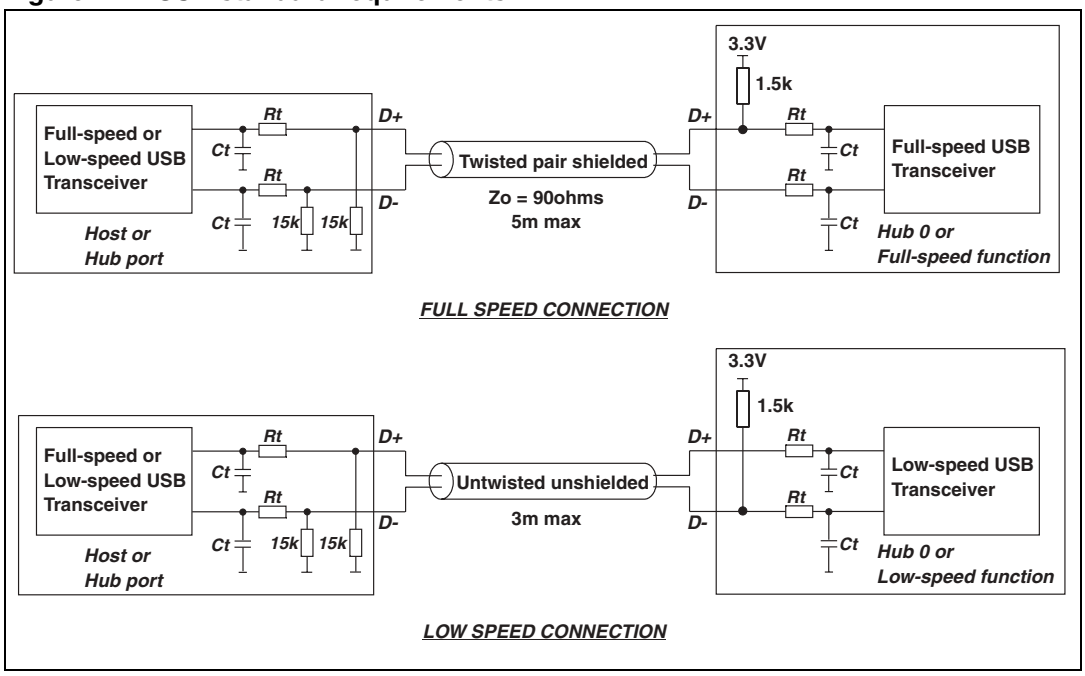
# 1 Characteristics

**Table 2. Absolute ratings ($T_{amb}$ = 25° C)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{PP}$ | ESD discharge IEC 61000-4-2, air discharge<br>ESD discharge IEC 61000-4-2, contact discharge<br>ESD discharge - MIL STD 883E - Method 3015-7 | ± 16<br>± 9<br>± 25 | kV |
| $T_j$ | Maximum junction temperature | 150 | °C |
| $T_{stg}$ | Storage temperature range | - 55 to + 150 | °C |
| $T_L$ | Lead solder temperature (10 second duration) | 260 | °C |
| $T_{op}$ | Operating temperature range | -40 to 70 | °C |
| P | Power rating per resistor | 100 | mW |

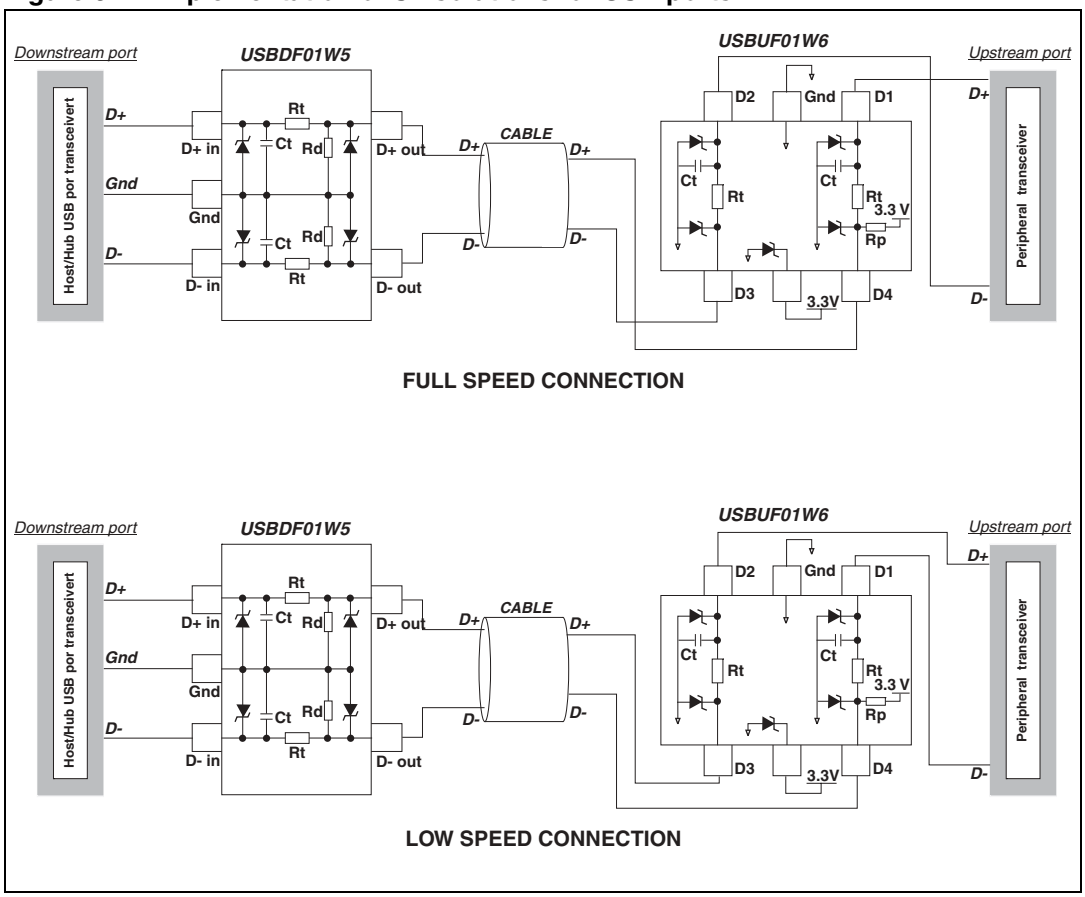
# 2 Technical information

**Figure 2. USB standard requirements**



## 2.1 Application example

**Figure 3. Implementation of ST solutions for USB ports**




## 2.2 EMI filtering

Current FCC regulations requires that class B computing devices meet specified maximum levels for both radiated and conducted EMI.

- Radiated EMI covers the frequency range from 30 MHz to 1 GHz.
- Conducted EMI covers the 450 kHz to 30 MHz range.

For the types of devices utilizing the USB, the most difficult test to pass is usually the radiated EMI test. For this reason the USBUFxxW6 device is aiming to minimize radiated EMI.

The differential signal (D+ and D-) of the USB does not contribute significantly to radiated or conducted EMI because the magnetic field of both conductors cancels each other.

The inside of the PC environment is very noisy and designers must minimize noise coupling from the different sources. D+ and D-must not be routed near high speed lines (clocks spikes).

Induced common mode noise can be minimized by running pairs of USB signals parallel to each other and running grounded guard trace on each side of the signal pair from the USB controller to the USBUF device. If possible, locate the USBUF device physically near the

USB connectors. Distance between the USB controller and the USB connector must be minimized.

The 47 pF ($C_t$) capacitors are used to bypass high frequency energy to ground and for edge control, and are placed between the driver chip and the series termination resistors (Rt). Both Ct and Rt should be placed as close to the driver chip as is practicable.

The USBUFxxW6 ensures a filtering protection against ElectroMagnetic and RadioFrequency Interferences thanks to its low-pass filter structure. This filter is characterized by the following parameters:

- cut-off frequency
- Insertion loss
- high frequency rejection.

**Figure 4. USBUFxxW6 typical attenuation**

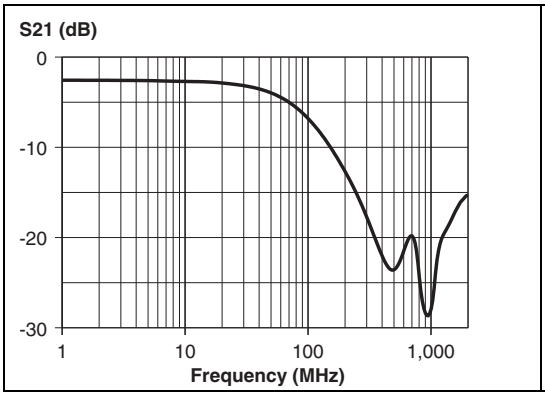
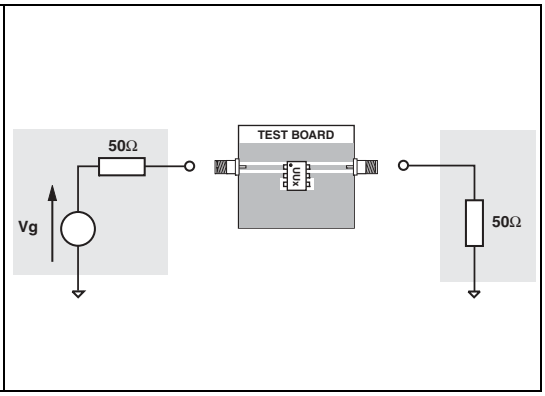



**Figure 5. Measurement configuration**




## 2.3 ESD PROTECTION

In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in the IEC 61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remains operational without user intervention.

The USBUFxxW6 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at:

$$V_{cl} = V_{BR} + R_d \cdot I_{PP}$$

This protection function is splitted in 2 stages. As shown in figure 6, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor Rt. Such a configuration makes the output voltage very low at the output.

**Figure 6. USBUFxxW6 ESD clamping behavior**

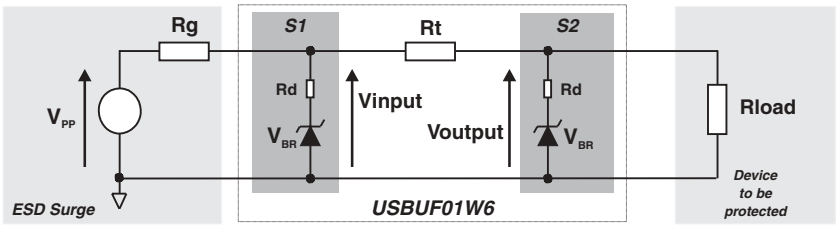
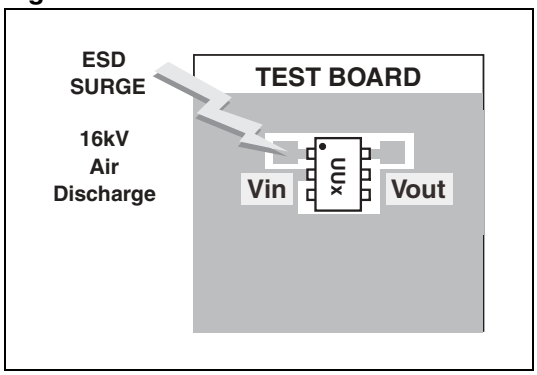



**Figure 7. Measurement board**




To have a good approximation of the remaining voltages at both Vin and Vout stages, we give the typical dynamical resistance value Rd. By taking into account these following hypothesis: $R_t > R_d$, $R_g > R_d$ and $R_{load} > R_d$, it gives these formulas:

$$Vinput = \frac{R_g \cdot V_{BR} + R_d \cdot V_g}{R_g}$$

$$Vouput = \frac{R_t \cdot V_{BR} + R_d \cdot Vinput}{R_t}$$

The results of the calculation done for $V_g$ = 8 kV, $R_g$ = 330 Ω (IEC 61000-4-2 standard), $V_{BR}$ = 7 V (typ.) and $R_d$ = 1 Ω (typ.) give:

Vinput = 31.2 V

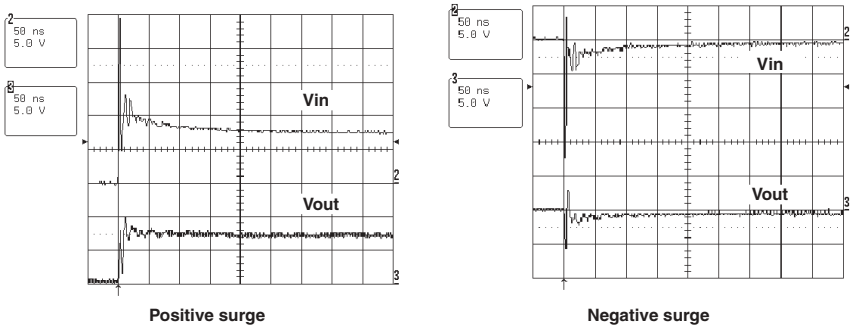
Voutput = 7.95 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the $V_{input}$ side. This parasitic effect is not present at the $V_{output}$ side due the low current involved after the resistance $R_t$.

The measurements done hereafter show very clearly (figure 8) the high efficiency of the ESD protection:

- no influence of the parasitic inductances on Voutput stage
- Voutput clamping voltage very close to $V_{BR}$ (breakdown voltage) in the positive way and - $V_F$ (forward voltage) in the negative way

**Figure 8. Remaining voltage at both stages S1 (Vinput) and S2 (Voutput) during ESD surge**



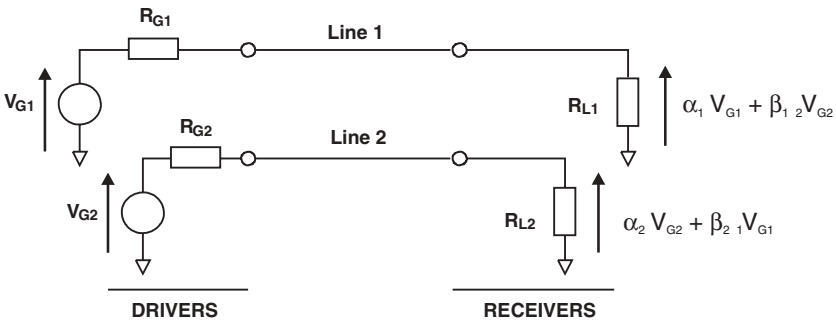

Please note that the USBUFxxW6 is not only acting for positive ESD surges but also for negative ones. For these kinds of disturbances it clamps close to ground voltage as shown in *Figure 8.* (negative surge.

## 2.4 Latch-up phenomena

The early ageing and destruction of IC's is often due to latch-up phenomenon which is mainly induced by dV/dt. Thanks to its structure, the USBUFxxW6 provides a high immunity to latch-up phenomenon by smoothing very fast edges.

## 2.5 Crosstalk behavior

**Figure 9. Crosstalk phenomenon.**




The crosstalk phenomenon is due to the coupling between 2 lines. The coupling factor ($\beta_{12}$ or $\beta_{21}$) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load $R_{L2}$ is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the $V_{G1}$ signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

**Figure 10. Figure 10: Analog crosstalk measurements**

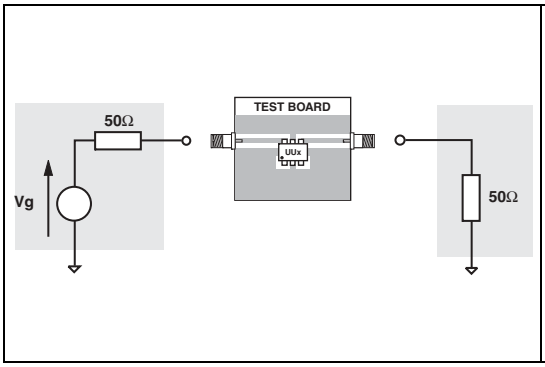



**Figure 11. Typical analog crosstalk results**

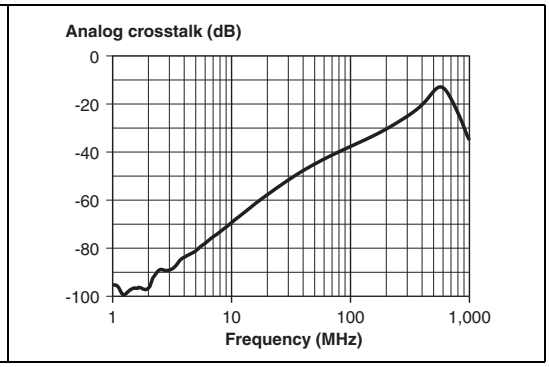



*Figure 10.* gives the measurement circuit for the analog crosstalk application. In *Figure 11.*, the curve shows the effect of the D+ cell on the D-cell. In usual frequency range of analog signals (up to 100 MHz) the effect on disturbed line is less than -37 db.

**Figure 12. Digital crosstalk measurements configuration**

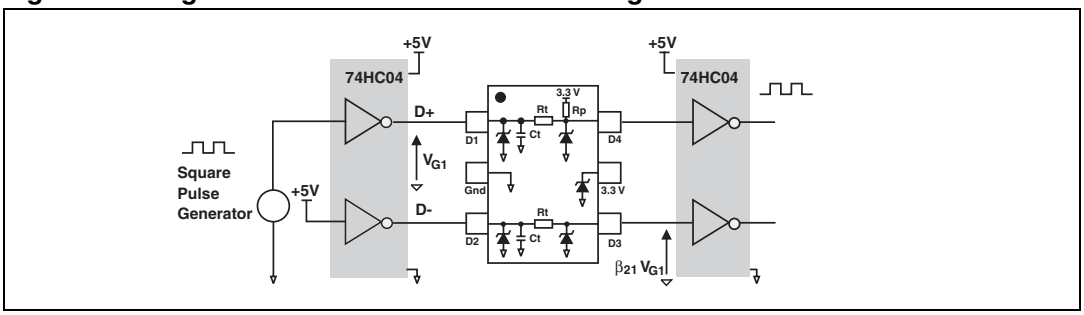



*Figure 12.* shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

**Figure 13. Digital crosstalk results**

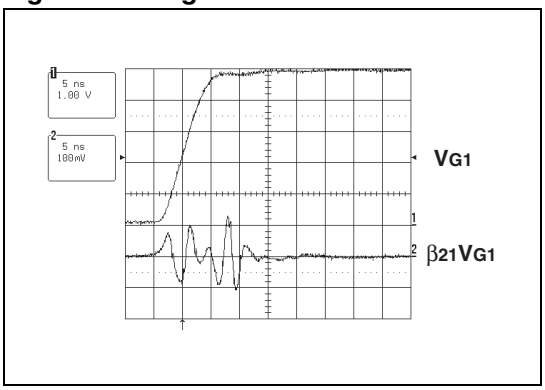



*Figure 13.* shows, with a signal from 0 to 5 V and rise time of few ns, the impact on the disturbed line is less than 250 mV peak to peak. No data disturbance was noted on the other line.The measurements performed with falling edges gives an impact within the same range.

## 2.6 Transition times

This low pass filter has been designed in order to meet the USB 1.1 standard requirements that implies the signal edges are maintained within the 4 -20 ns stipulated USB specification limits. To verify this point, we have measured the rise time of VD+ voltage with and without the USBUFxxW6 device.

**Figure 14. Typical rise and fall times: measurement configuration**

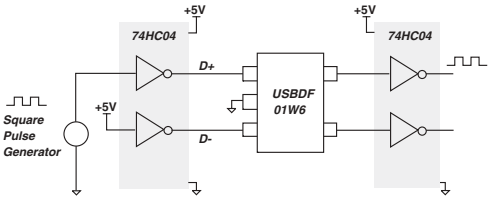



**Figure 15. Typical rise times with and without protection device**

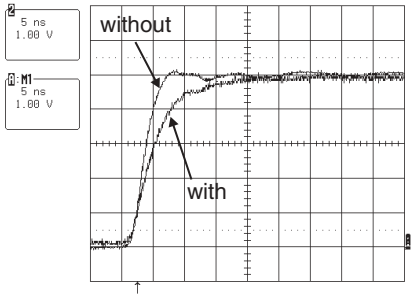



*Figure 14.* shows the circuit used to perform measurements of the transition times. In *Figure 15.*, we see the results of such measurements:

trise = 3.8 ns driver alone

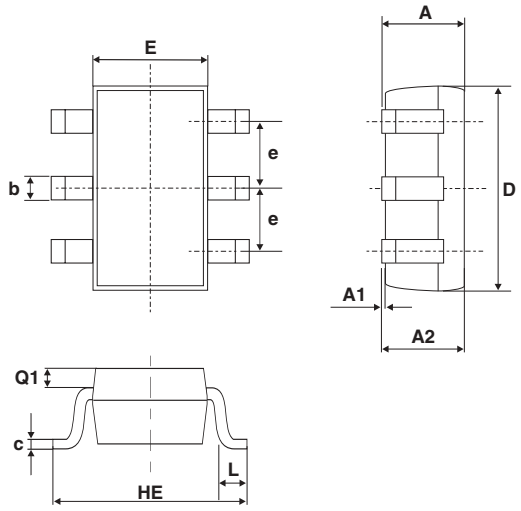
trise = 7.8 ns with protection device

The adding of the protection device causes the rise time increase of roughly 4ns.

*Note: Rise time has been measured between 10% and 90% of the signal (resp. 90% and 10%)*

# 3 Packaging information

**Table 3. SOT323-6L Package Mechanical Data**




| REF. | DIMENSIONS | | | |
|---|---|---|---|---|
| | Millimeters | | Inches | |
| | Min. | Max. | Min. | Max. |
| A | 0.8 | 1.1 | 0.031 | 0.043 |
| A1 | 0 | 0.1 | 0 | 0.004 |
| A2 | 0.8 | 1 | 0.031 | 0.039 |
| b | 0.15 | 0.3 | 0.006 | 0.012 |
| c | 0.1 | 0.18 | 0.004 | 0.007 |
| D | 1.8 | 2.2 | 0.071 | 0.086 |
| E | 1.15 | 1.35 | 0.045 | 0.053 |
| e | 0.65 Typ. | | 0.025 Typ. | |
| HE | 1.8 | 2.4 | 0.071 | 0.094 |
| L | 0.1 | 0.4 | 0.004 | 0.016 |
| Q1 | 0.1 | 0.4 | 0.004 | 0.016 |

**Figure 16. Recommeneded footprint (dimensions in mm)**

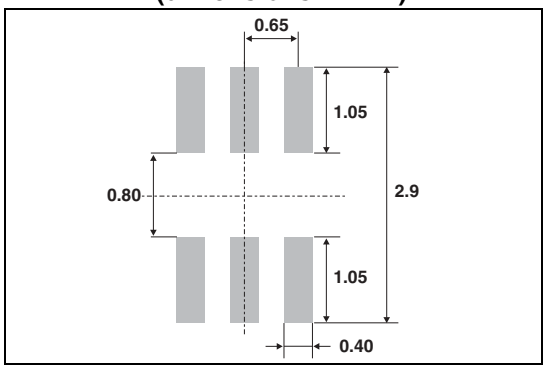



**Table 4. Mechanical specifications**

| | |
|---|---|
| Lead plating | Tin-lead |
| Lead plating thickness | 5 m min<br>25 m max |
| Lead material | Sn / Pb<br>(70% to 90%Sn) |
| Lead coplanarity | 10 m max |
| Body material | Molded epoxt |
| Flammability | UL94V-0 |

# 4 Ordering Information

| Ordering code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| USBUF01W6 | UU1 | SOT323-6L | 5.4 mg | 3000 | Tape & reel |
| USBUF02W6 | UU2 | SOT323-6L | 5.4 mg | 3000 | Tape & reel |

# 5 Revision History

| Date | Revision | Description of Changes |
|---|---|---|
| Mar-2002 | 3A | Last update. |
| Feb-2005 | 4 | Layout update. No content change. |
| 28-Feb-2006 | 5 | Operating temperature range updated to -40 to 70° C.<br>Layout updated to current standard. |

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