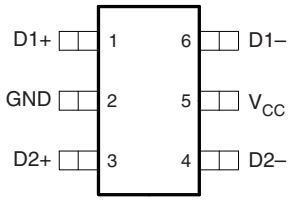
4-CHANNEL ESD SOLUTION FOR HIGH-SPEED DIFFERENTIAL INTERFACE

Check for Samples: TPD4S009, TPD4S010

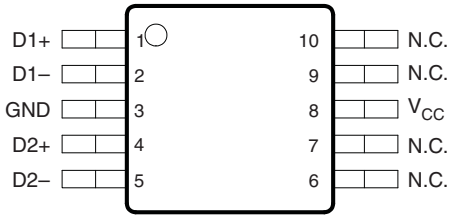
FEATURES

- **Supports High-Speed Differential Data Rates (3-dB Bandwidth > 4 GHz)**
- **Ultra-low Matching Capacitance Between Differential Signal Pairs**
- **Low 0.8-pF Line Capacitance for Each Data Line to GND**
- **Flow-Through Single-in-Line Pin Mapping for High-Speed Lines Ensures No Additional Board Layout Burden While Placing ESD Protection Chip Near Connector**
- **IEC 61000-4-2 (Level 4) System-Level ESD Compliance**
- **2.5-A Peak Pulse Current (8/20-µs Pulse)**
- **I_{off} Feature for the TPD4S009**
- **Industrial Temperature Range: –40°C to 85°C**
- **Space-Saving Package Options**

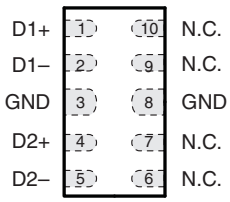
TPD4S009...DBV OR DCK PACKAGE (TOP VIEW)



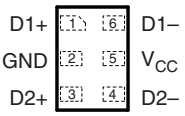
TPD4S009...DGS PACKAGE (TOP VIEW)



TPD4S010...DQA PACKAGE (TOP VIEW)



TPD4S009...DRY PACKAGE (TOP VIEW)



DESCRIPTION

The TPD4S009 and TPD4S010 provide system level electrostatic discharge (ESD) solution for high-speed differential lines. These devices offer four ESD clamp circuits for dual pair differential lines. The TPD4S009 offers an optional V_{CC} supply pin which can be connected to system supply plane. There is a blocking diode at the V_{CC} pin to enable the Ioff feature for the TPD4S009. The TPD4S009 can handle live signal at the D+, D- pins when the V_{CC} pin is connected to zero volt. The V_{CC} pin allows all the internal circuit nodes of the TPD4S009 to be at known potential during start up time. However, connecting the optional V_{CC} pin to board supply plane doesn't affect the system level ESD performance of the TPD4S009. The TPD4S010 does not offer the V_{CC} pin.

The TPD4S009 is offered in DBV, DCK, DGS, and DRY packages. The TPDS4010 is offered in DQA package. The TPD4S009DRYR is the most space saving package option available for dual pair high-speed differential lines. The TPD4S009DGSR and TPD4S010DQAR offer flow-through board layout option to reduce signal glitches due to mismatch between the D+ and D- signal pair routing.

The monolithic silicon technology allows matching between the differential signal pairs. The excellent matching between the differential pair signal lines (0.05-pF line-line capacitance for the TPD4S009DRY) enables this device to operate at high-speed differential data rates (3-dB bandwidth > 4 GHz). The TPD4S009 and TPD4S010 are suitable for high-speed differential applications, such as high-definition multimedia interface (HDMI), low-voltage differential signaling (LVDS), serial advanced technology attachment (SATA), Ethernet, 1394 (FireWire®), etc.

TPD4S009/TPD4S010 comply with IEC 61000-4-2 (Level 4) ESD.

TPD4S009/TPD4S010 are characterized for operation over the ambient air temperature range of –40°C to 85°C.

CIRCUIT DIAGRAMS

Figure 1. TPD4S009

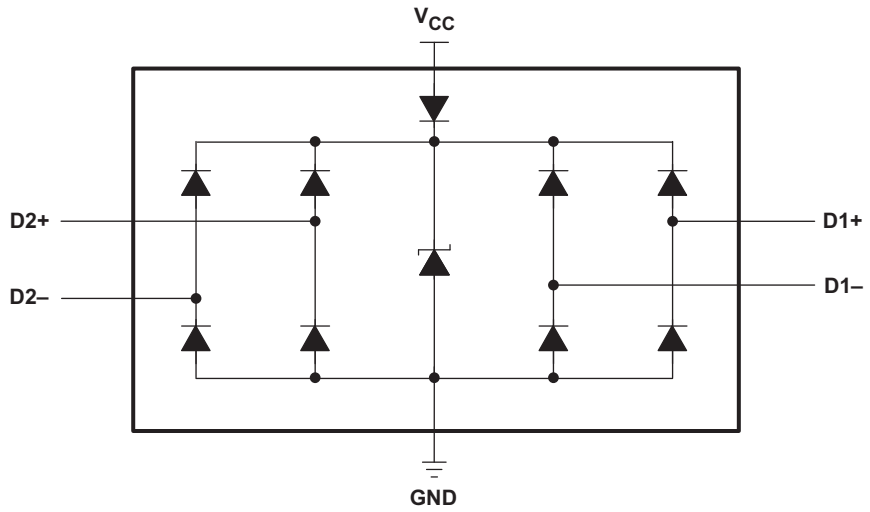
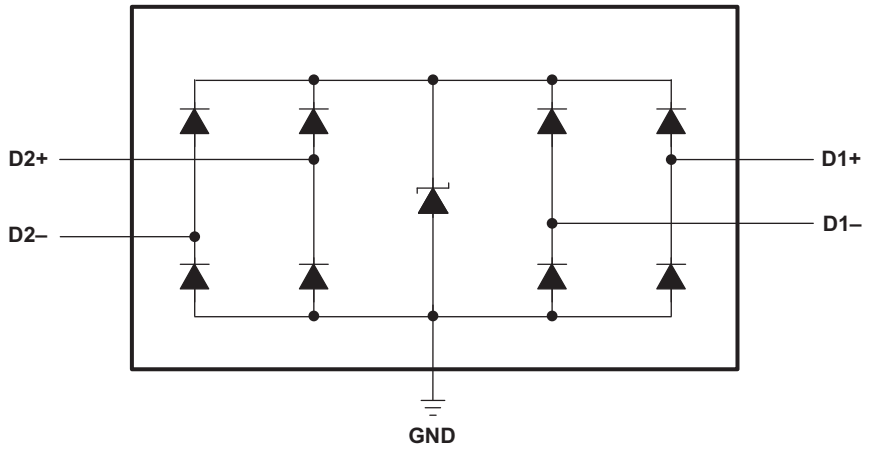


Figure 2. TPD4S010



TERMINAL FUNCTIONS

DBV, DCK, OR DRY PIN NO.	DGS PIN NO.	DQA PIN NO.	NAME	I/O	DESCRIPTION
1, 6, 3, 4	1, 2, 4, 5	1, 2, 4, 5	D1+, D1–, D2+, D2–	ESD port	High-speed ESD clamp provides ESD protection to the high-speed differential data lines.
2	3	3, 8	GND	GND	Ground
–	6, 7, 9, 10	6, 7, 9, 10	N.C.	–	Not internally connected
5	8	–	V_{CC}	Power	Supply

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range for TPD4S009	–0.3	6	V
V_{IO}	IO signal voltage range	0	V_{CC}	V
T_{stg}	Storage temperature range	–65	125	°C
T_A	Characterized free-air operating temperature range	–40	85	°C
	Lead temperature, 1.6 mm (1/16 in) from case for 10 s)		260	°C
	IEC 61000-4-2 Contact Discharge		±8	kV
	IEC 61000-4-2 Air-Gap Discharge		±9	kV
	Peak pulse power (t_p = 8/20 µs)		25	W
	Peak pulse current (t_p = 8/20 µs)		2.5	A

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse standoff voltage	Any IO pin to ground				5.5	V
V_{BR}	Breakdown voltage	I_{IO} = 1 mA	Any IO pin to ground	9			V
I_{IO}	IO port current	V_{IO} = 3.3 V, V_{CC} = 5 V	Any IO pin		0.01	0.1	µA
I_{off}	Current from IO port to supply pins	V_{IO} = 3.3 V, V_{CC} = 5 V	Any IO pin		0.01	0.1	µA
V_D	Diode forward voltage	I_{IO} = 8 mA	Lower clamp diode	0.6	0.8	0.95	V
R_{DYN}	Dynamic resistance	I = 1 A	Any IO pin		1.1		Ω
C_{IO}	IO capacitance	V_{CC} = 5 V, V_{IO} = 2.5 V	Any IO pin		0.8		pF
I_{CC}	Operating supply current	V_{IO} = Open, V_{CC} = 5 V	V_{CC} pin		0.1	1	µA

TYPICAL CHARACTERISTICS

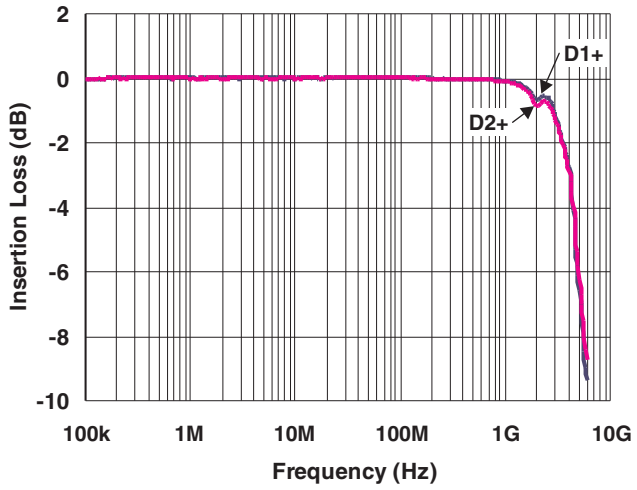


Figure 3. Insertion Loss S21 – I/O to GND

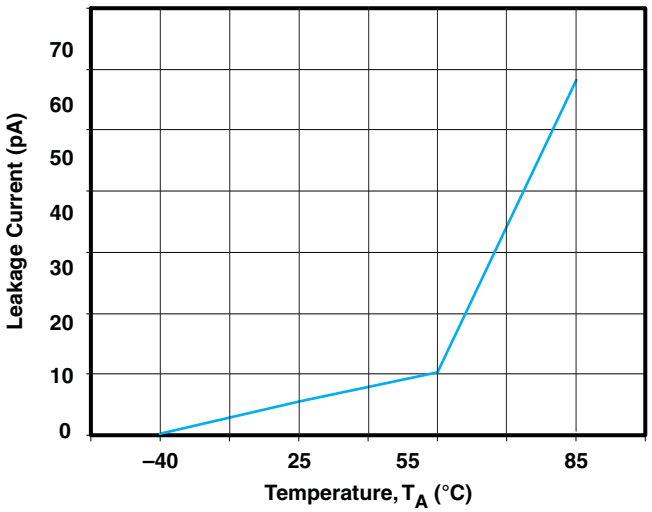


Figure 4. Leakage Current vs Temperature (V_{IO} = 2.5 V)

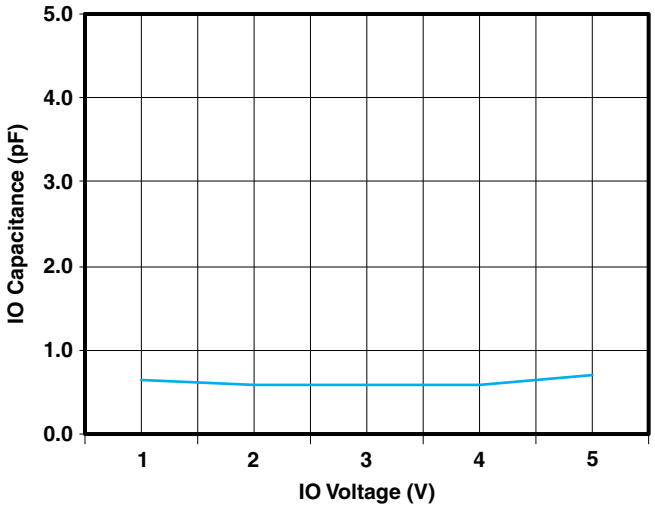


Figure 5. IO Capacitance vs Input Voltage (V_{CC} = 5 V)

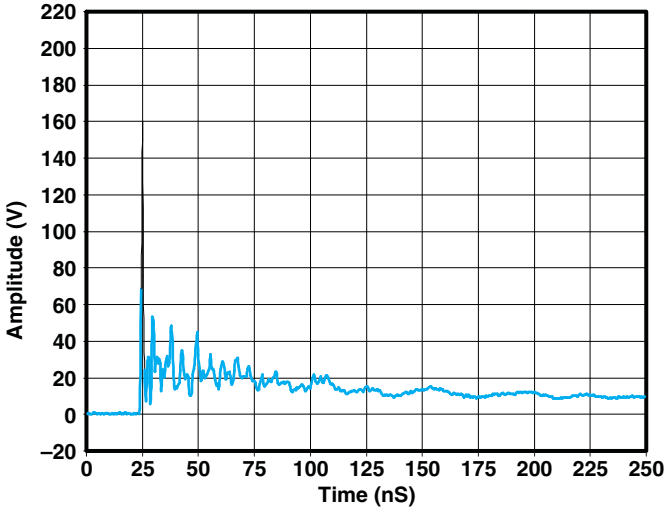


Figure 6. IEC Clamping Waveforms
(8-kV Contact, Average of Ten Waveforms)

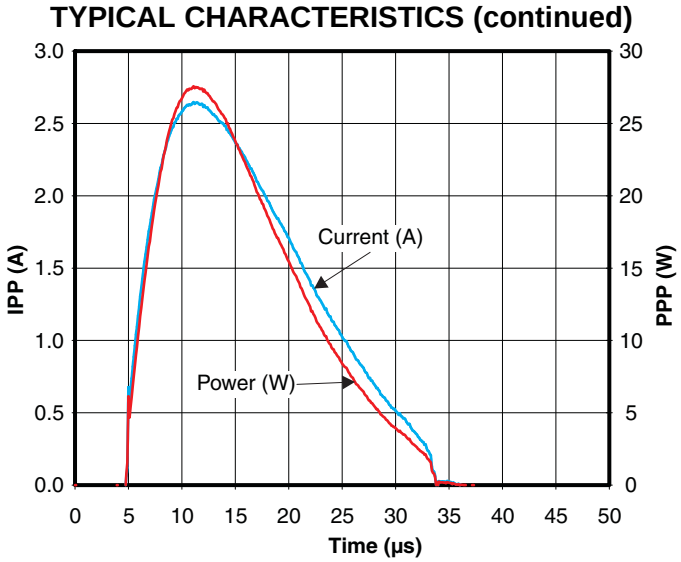


Figure 7. Pulse Waveform (8/20 µs Pulse)

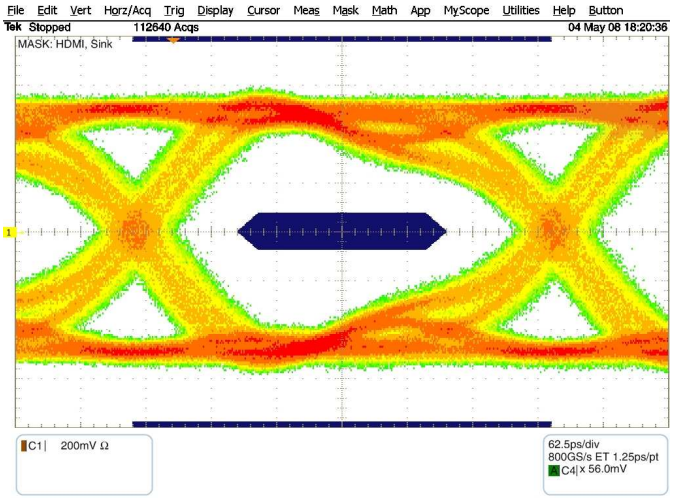


Figure 8. Eye Diagram Without TPD4S009

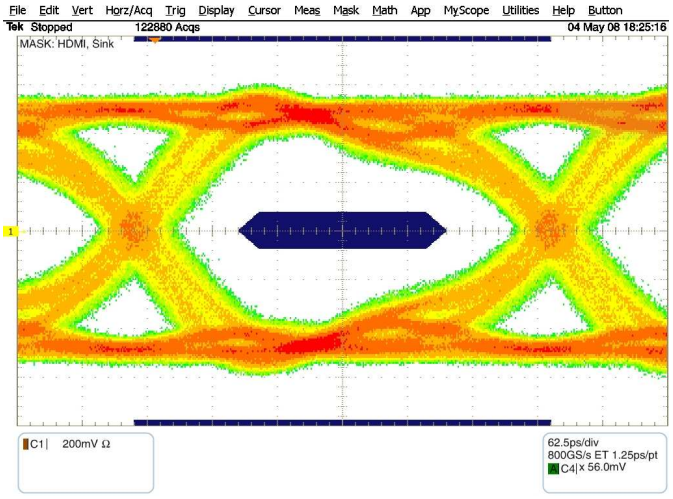


Figure 9. Eye Diagram With TPD4S009

REVISION HISTORY

Changes from Revision E (December 2011) to Revision F	Page
• Removed Ordering Information table.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4S009DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	(NFJ ~ NFJK)	Samples
TPD4S009DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	(NFJ ~ NFJK)	Samples
TPD4S009DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3HR	Samples
TPD4S009DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3HR	Samples
TPD4S009DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(3HQ ~ 3HR)	Samples
TPD4S009DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3H	Samples
TPD4S010DQAR	ACTIVE	USON	DQA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(4U7 ~ 4UO ~ 4UR)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

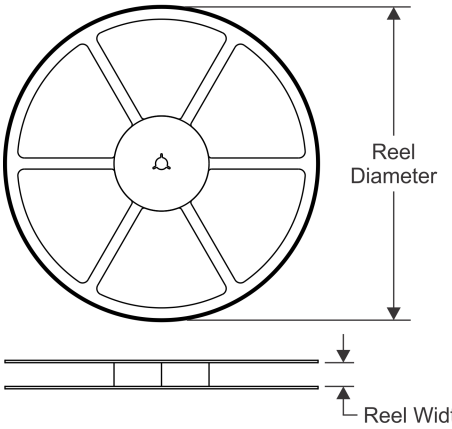
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

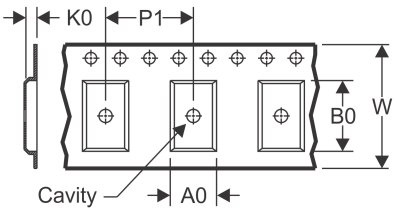
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

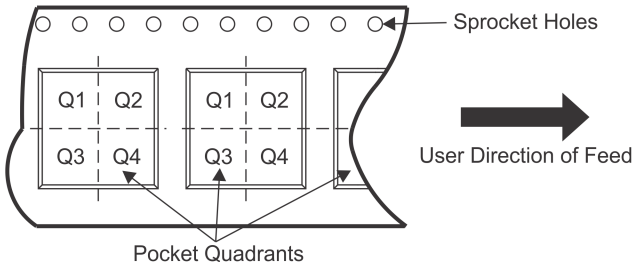


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

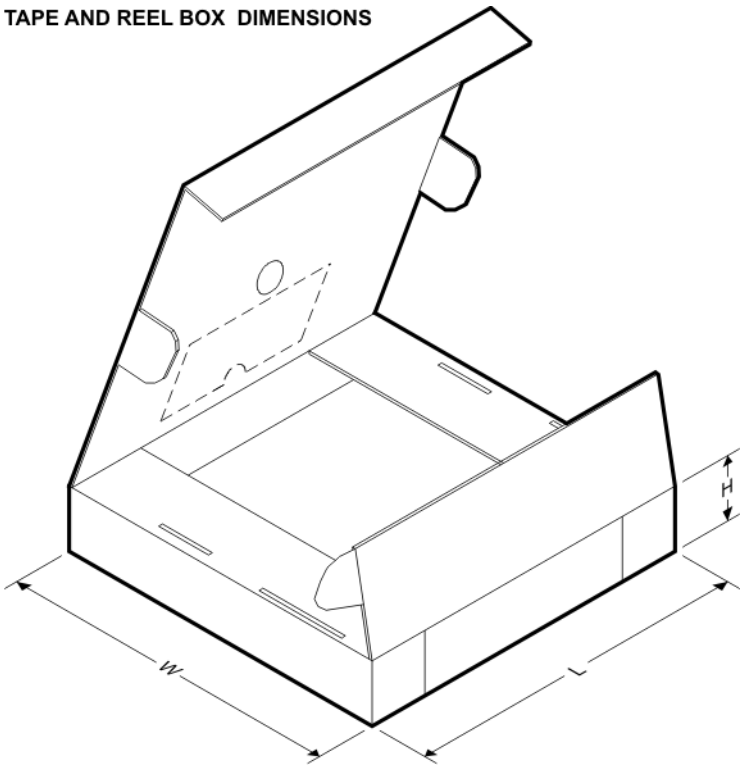
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S009DBVR	SOT-23	DBV	6	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
TPD4S009DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPD4S009DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPD4S009DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
TPD4S010DQAR	USON	DQA	10	3000	180.0	9.5	1.23	2.7	0.7	4.0	8.0	Q1
TPD4S010DQAR	USON	DQA	10	3000	180.0	8.4	1.3	2.83	0.65	4.0	8.0	Q1

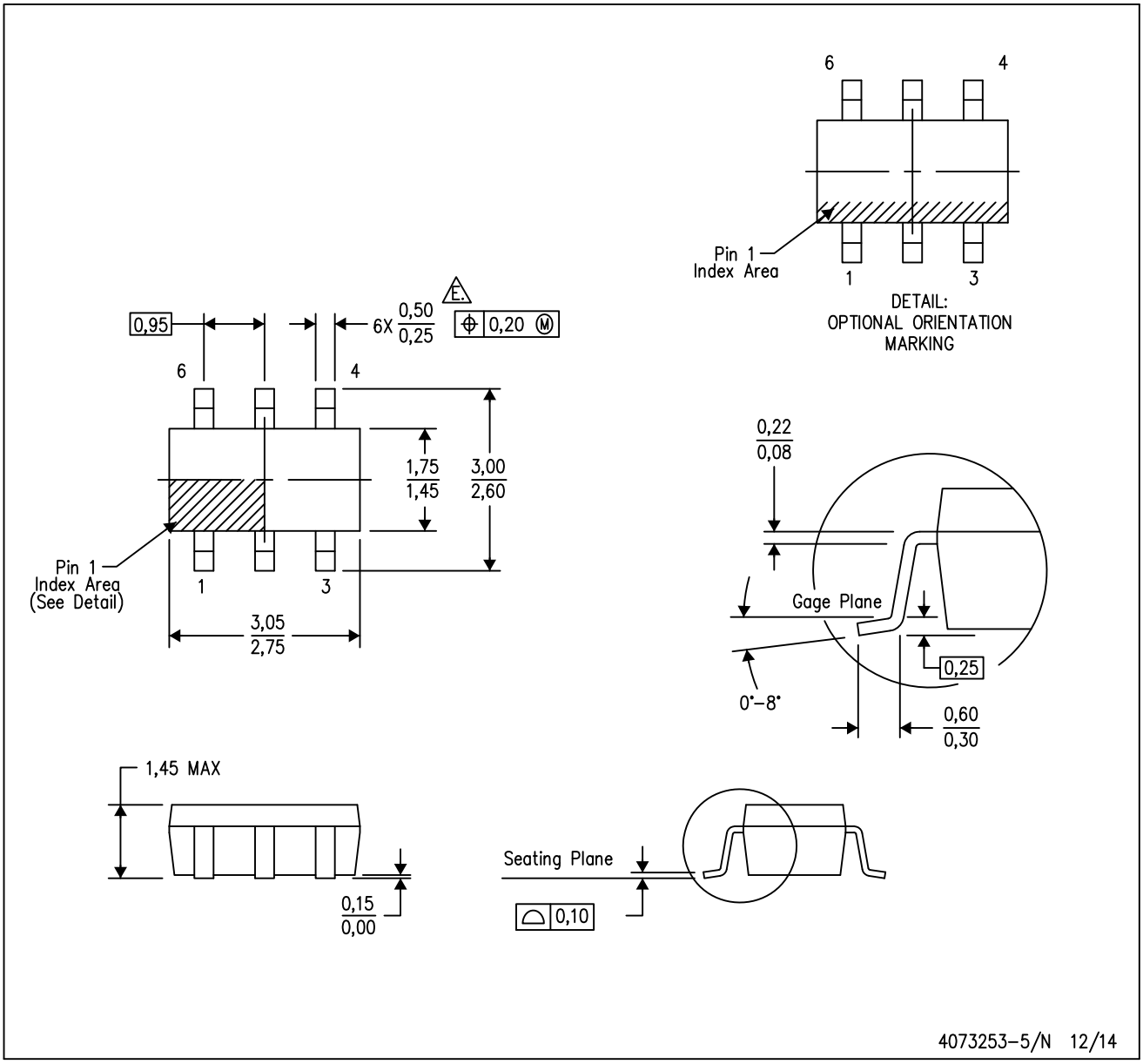
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

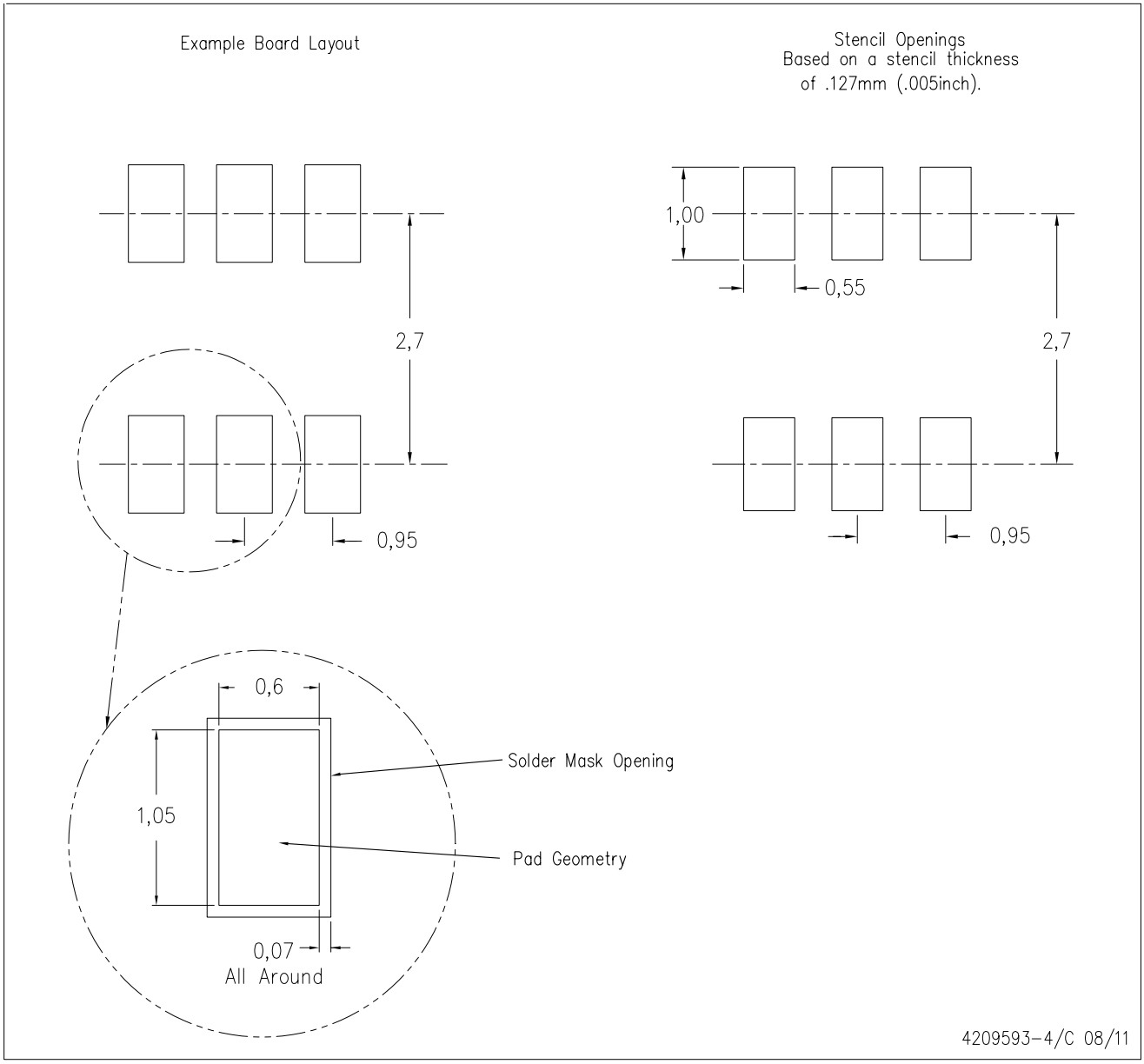
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S009DBVR	SOT-23	DBV	6	3000	205.0	200.0	33.0
TPD4S009DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPD4S009DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TPD4S009DRYR	SON	DRY	6	5000	203.0	203.0	35.0
TPD4S010DQAR	USON	DQA	10	3000	184.0	184.0	19.0
TPD4S010DQAR	USON	DQA	10	3000	202.0	201.0	28.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



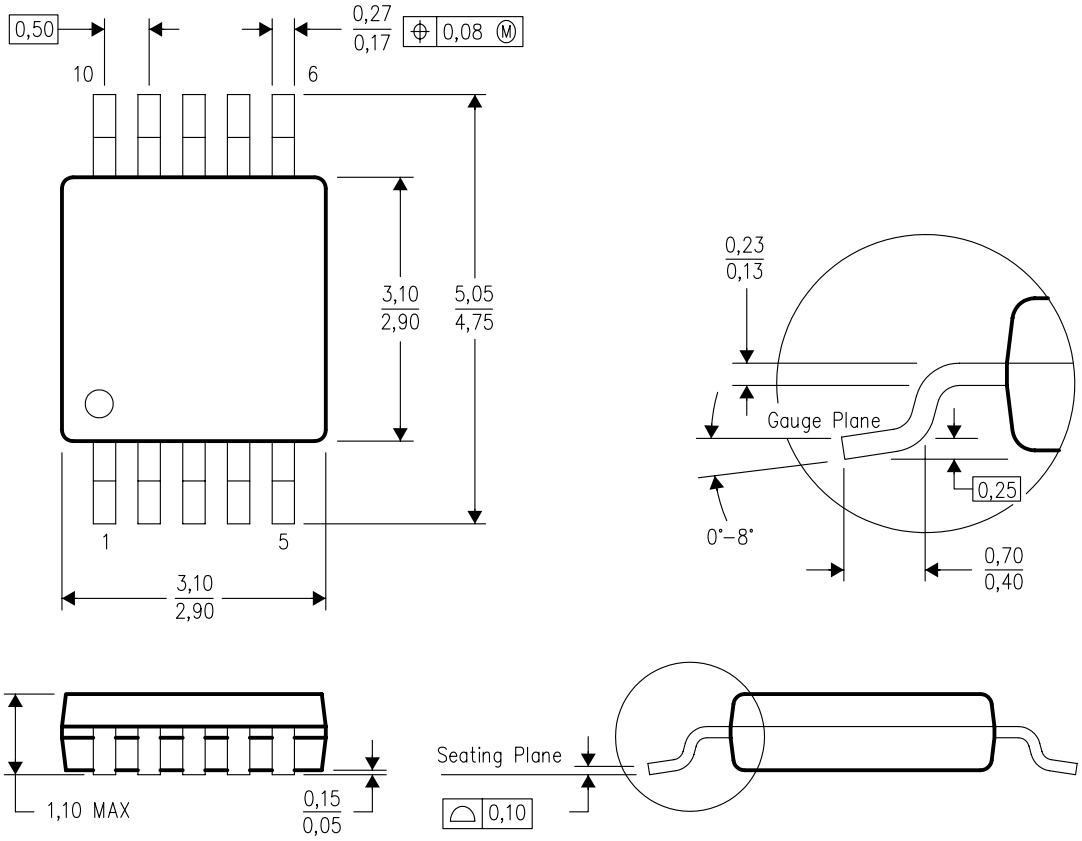
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



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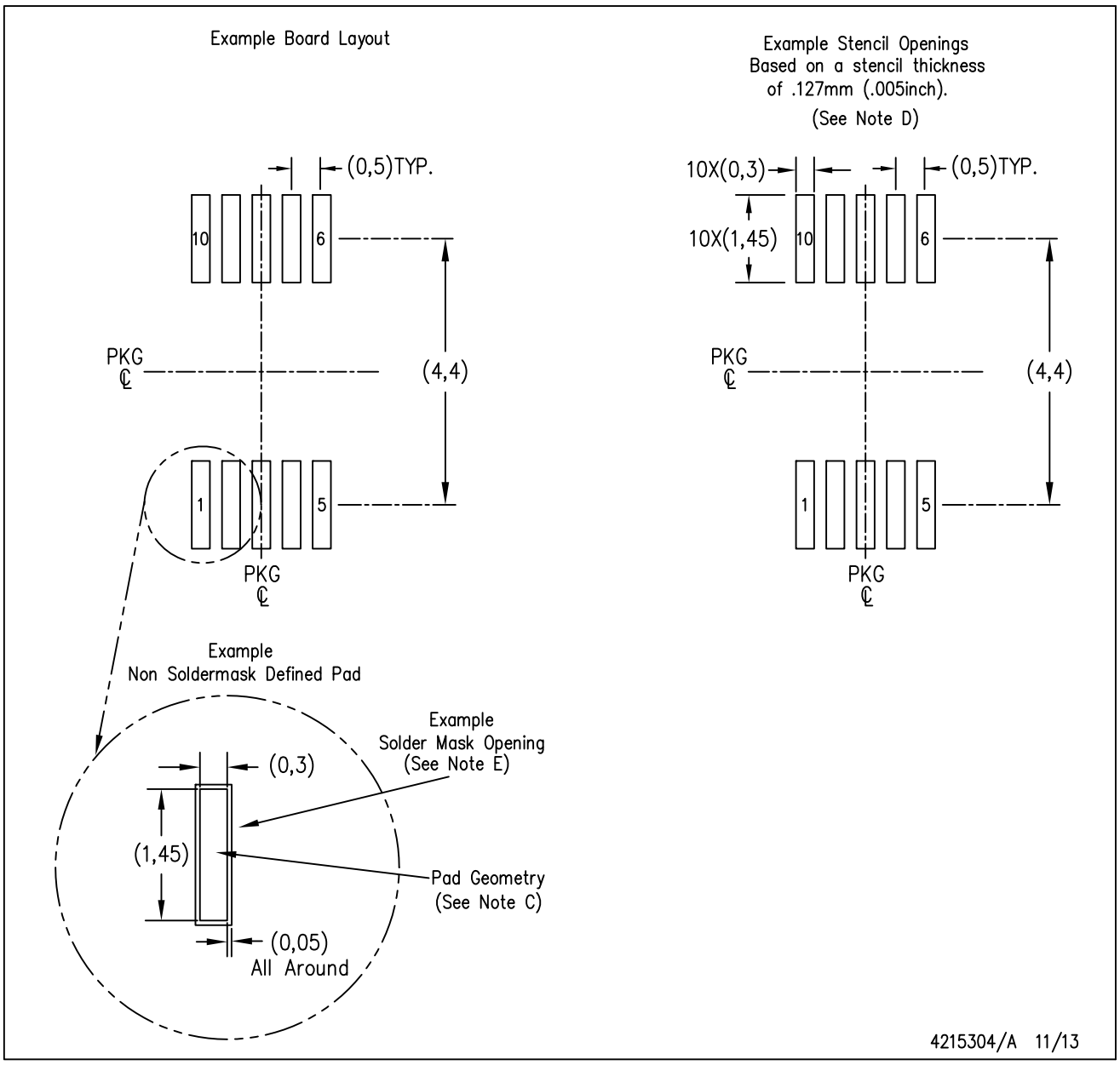
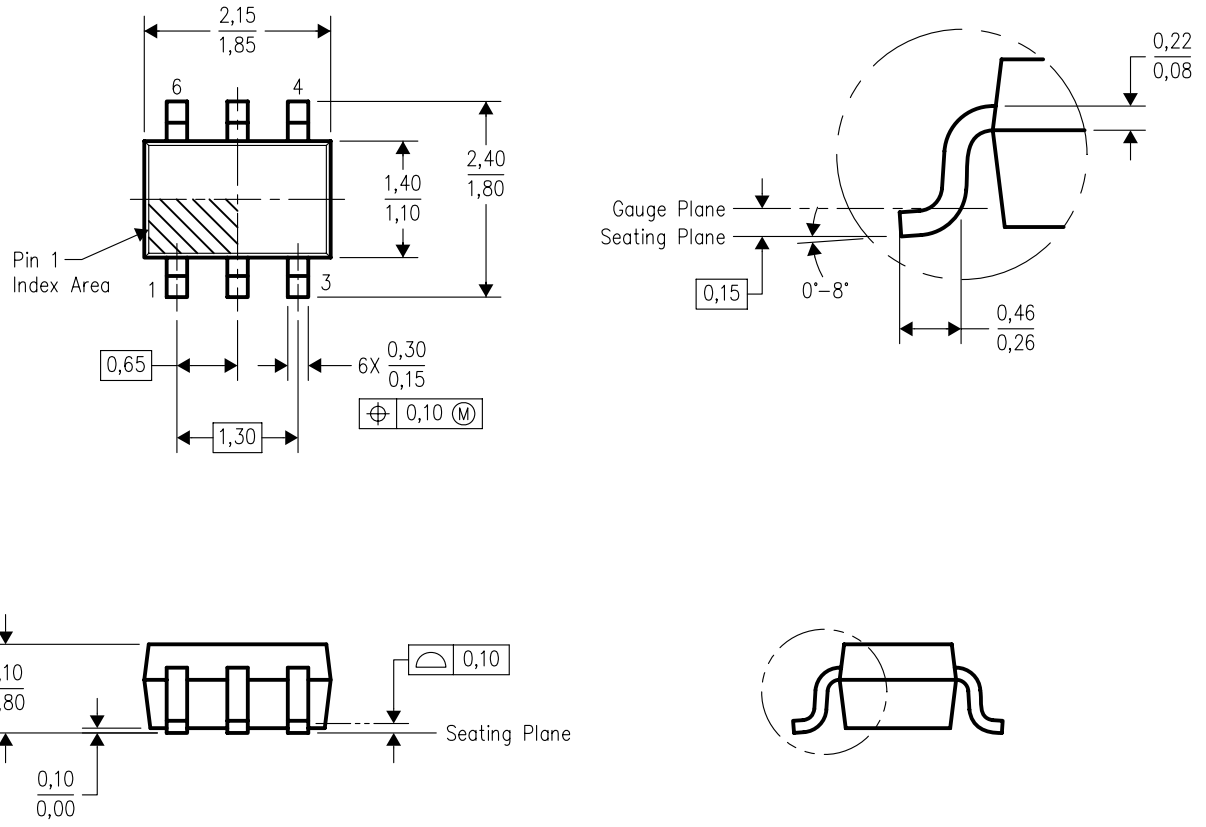
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

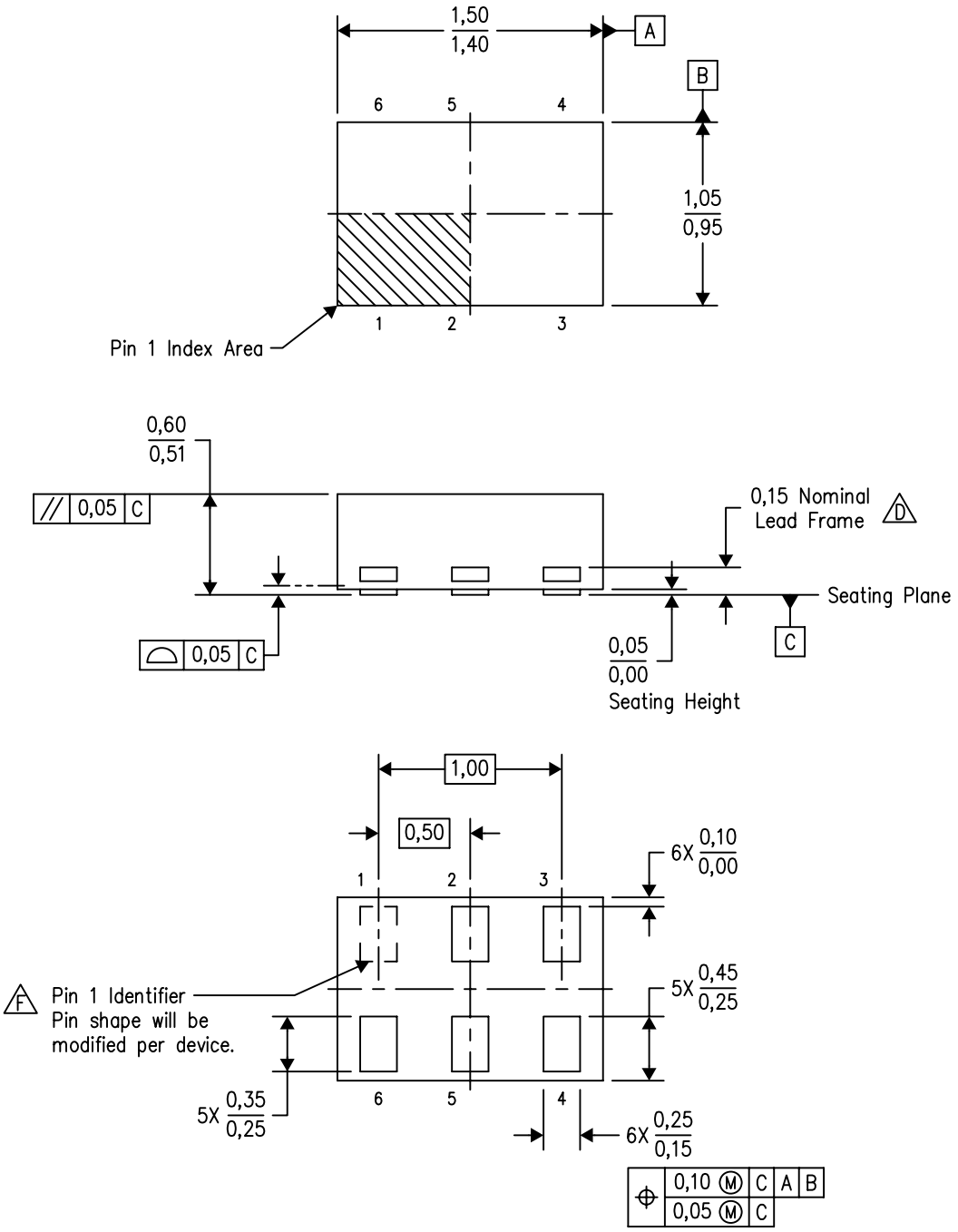
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

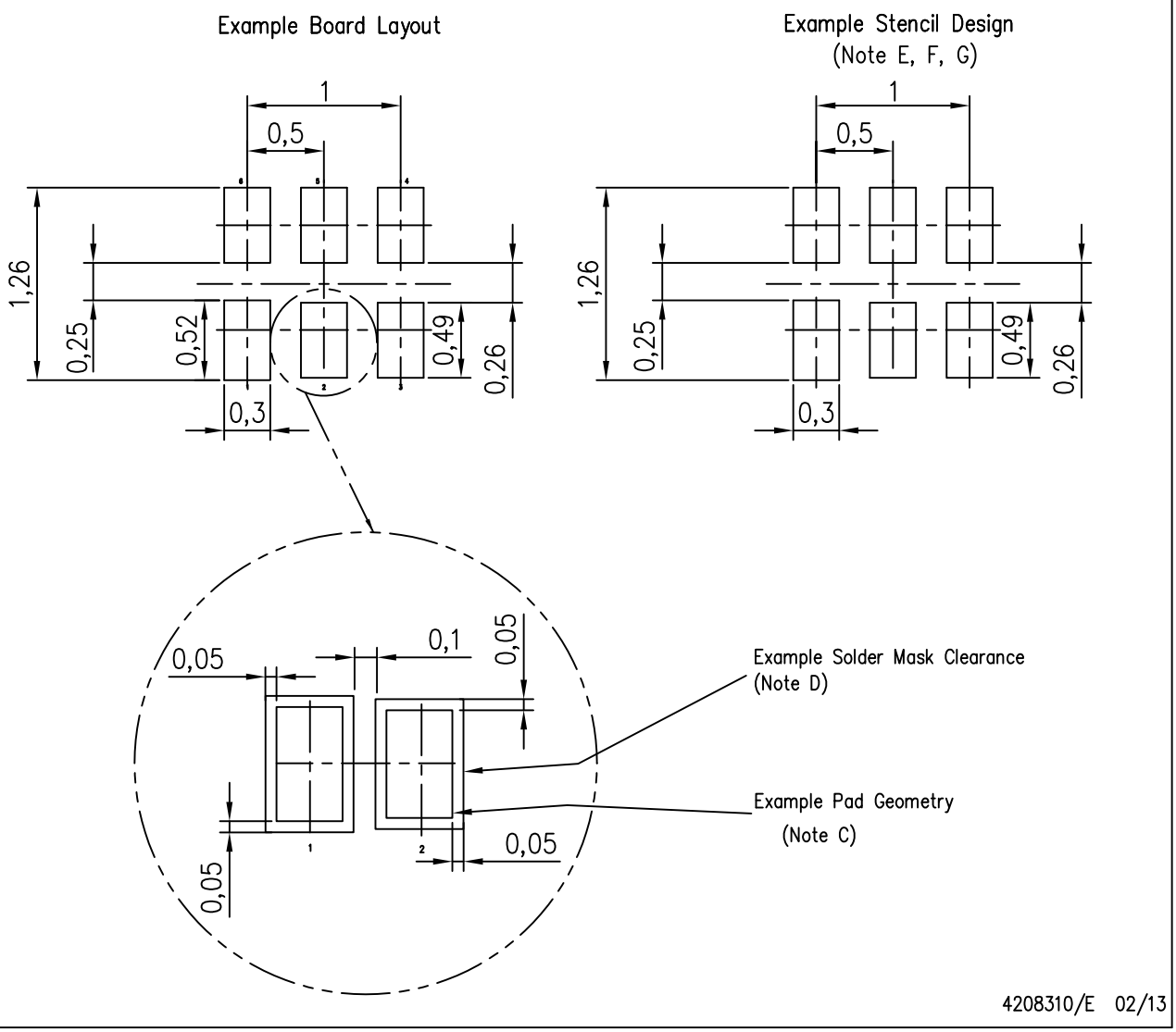
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

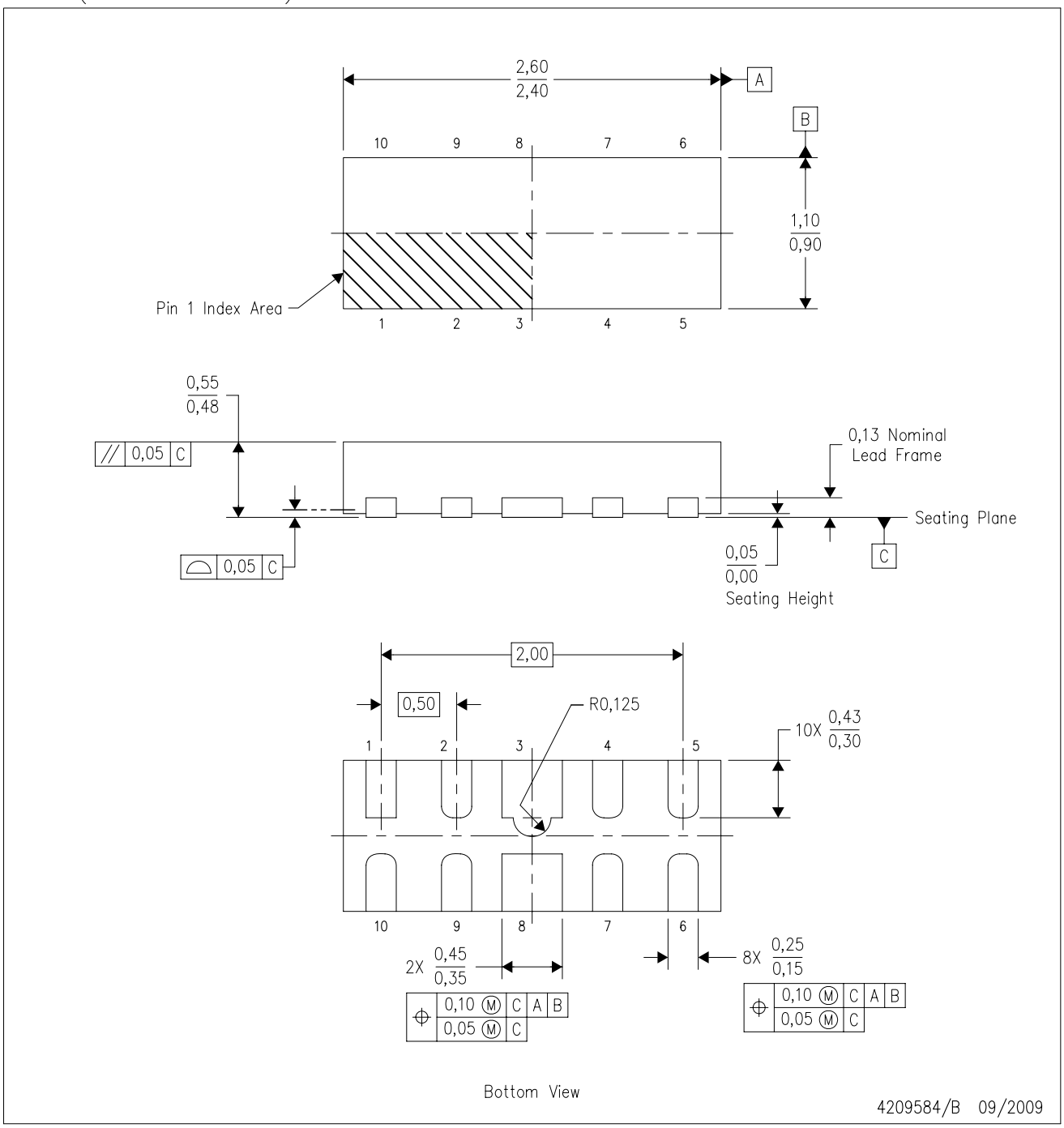
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



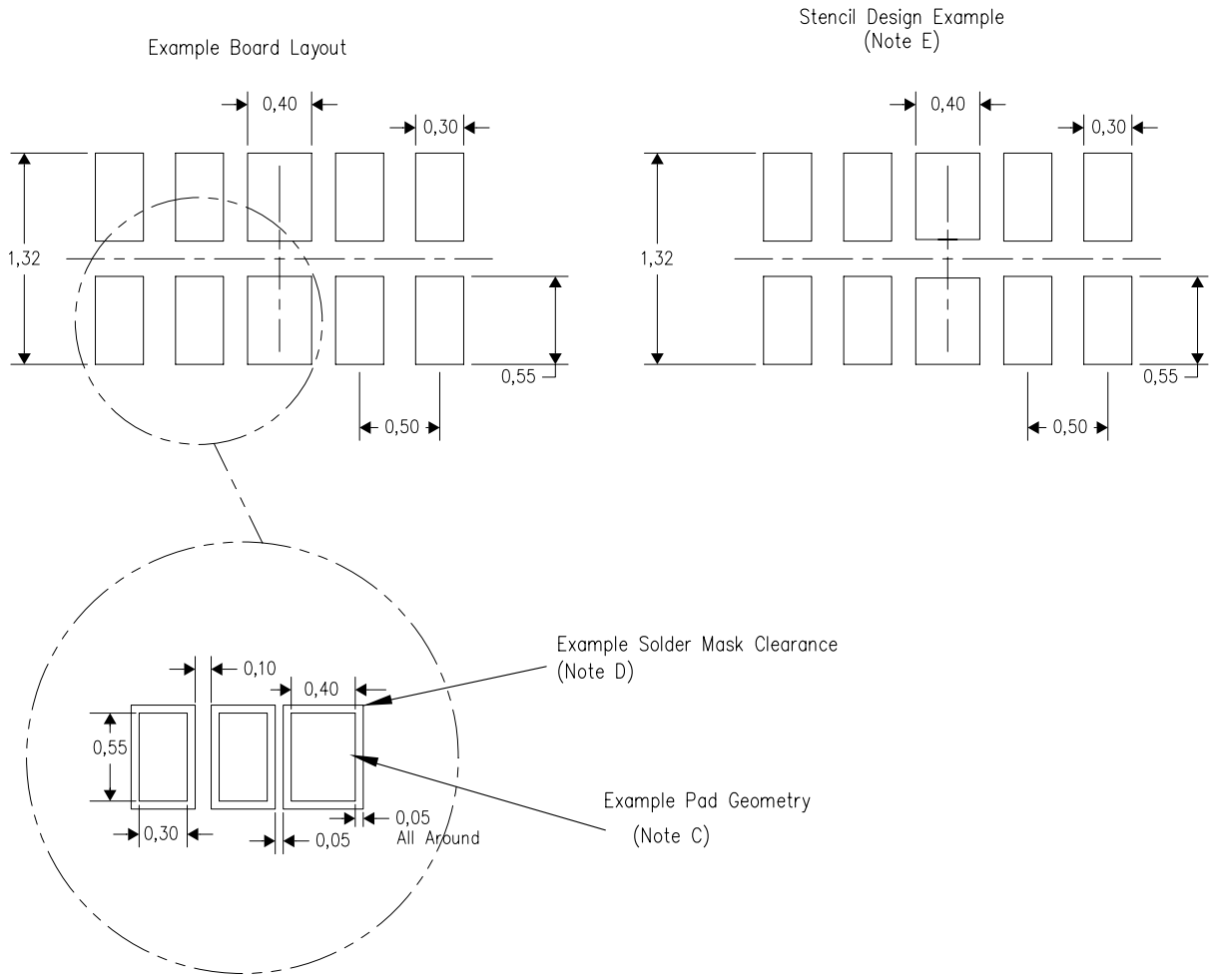
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQA (R–PSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQA (R–PUSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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