











SN74LVC1G74

SCES794E - OCTOBER 2009 - REVISED JANUARY 2015

SN74LVC1G74 Single Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset

Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Max t_{pd} of 5.9 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

Applications

- Servers
- LED Displays
- Network switch
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

Simplified Schematic

3 Description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE			
	SM8 (8)	2.95 mm × 2.80 mm			
CNIZAL VICA CZA	US8 (8)	2.30 mm × 2.00 mm			
SN74LVC1G74	X2SON (8)	1.40 mm × 1.00 mm			
	UQFN (8)	1.50 mm × 1.50 mm			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

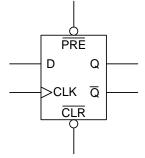




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5 Revision History

Changes f	from Revision	D (,	Januarv	2013) to	Revision E

Page

•	Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table,	
	Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation	
	section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and	
	Mechanical, Packaging, and Orderable Information section	. 1
•	Deleted Ordering Information table.	. 1
•	Updated Features	1

Changes from Original (October 2009) to Revision A

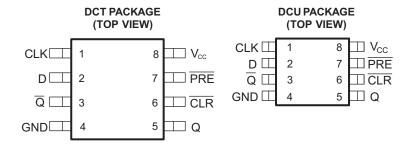
Page

•	Changed I _{off} description in <i>Features</i>
•	Changed Timing Requirements table.
	Changed Switching Requirements table

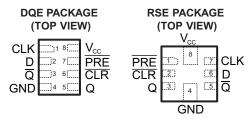
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6 Pin Configuration and Functions



See mechanical drawings for dimensions.



See mechanical drawings for dimensions

Pin Functions

	PIN	TYPE	DESCRIPTION
NAME	NO.	ITPE	DESCRIPTION
CLK	1	I	Clock input
CLR	6	I	Clear input - Pull low to set Q output low
D	2	1	Input
GND	4	_	Ground
Q	5	0	Output
Q	3	0	Inverted output
PRE	7	I	Preset input - Pull low to set Q output high
V _{CC}	8	_	Supply



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V	
V_{I}	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or po	-0.5	6.5	V	
Vo	Voltage range applied to any output in the high or low state (2)(3)	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	/ _I < 0		-50	mA
I _{OK}	Output clamp current	/ _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND		±100	mA	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

	PARAMETER	DEFINITION	VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	1000	V

1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the *Recommended Operating Conditions* table.



7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
.,	Complements	Operating	1.65	5.5	V
V _{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
.,	I Pale Java Panasta a Rana	V _{CC} = 2.3 V to 2.7 V	1.7		.,
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
		V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	
.,	Lave lavel Samuel and to be	V _{CC} = 2.3 V to 2.7 V		0.7	.,
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I_{OH}	High-level output current	V 2.V		-16	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I_{OL}	Low-level output current			16	mA
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
		RSE Package	40	0.5	
т	Operating free air temperature	DQE Package	-40	85	۰.
T_A	Operating free-air temperature	DCT Package		405	°C
		DCU Package	-40	125	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾						
		DCT	DCU	RSE	DQE	UNIT
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	227	243	261	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.



7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

P	PARAMETER	TEST CONDITIONS	V _{CC}	MIN TYP(1)	MAX	UNIT		
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V _{CC} - 0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
V _{OH}		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V		
	$I_{OH} = -16 \text{ mA}$	3 V	2.4		V			
		$I_{OH} = -24 \text{ mA}$	3 V	2.3				
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8				
		$I_{OL} = 100 \mu A$	1.65 V to 5.5 V		0.1			
		I _{OL} = 4 mA	1.65 V		0.45			
		I _{OL} = 8 mA	2.3 V		0.3	V		
V _{OL}		I _{OL} = 16 mA	3 V	0.4		v 		
		I _{OL} = 24 mA	3 V		0.55			
		I _{OL} = 32 mA	4.5 V		0.55			
I _I	Data or control inputs	V _I = 5.5 V or GND	0 to 5.5 V		±5	μΑ		
I _{off}	•	V_I or $V_O = 5.5 \text{ V}$	0		±10	μΑ		
I _{CC}		$V_1 = 5.5 \text{ V or GND}, \qquad I_0 = 0$	1.65 V to 5.5 V		10	μΑ		
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V		500	μΑ		
Ci		$V_I = V_{CC}$ or GND	3.3 V	5		рF		

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

				-40°C to 85°C									-40°C to 125°C			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V	V _{CC} =	3.3 V	V _{cc} =	= 5 V	V _{CC} =	3.3 V	V _{cc} =	5 V	UNIT	
	(1141 01)	(1141 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}				80		175		175		200		175		200	MHz	
	(CLK			2.7		2.7		2		2.7		2		20	
ı _w	PRE or CLR low		6.2		2.7		2.7		2		2.7		2		ns	
	Data		2.9		1.7		1.3		1.1		1.3		1.1			
t _{su}	PRE or C	CLR inactive	1.9		1.4		1.2		1		1.2		1.2		ns	
t _h			0		0.3		1.2		0.5		1.2		0.5		ns	

7.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

						-40°C t	o 85°C				-	-40°C to	125°C		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V	V _{CC} =	3.3 V	V _{CC} =	= 5 V	V _{CC} =	3.3 V	V _{CC} =	V _{CC} = 5 V	
	(01)	(5511 51)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN MAX		
f _{max}			80		175		175		200		175		200		MHz
	CLK	Q	4.8	13.4	2.2	7.1	2.2	5.9	1.4	4.1	2.2	7.9	1.4	6.1	
t _{pd}	CLK	Ια	6	14.4	3	7.7	2.6	6.2	1.6	4.4	2.6	8.2	1.6	6.4	ns
	PRE or CLR low	Q or Q	4.4	12.9	2.3	7	1.7	5.9	1.6	4.1	1.7	7.9	1.6	6.1	

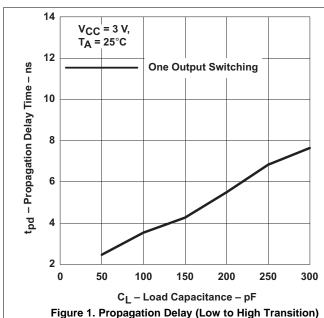


7.8 Operating Characteristics

 $T_A = 25$ °C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	$V_{CC} = 2.5 \text{ V}$	V _{CC} = 3.3 V	$V_{CC} = 5 V$	UNIT	
	PARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII	
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF	

7.9 Typical Characteristics





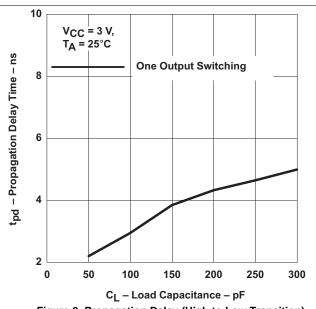
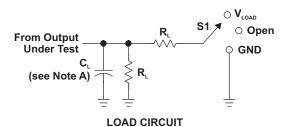


Figure 2. Propagation Delay (High to Low Transition) vs Load Capacitance

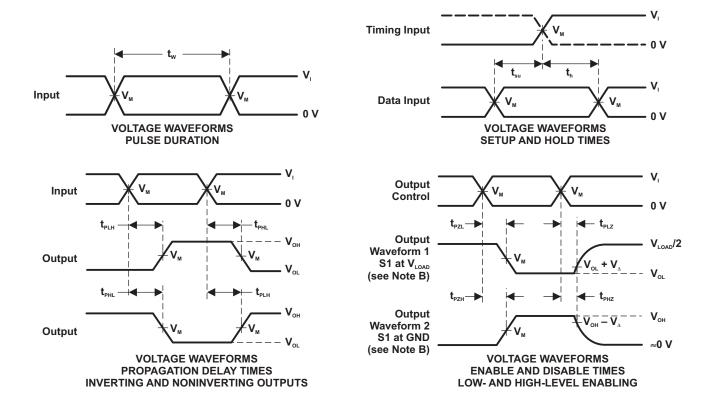


8 Parameter Measurement Information



TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	INI	PUTS		V			.,
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _⊾	V _A
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
2.5 V ± 0.2 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{o} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\mbox{\tiny PLZ}}$ and $t_{\mbox{\tiny PHZ}}$ are the same as $t_{\mbox{\tiny dis}}.$
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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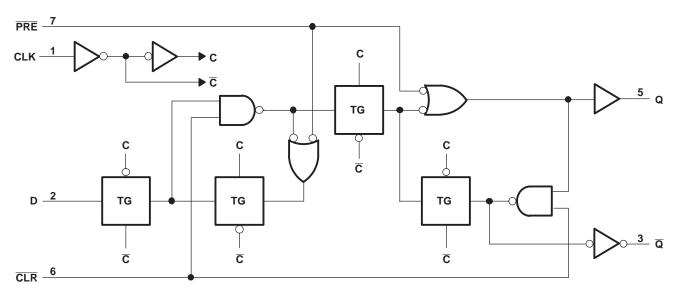


9 Detailed Description

9.1 Overview

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram



9.3 Feature Description

- Allow down voltage translation
 - 5 V to 3.3 V
 - 5.0 V to 1.8 V
 - 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V
- I_{off} Feature
 - Can prevent backflow current that can damage device when powered down

9.4 Device Functional Modes

Table 1. Function Table

	INPUTS	OUTPUTS			
PRE	CLR	CLK	D	Q	Ø
L	Н	X	X	Н	Г
Н	L	X	X	L	Н
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
Н	Н	↑	Н	Н	L
Н	Н	↑	L	L	Н
Н	Н	L	X	Q_0	\overline{Q}_0

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.



10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The resistor and capacitor at the $\overline{\text{CLR}}$ pin are optional. If they are not used, the $\overline{\text{CLR}}$ pin should be connected directly to V_{CC} to be inactive.

10.2 Typical Power Button Circuit

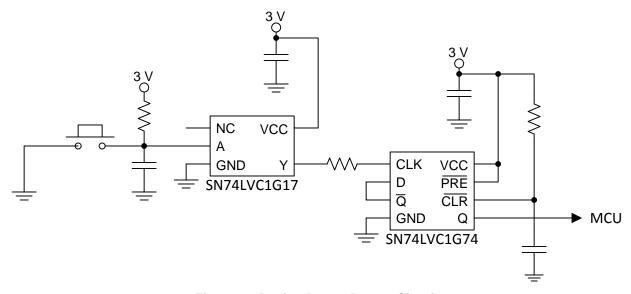


Figure 4. Device Power Button Circuit

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

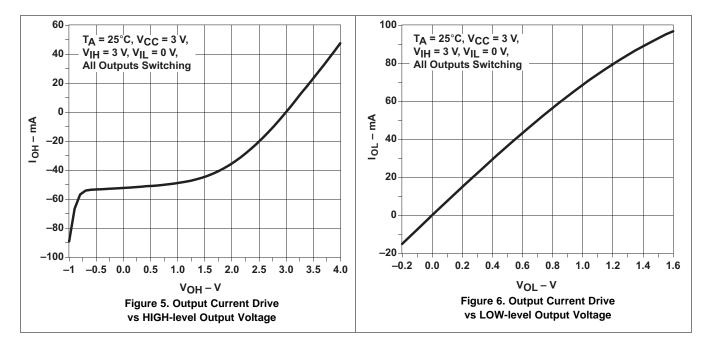
- 1. Recommended Input Conditions:
 - For rise time and fall time specifications, see (Δt/ΔV) in Recommended Operating Conditions table.
 - For specified high and low levels, see (V_{IH} and V_{IL}) in Recommended Operating Conditions table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- 2. Recommend Output Conditions:
 - Load currents should not exceed 50 mA per output and 100 mA total for the part.
 - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the



Typical Power Button Circuit (continued)

output current.

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} terminals then .01- μ F or .022- μ F capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.



12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example

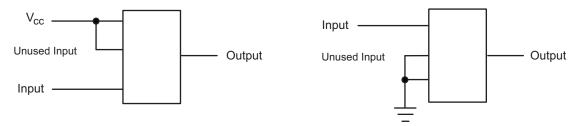


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

NanoFree is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

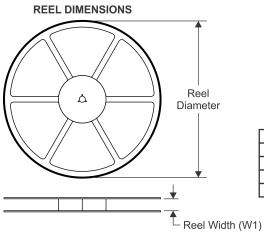
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGE MATERIALS INFORMATION

www.ti.com 14-Nov-2014

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G74DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1G74DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DCUR	US8	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DCURG4	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DCUT	US8	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DCUT	US8	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DQER	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
SN74LVC1G74RSE2	UQFN	RSE	8	5000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q3
SN74LVC1G74RSER	UQFN	RSE	8	5000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q2

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G74DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC1G74DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G74DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G74DCURG4	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G74DCUT	US8	DCU	8	250	202.0	201.0	28.0
SN74LVC1G74DCUT	US8	DCU	8	250	202.0	201.0	28.0
SN74LVC1G74DQER	X2SON	DQE	8	5000	184.0	184.0	19.0
SN74LVC1G74RSE2	UQFN	RSE	8	5000	184.0	184.0	19.0
SN74LVC1G74RSER	UQFN	RSE	8	5000	184.0	184.0	19.0

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.



DCU (S-PDSO-G8)

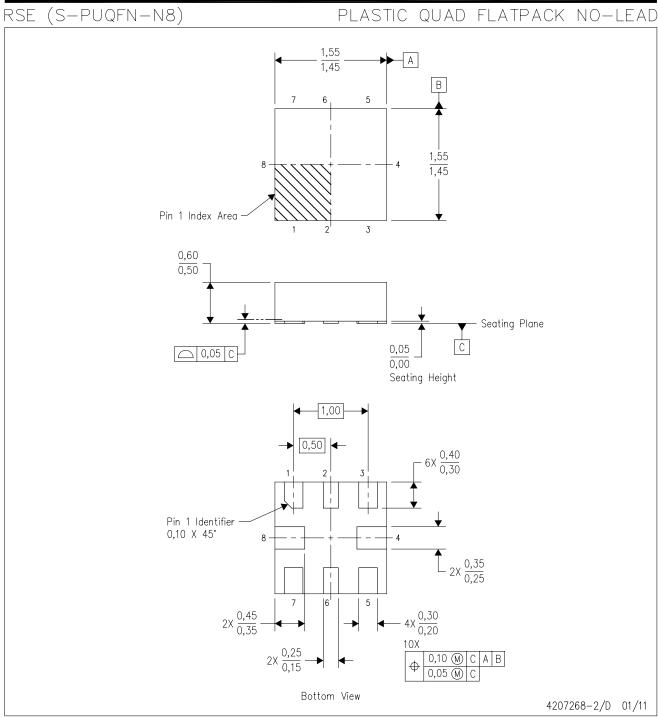
PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





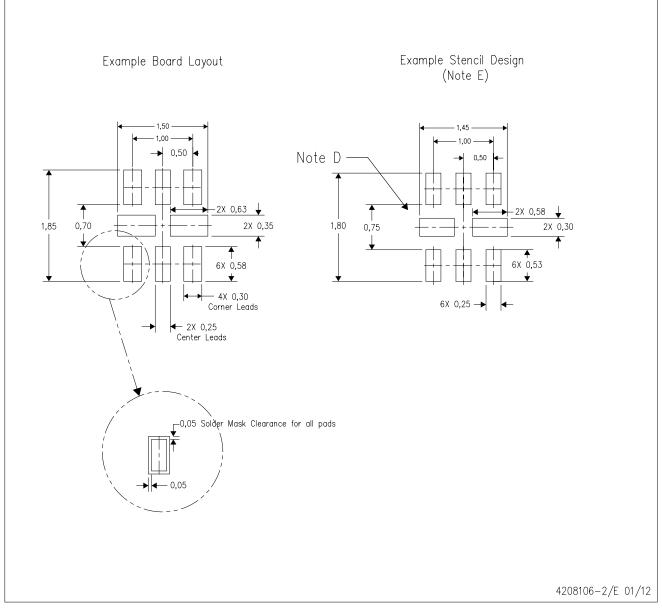
NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
 C. QFN (Quad Flatpack No-Lead) package configuration.
 D. This package complies to JEDEC MO-288 variation UECD.



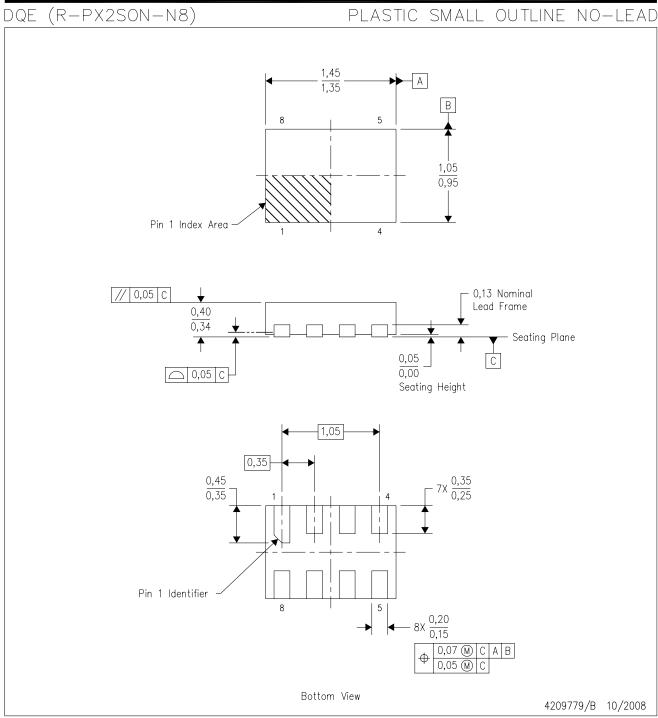
RSE (S-PUQFN-N8)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





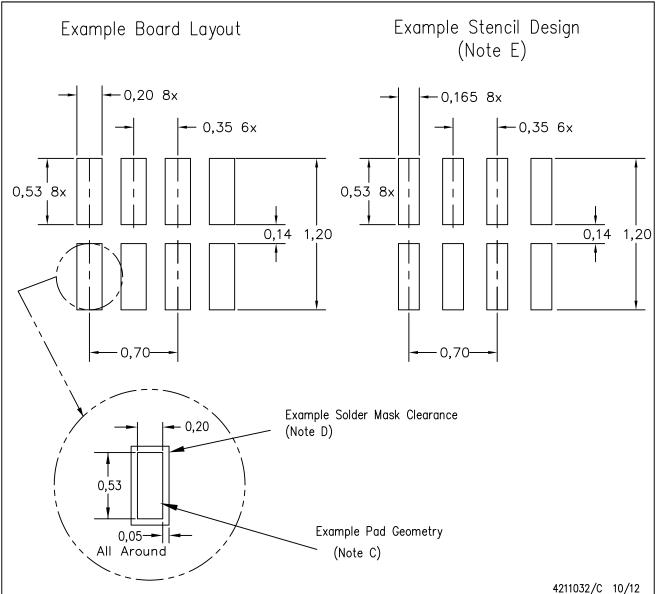
NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
 C. SON (Small Outline No-Lead) package configuration.
 D. This package complies to JEDEC MO-287 variation X2EAF.



DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Over—printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
- H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- I. Component placement force should be minimized to prevent excessive paste block deformation.



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