TPS744xx 3.0-A Ultra-LDO with Programmable Soft-Start

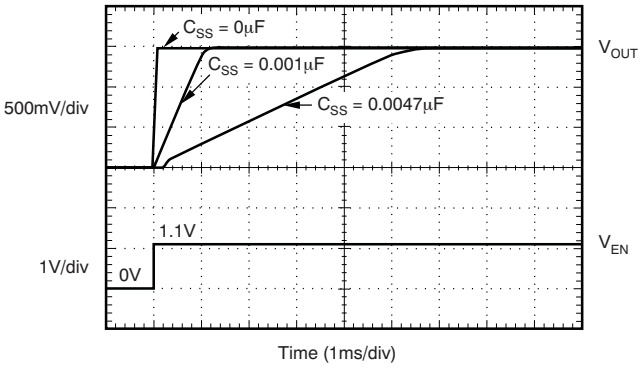
1 Features

- Soft-Start (SS) Pin Provides a Linear Startup With Ramp Time Set by External Capacitor
- 1% Accuracy Over Line, Load, and Temperature
- Supports Input Voltages as Low as 0.9 V With External Bias Supply
- Adjustable Output (0.8 V to 3.6 V)
- Fixed Output (0.9 V to 3.6 V)
- Ultra-Low Dropout: 115 mV at 3.0 A (typical)
- Stable With Any or No Output Capacitor
- Excellent Transient Response
- Available in 5-mm × 5-mm × 1-mm QFN and DDPAK-7 Packages
- Open-Drain Power-Good (QFN Only)

2 Applications

- FPGA Applications
- DSP Core and I/O Voltages
- Post-Regulation Applications
- Applications With Special Start-Up Time or Sequencing Requirements
- Hot-Swap and Inrush Controls

Turn-On Response



3 Description

The TPS744xx low-dropout (LDO) linear regulators provide an easy-to-use robust power-management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility lets the user configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with specific start-up requirements.

A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. The TPS744xx family of LDOs is stable without an output capacitor or with ceramic output capacitors. The device family is fully specified from T_J = –40°C to 125°C. The TPS744xx is offered in a small (5-mm × 5-mm) QFN package, yielding a highly compact total solution size. For applications that require additional power dissipation, the DDPAK (KTW) package is also available.

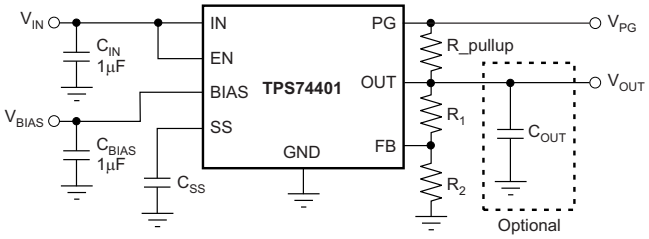
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS744xx	TO-263 (7)	10.10 mm x 8.89 mm
	VQFN (20)	5.00 mm x 5.00 mm

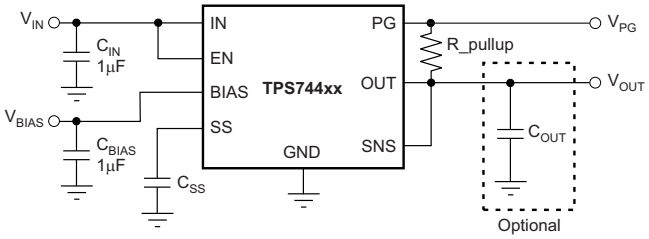
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuits

ADJUSTABLE VOLTAGE VERSION



FIXED VOLTAGE VERSION



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (March 2013) to Revision P — **Page**

- Deleted Active High Enable bullet from *Features* list ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4
- Changed footnote 3c for *Thermal Information* table ... 5
- Changed y-axis in Figure 1, Figure 2, Figure 4, and Figure 7 from abbreviation (I_{OUT}) to text (Output Current) ... 7
- Added "V" to V_{IN} = 1.8 V condition in Figure 9, Figure 10, and Figure 11 ... 7
- Changed Figure 25; made V_{OUT} trace red to show data trend separation ... 10
- Changed *Overview* section text ... 12
- Changed second paragraph of *Dropout Voltage* ... 17
- Changed Figure 29; updated equation in figure ... 17

Changes from Revision N (December 2012) to Revision O — **Page**

- Changed RGW and KTW values in Thermal Information table ... 5

Changes from Revision M (November 2010) to Revision N — **Page**

- Changed T_J max value from 125 to 150 in Absolute Maximum Ratings table ... 4

Changes from Revision L (August, 2010) to Revision M — **Page**

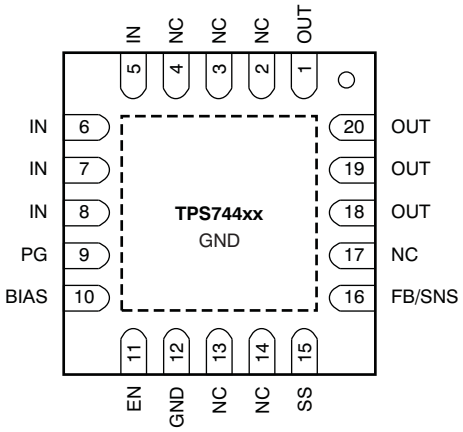
- Corrected equation for Table 1 ... 15

Changes from Revision K (December, 2009) to Revision L **Page**

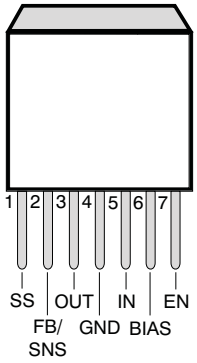
- Replaced the *Dissipation Ratings* table with the *Thermal Information* table 5
- Revised *Layout Recommendations and Power Dissipation* section 23
- Revised *Estimating Junction Temperature* section 23

5 Pin Configuration and Functions

RGW Package
5-mm × 5-mm QFN-20
(Top View)



KTW Package
DDPAK-7
Surface-Mount



Pin Functions

PIN			I/O	DESCRIPTION
NAME	KTW	RGW		
BIAS	6	10	I	Bias input voltage for error amplifier, reference, and internal control circuits. A 1uF or larger input capacitor is recommended for optimal performance. If IN is connect to BIAS, a 4.7-uF or larger capacitor should be used.
EN	7	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
FB	2	16	I	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating. (Adjustable version only.)
GND	4	12	—	Ground
IN	5	5–8	I	Unregulated input to the device. An input capacitor of 1 µF or greater is recommended for optimal performance.
NC	N/A	2–4, 13, 14, 17	O	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	3	1, 18–20	O	Regulated output voltage. No capacitor is required on this pin for stability, but is recommended for optimal performance.
PAD/TAB	—	—	—	Must be soldered to the ground plane for increased thermal performance. Internally connect to ground. Internally connected to ground.
PG	N/A	9	O	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
SNS	2	16	I	This pin is the sense connection to the load device. This pin must be connected to V_{OUT} and must not be left floating. (Fixed versions only.)
SS	1	15	—	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100 µs.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	+6	V
V_{EN}	Enable voltage	–0.3	+6	V
V_{PG}	Power-good voltage	–0.3	+6	V
I_{PG}	PG sink current	0	+1.5	mA
V_{SS}	SS pin voltage	–0.3	+6	V
V_{FB}	Feedback pin voltage	–0.3	+6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.1		5.5	V
V_{EN}	Enable supply voltage range	0		5.5	V
V_{BIAS} (1)	BIAS supply voltage range	V_{OUT} + 1.62		5.5	V
I_{OUT}	Output current	0		3	A
C_{OUT}	Output capacitor	0			µF
C_{IN} (2)	Input capacitor	1			µF
C_{BIAS}	Bias capacitor	1			µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS744xx[3]		UNIT
		RGW	KTW	
		20 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	41.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	12.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	4.0	
ψ_{JB}	Junction-to-board characterization parameter	14.8	7.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the RGW and KTW packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. RGW: The exposed pad is connected to the PCB ground layer through a 4x4 thermal via array.
ii. KTW: The exposed pad is connected to the PCB ground layer through a 6x6 thermal via array.
(b) Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, refer to the *Estimating Junction Temperature*.

6.5 Electrical Characteristics

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{IN} = C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.375		5.25	V
V_{REF}	Internal reference (adjustable version)	T_J = 25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A, V_{BIAS} = 5 V	V_{REF}		3.6	V
	Accuracy(1)	2.97 V ≤ V_{BIAS} ≤ 5.25 V, V_{OUT} + 1.62 V ≤ V_{BIAS}, 50 mA ≤ I_{OUT} ≤ 3.0 A	–1%	±0.2%	+1%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V, QFN		0.0005	0.05	%/V
		$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V, DDPAK		0.0005	0.06	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.013		%/mA
		50 mA ≤ I_{OUT} ≤ 3.0 A		0.03		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 3.0 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 1.62 V, QFN		115	195	mV
		I_{OUT} = 3.0 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 1.62 V, DDPAK		120	240	
	V_{BIAS} dropout voltage(2)	I_{OUT} = 3.0 A, V_{IN} = V_{BIAS}			1.62	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT(nom)}$, QFN	3.8		6.0	A
		V_{OUT} = 80% × $V_{OUT(nom)}$, DDPAK	3.5		6.0	
I_{BIAS}	Bias pin current	I_{OUT} = 0 mA to 3.0 A		2	4	mA
I_{SHDN}	Shutdown supply current (V_{IN})	V_{EN} ≤ 0.4 V		1	100	µA
I_{FB}, I_{SNS}	Feedback, Sense pin current(3)	I_{OUT} = 50 mA to 3.0 A	–250	95	250	nA
PSRR(4)	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		73		dB
		800 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		42		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		62		dB
		800 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		
V_n	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 0.001 µF		16 × V_{OUT}		μV_{RMS}
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 100 mA to 3.0 A at 1 A/µs, C_{OUT} = 0 µF		4		%V_{OUT}
t_{STR}	Minimum startup time	I_{OUT} = 1.5 A, C_{SS} = open		100		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V	0.5	0.73	1	µA
$V_{EN(high)}$	Enable input high level		1.1		5.5	V
$V_{EN(low)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			50		mV
$V_{EN(dg)}$	Enable pin de-glitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG(low)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.03	1	µA
T_J	Operating junction temperature		–40		125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		155		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
(3) I_{FB}, I_{SNS} current flow is out of the device.
(4) See Figure 8 to Figure 11 for PSRR at different conditions.

6.6 Typical Characteristics

At T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

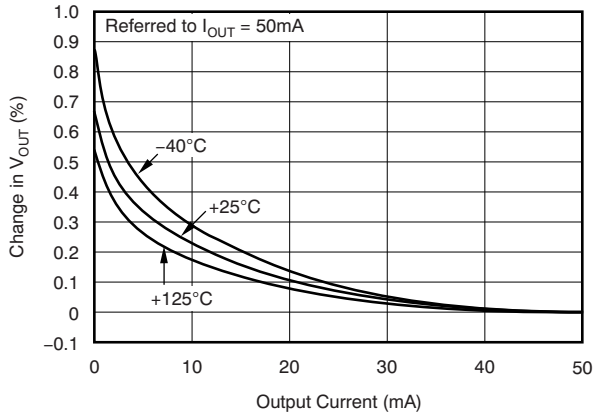


Figure 1. Load Regulation

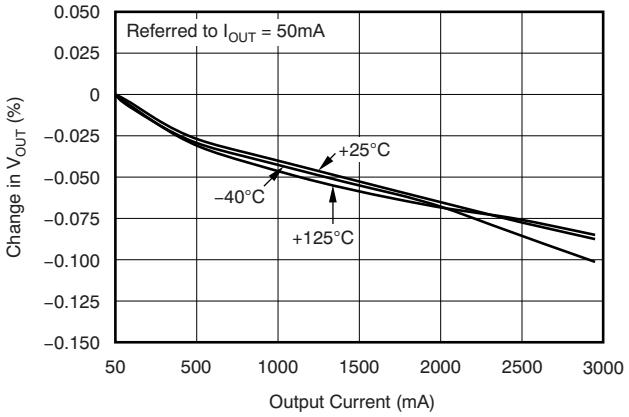


Figure 2. Load Regulation

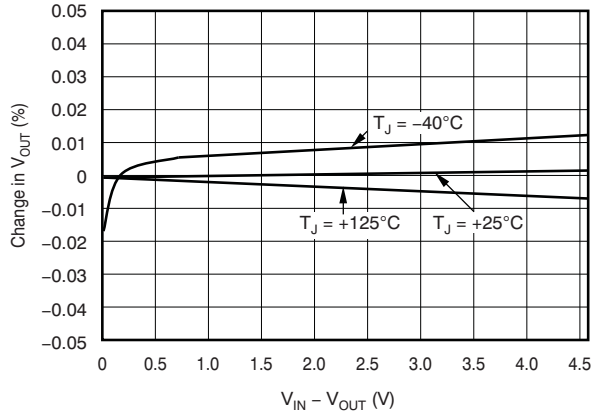


Figure 3. Line Regulation

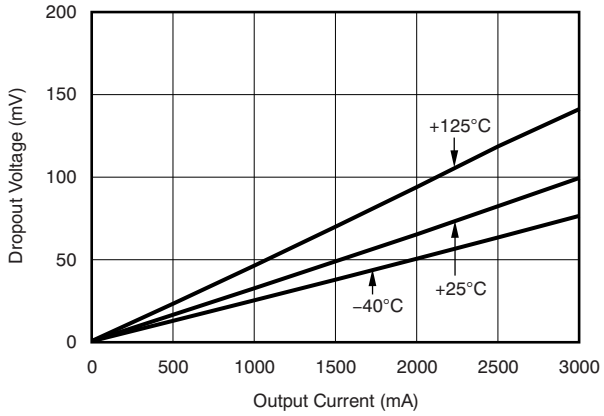


Figure 4. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

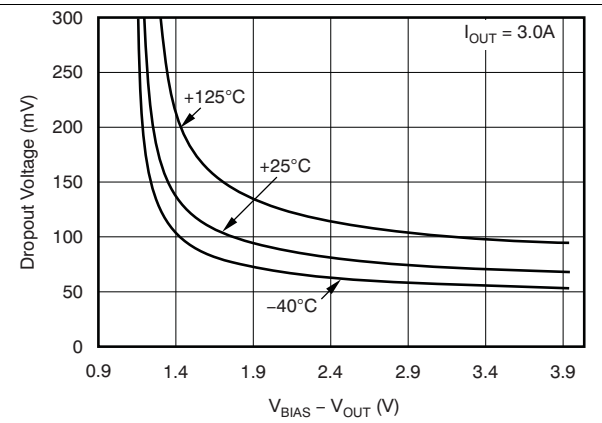


Figure 5. V_{IN} Dropout Voltage vs V_{BIAS} − V_{OUT} and Temperature (T_J)

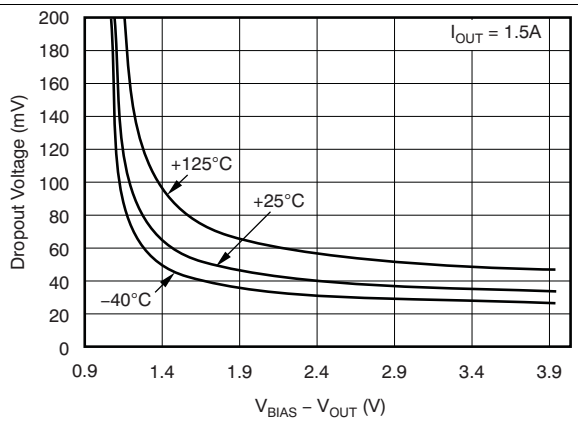


Figure 6. V_{IN} Dropout Voltage vs V_{BIAS} − V_{OUT} and Temperature (T_J)

Typical Characteristics (continued)

At T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

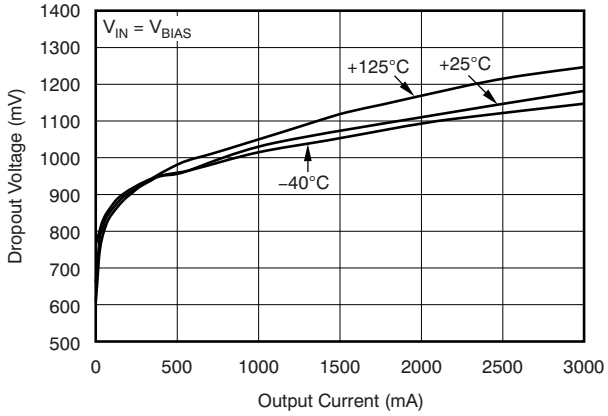


Figure 7. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

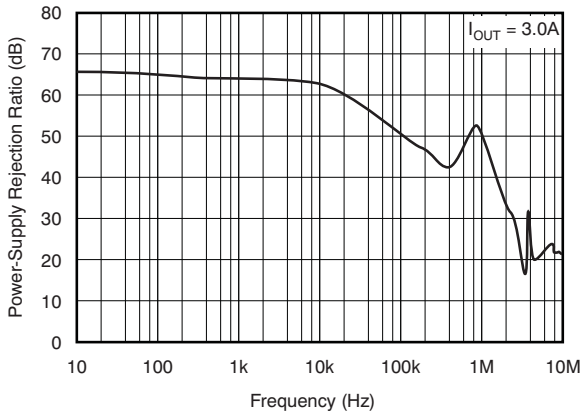


Figure 8. V_{BIAS} PSRR vs Frequency

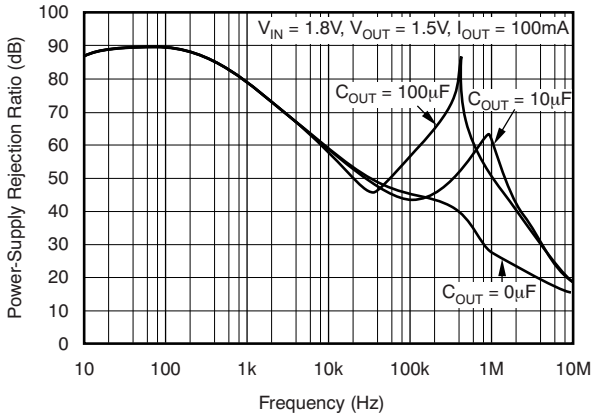


Figure 9. V_{IN} PSRR vs Frequency

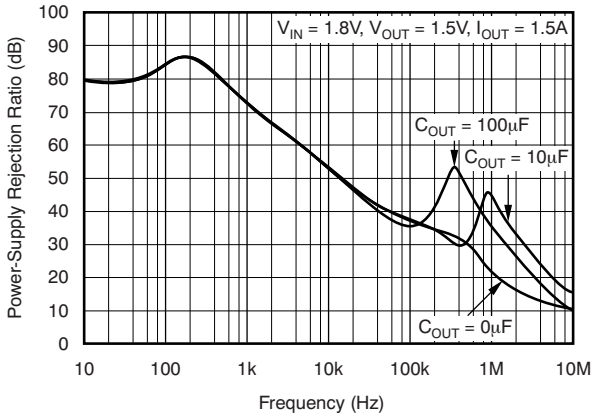


Figure 10. V_{IN} PSRR vs Frequency

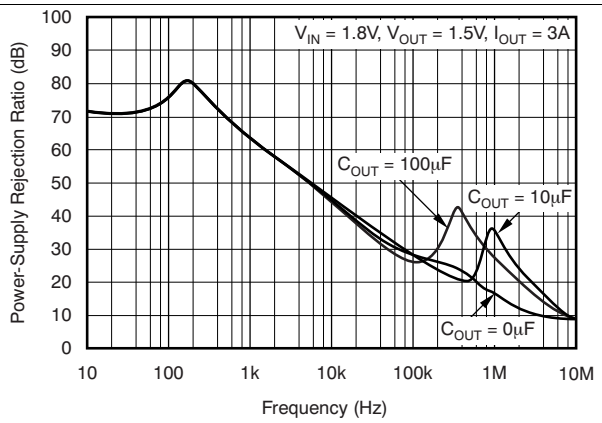


Figure 11. V_{IN} PSRR vs Frequency

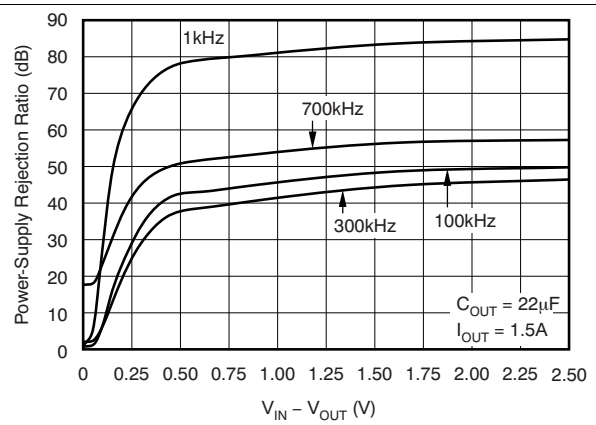


Figure 12. V_{IN} PSRR vs V_{IN} – V_{OUT}

Typical Characteristics (continued)

At T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

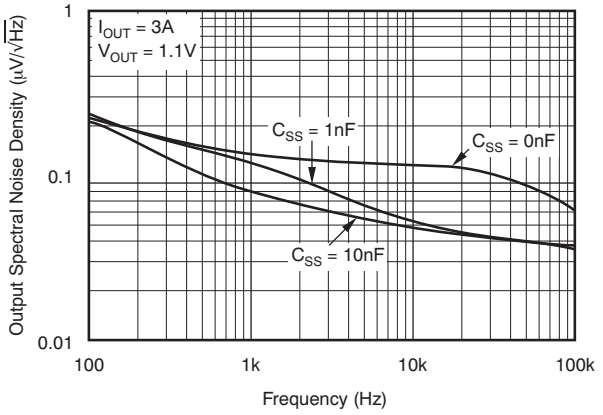


Figure 13. Noise Spectral Density

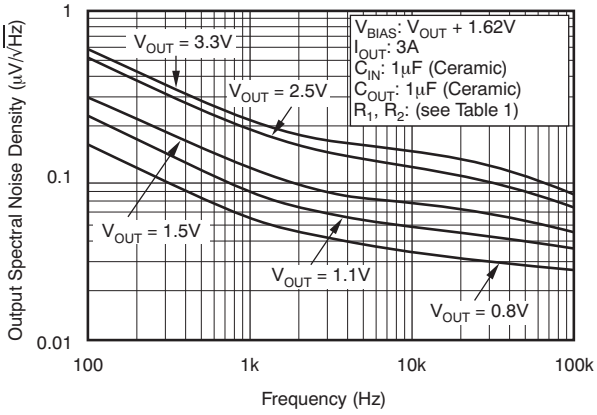


Figure 14. Noise Spectral Density

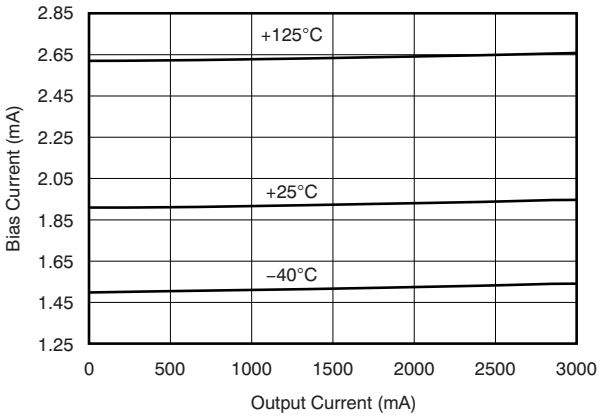


Figure 15. I_{BIAS} vs Output Current and Temperature

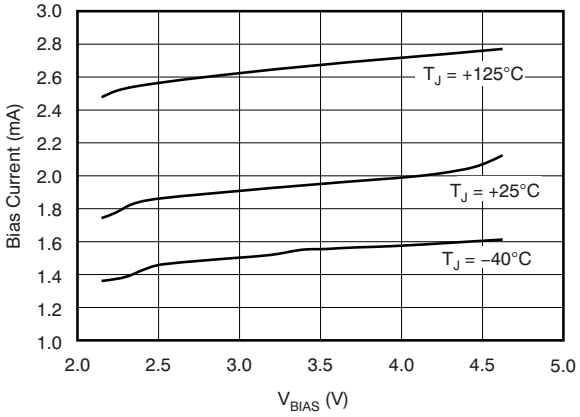


Figure 16. I_{BIAS} vs V_{BIAS} and V_{OUT}

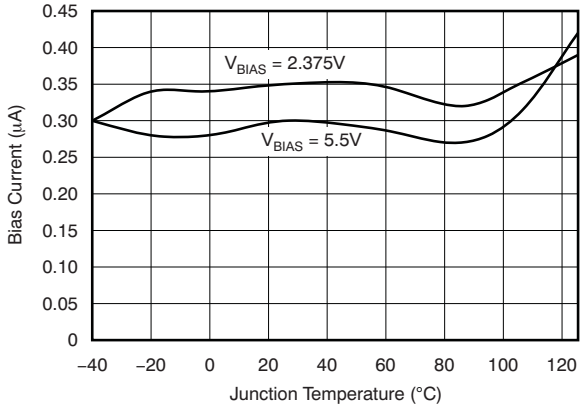


Figure 17. I_{BIAS} Shutdown vs Temperature

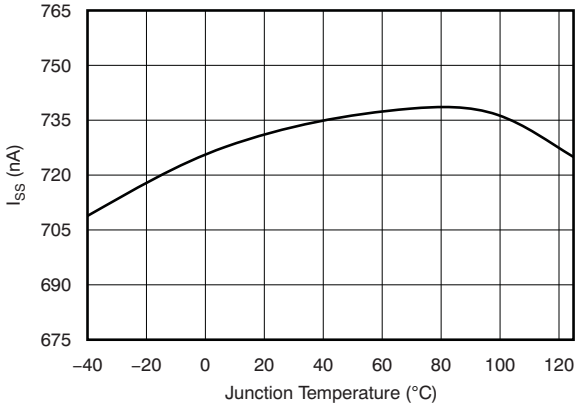


Figure 18. Soft-Start Charging Current (I_{SS}) vs Temperature

Typical Characteristics (continued)

At T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

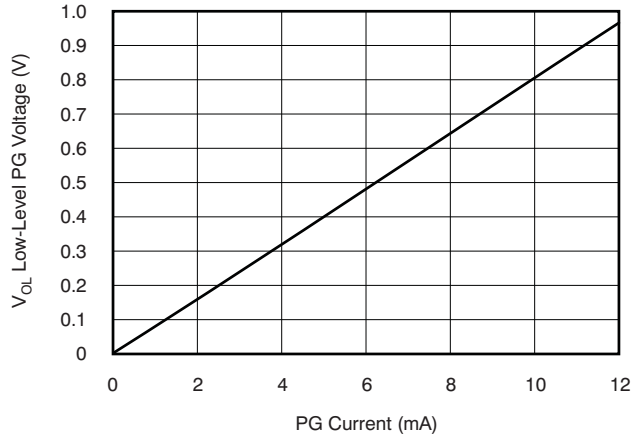


Figure 19. Low-Level PG Voltage vs PG Current

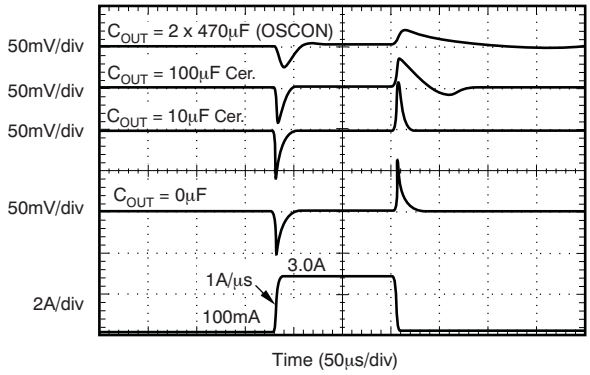


Figure 20. Load Transient Response

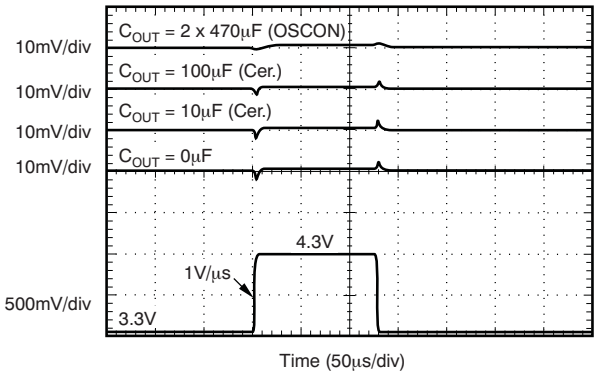


Figure 21. V_{BIAS} Line Transient (3 A)

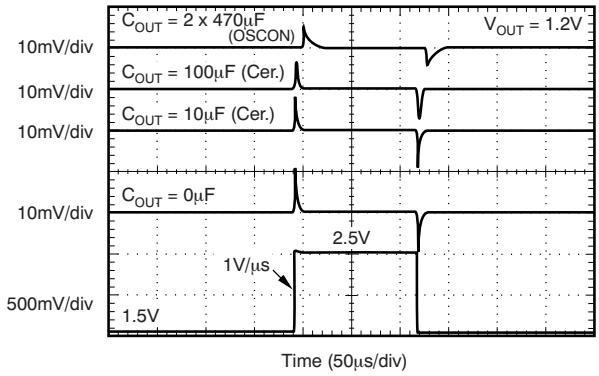


Figure 22. V_{IN} Line Transient (3 A)

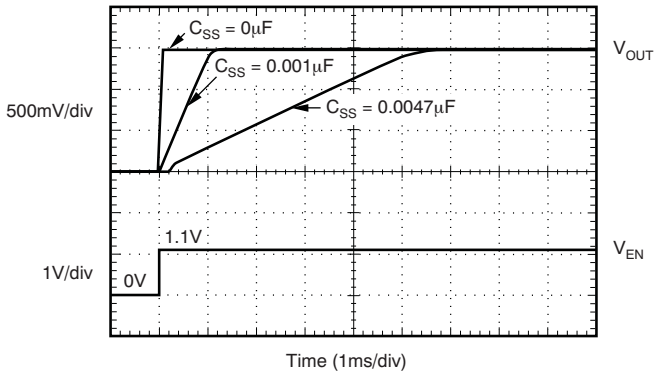


Figure 23. Turn-On Response

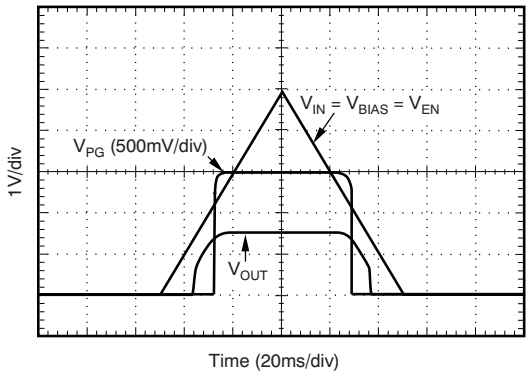


Figure 24. Power-Up/Power-Down

Typical Characteristics (continued)

At T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, C_{IN} = 1 µF, C_{BIAS} = 1 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF, unless otherwise noted.

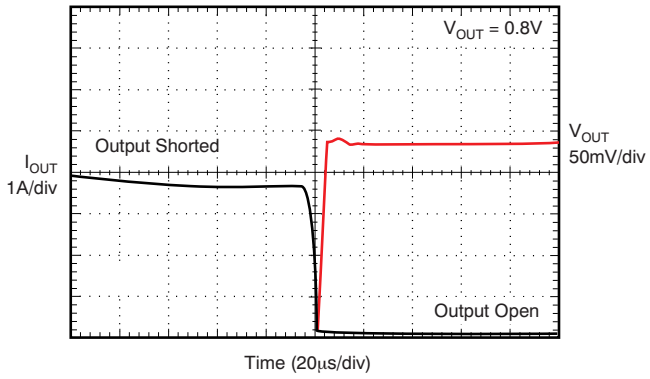


Figure 25. Output Short-Circuit Recovery

7 Detailed Description

7.1 Overview

The TPS744xx family of low-dropout regulators (LDOs) incorporates many features to ensure a wide range of uses. Hysteresis and de-glitch on the EN input improve the ability to sequence multiple devices without worrying about false start-up. The soft-start is fully programmable and allows the user to control the startup time of the LDOs output. There is also hysteresis on the PG comparator, to ensure no false PG signals. The TPS744xx family of LDOs is ideal for FPGAs, DSPs, and any other device that requires a linear supply and sequencing.

7.2 Functional Block Diagrams

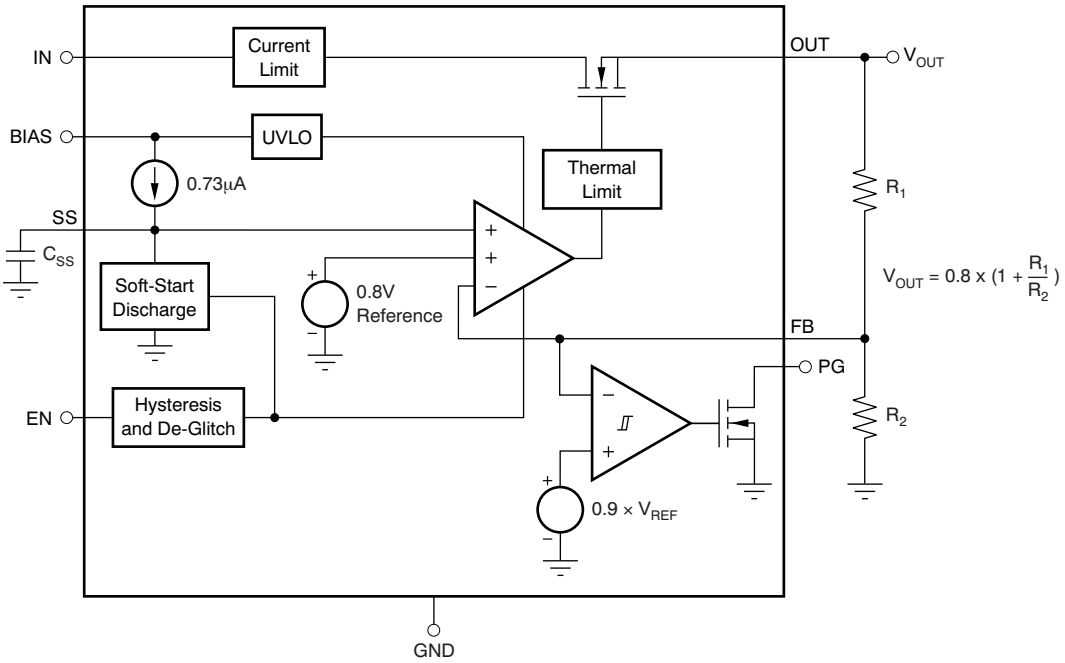


Figure 26. Adjustable Voltage Version

Functional Block Diagrams (continued)

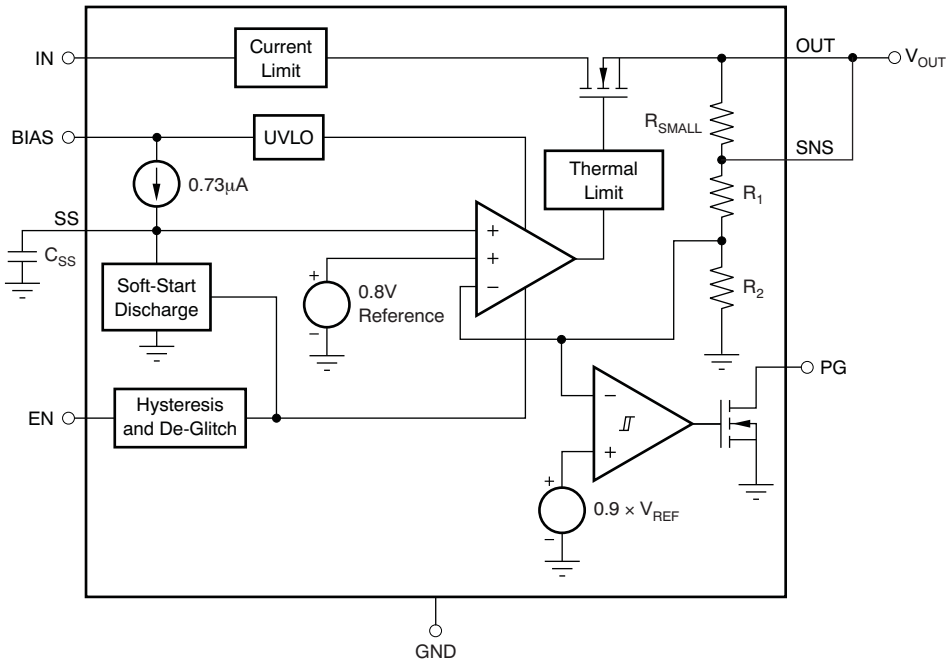


Figure 27. Fixed Voltage Versions

7.3 Feature Description

7.3.1 Enable/Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} lower than 0.4 V turns the regulator off, while V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and de-glitching for use with relatively slow-ramping analog signals. This configuration allows the TPS744xx to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a de-glitch circuit to help avoid on-off cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8V and varies with temperature and process variations. Temperature variation is approximately –1mV/°C; therefore, process variation accounts for most of the variation in the enable threshold. If precise turn-on timing is required, a fast rise-time signal should be used to enable the TPS744xx.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

7.3.2 Power-Good (QFN Package Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pull-up resistor. This pin requires at least 1.1 V on V_{BIAS} in order to have a valid output. The PG output is high-impedance when V_{OUT} is greater than (V_{IT} + V_{HYS}). If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pull-up resistor for PG must be in the range of 10 kΩ to 1 MΩ. PG is only provided on the QFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

Feature Description (continued)

7.3.3 Internal Current Limit

The TPS744xx features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 3.5 A and maintain regulation. The current limit responds in approximately 10 µs to reduce the current during a short-circuit fault. Recovery from a short-circuit condition is well-controlled and results in very little output overshoot when the load is removed. See Figure 25 in *Typical Characteristics* for short-circuit recovery performance.

The internal current limit protection circuitry of the TPS744xx is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS744xx above the rated current degrades device reliability.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 155°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 30°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS744xx is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS744xx into thermal shutdown degrades device reliability.

7.4 Programming

7.4.1 Programmable Soft-Start

The TPS744xx features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic soft-start, the TPS744xx error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), the soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 1:

$$t_{SS} = \frac{\left(V_{REF} \times C_{SS}\right)}{I_{SS}} \quad (1)$$

Programming (continued)

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 2:

$$t_{SSCL} = \frac{(V_{OUT(nom)} \times C_{OUT})}{I_{CL(min)}} \quad (2)$$

$V_{OUT(nom)}$ is the nominal set output voltage as set by the user, C_{OUT} is the output capacitance, and $I_{CL(min)}$ is the minimum current limit for the device. In applications where monotonic startup is required, the soft-start time given by Equation 1 should be set to be greater than Equation 2.

The maximum recommended soft-start capacitor is 0.015 µF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when re-enabled. Soft-start capacitors larger than 0.015 µF may be a problem in applications where the user must rapidly pulse the enable pin and also require the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Refer to Table 1 for suggested soft-start capacitor values.

Table 1. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1 ms
470 pF	0.5 ms
1000 pF	1 ms
4700 pF	5 ms
0.01 µF	10 ms
0.015 µF	16 ms

(1) $$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.73\mu A}$$ where $t_{SS}(s)$ = soft-start time in seconds.

7.4.2 Sequencing Requirements

The device can have V_{IN}, V_{BIAS}, and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} and V_{BIAS} are present is preferred, and can be accomplished using a digital output from a processor or supply supervisor. An analog signal from an external RC circuit, as shown in Figure 28, can also be used as long as the delay time is long enough for V_{IN} and V_{BIAS} to be present.

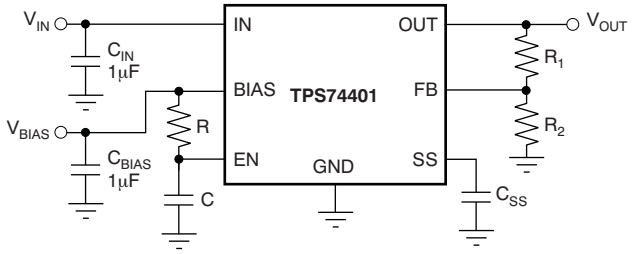


Figure 28. Soft-Start Delay Using an RC Circuit on Enable

If a signal is not available to enable the device after IN and BIAS, simply connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply less the dropout voltage until it reaches the set output voltage. If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS744xx belongs to a family of new generation ultra-low dropout regulators that feature soft-start and tracking capabilities. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS744xx to be stable with any or even no output capacitor. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS744xx features a programmable, voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits startup inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and de-glitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

8.1.1 Input, Output, and Bias Capacitor Requirements

The TPS744xx does not require any output capacitor for stability. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, of any type or value. This flexibility is a result of an innovative control loop that ensures the device is stable independent of the output capacitance.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good quality, low-ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance and to help ensure stability.

8.1.2 Transient Response

The TPS744xx was designed to have transient response within 5% for most applications without any output capacitor. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time. Refer to Figure 20 in *Typical Characteristics*. Because the TPS744xx is stable without an output capacitor, many applications may allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

8.1.3 Dropout Voltage

The TPS744xx offers industry-leading dropout performance, making it well-suited for high-current, low V_{IN}/low V_{OUT} applications. The extremely low dropout of the TPS744xx also allows the device to be used in place of a dc/dc converter and also achieve good efficiencies. Equation 3 provides a quick estimate of the efficiencies.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \quad (3)$$

Application Information (continued)

This efficiency allows users to redesign the power architecture for their applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS744xx. The first specification (illustrated in Figure 41) is referred to as *V_{IN} Dropout* and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62 V above V_{OUT}; for example, when V_{BIAS} is powered by a 3.3-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than (3.3 V × 0.95) or V_{OUT} is less than 1.5 V, V_{IN} dropout is less than specified.

The second specification (shown in Figure 42) is referred to as *V_{BIAS} Dropout* and is for users who wish to tie IN and BIAS together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be 1.62 V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

8.1.4 Output Noise

The TPS744xx provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001-µF soft-start capacitor, the output noise is reduced by half and is typically 19 μV_{RMS} for a 1.2-V output (100 Hz to 100 kHz). Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-µF soft-start capacitor is given in Equation 4.

$$V_N\left(\mu V_{RMS}\right) = 16\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}\,(V) \tag{4}$$

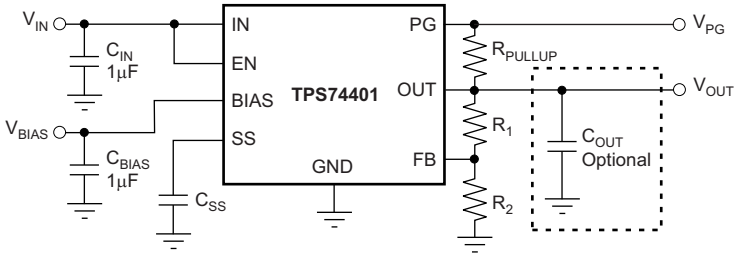
The low output noise of the TPS744xx makes it a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

8.2 Typical Applications

8.2.1 Adjustable Voltage Part and Setting

Figure 29 illustrates a typical application circuit for the TPS74401 adjustable output device.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 29. Refer to Table 2 for sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications, R_2 should be ≤ 4.99 kΩ.



$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2$$

Figure 29. Typical Application Circuit for the TPS74401 (Adjustable Version)

Table 2. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1/R_2)$

NOTE

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

8.2.1.1 Design Requirements

The design goals are V_{IN} = 1.8 V, V_{OUT} = 1.5 V, and I_{OUT} = 2 A max. The design should optimize transient response while meeting a 1-ms startup time with a startup dominated by the soft-start feature. The input supply comes from a supply on the same circuit board. The available system rails for V_{BIAS} are 2.7 V, 3.3 V, and 5 V.

The design space consists of C_{IN}, C_{OUT}, C_{BIAS}, C_{SS}, V_{BIAS}, R_1, R_2, and R_3, and the circuit is from Figure 29.

This example uses a V_{IN} of 1.8 V, with V_{BIAS} of 2.5 V.

8.2.1.2 Detailed Design Procedure

The first step for this design is to examine the maximum load current along with the input and output voltage requirements, to determine if the device thermal and dropout voltage requirements can be met. At 3 A, the input dropout voltage of the TPS744xx family is a maximum of 240 mV over temperature. As a result, the dropout headroom is sufficient for operation over both input and output voltage accuracy.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is (1.8 V – 1.5 V), giving us a V_{DROP} = 300 mV. The power dissipated can than be estimated by the equation $P_{DISS} = I_{L(max)} \times V_{DROP}$ = ~600 mW. This calculation gives an efficiency of nearly 83.3% by using Equation 3.

Once the power dissipated in the linear regulator is known, the corresponding junction temperature increase can be calculated. To estimate the junction temperature increase above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information, refer to *Thermal Information*. For this example, using the KTW package, the junction temperature rise is calculated to be 21.2°C. The maximum junction temperature increase is calculated by adding the junction temperature rise to the maximum ambient temperature. In this example, the maximum junction temperature is 46.2°C. Keep in mind that the junction temperate must be less than 125°C for reliable operation. Additional ground planes, added thermal vias, and air flow all help to improve the thermal transfer characteristics of the system.

The next step is to determine the bias voltage or if a separate source is needed for the bias voltage. Because $V_{IN} \geq V_{OUT}$ + 1.62 V, V_{BIAS} must be an independent supply. $V_{BIAS} = V_{IN}$ + 1.62 V = 3.12 V; the system has a 3.3-V rail to use for this supply and also provide some limited headroom for V_{BIAS}. The 5-V rail is a better choice to improve the performance of the LDO, so the 5-V rail is used.

8.2.1.3 Application Curves

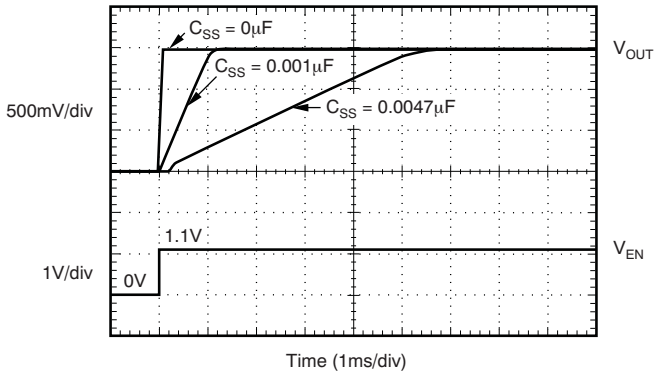


Figure 30. Turn-On Response

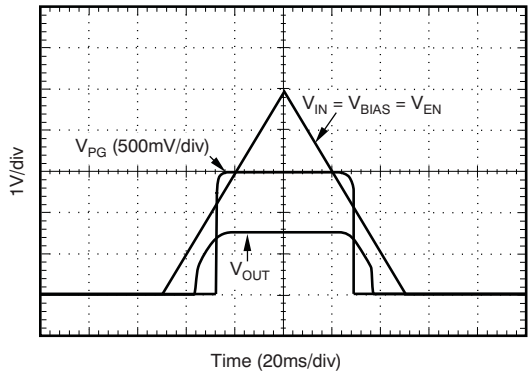


Figure 31. Power-Up/Power-Down

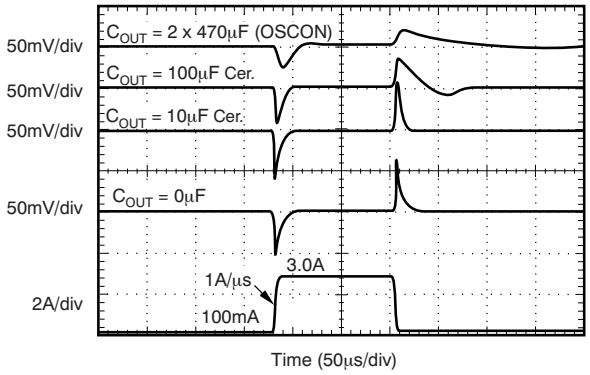


Figure 32. Load Transient Response

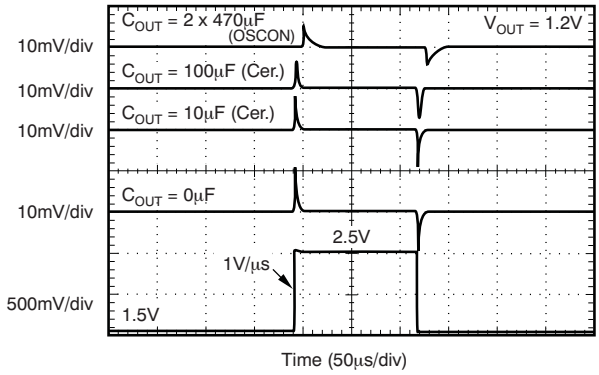


Figure 33. V_{IN} Line Transient (3 A)

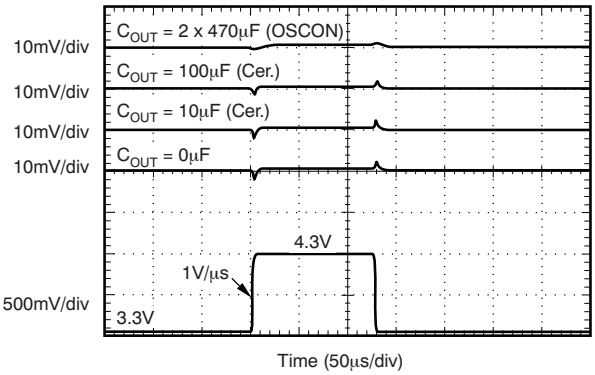


Figure 34. V_{BIAS} Line Transient (3 A)

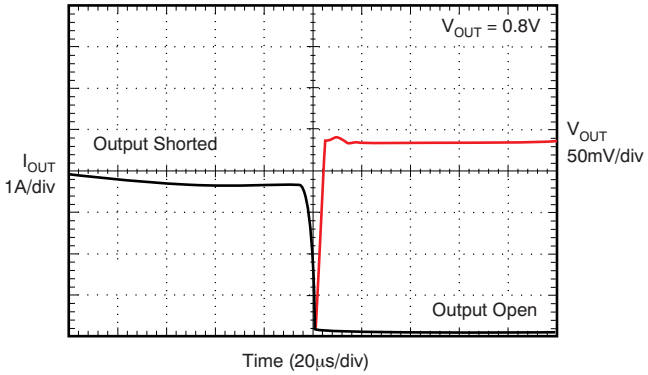


Figure 35. Output Short-Circuit Recovery

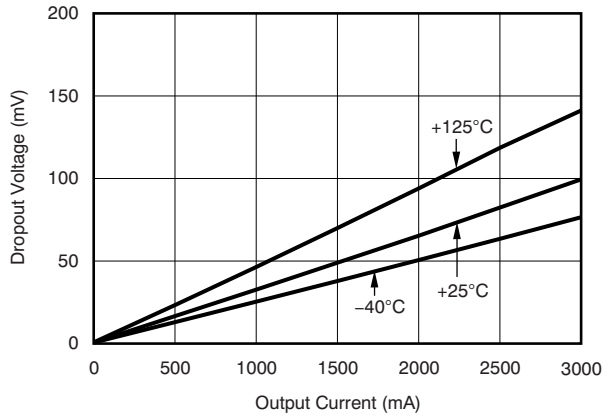


Figure 36. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

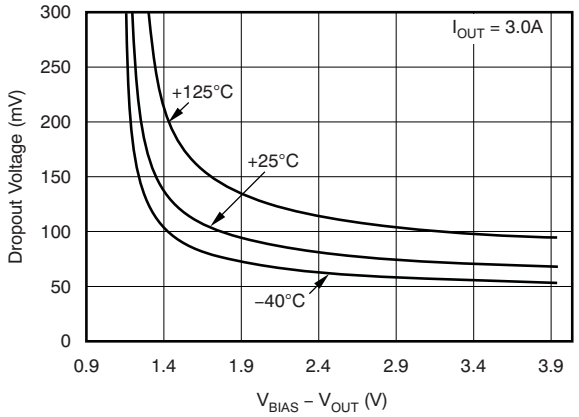


Figure 37. V_{IN} Dropout Voltage vs $V_{BIAS} - V_{OUT}$ and Temperature (T_J)

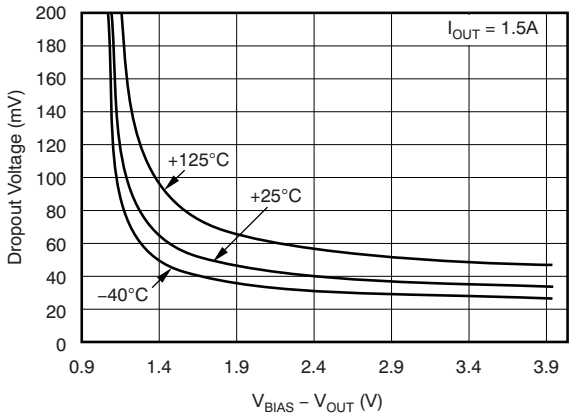


Figure 38. V_{IN} Dropout Voltage vs $V_{BIAS} - V_{OUT}$ and Temperature (T_J)

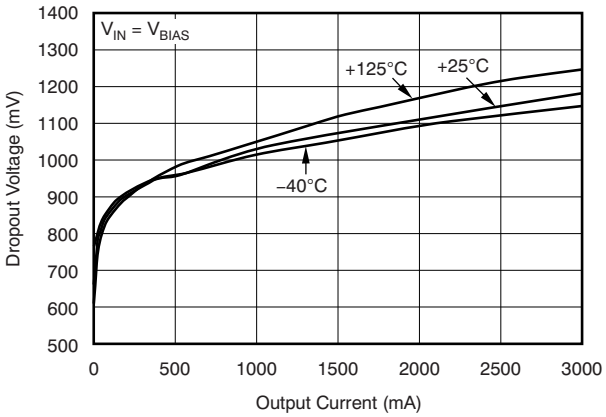


Figure 39. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

8.2.2 Fixed Voltage and Sense Pin

Figure 40 illustrates a typical application circuit for the TPS744xx fixed output device.

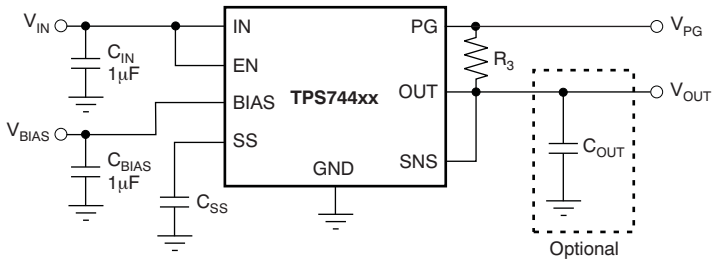


Figure 40. Typical Application Circuit for the TPS744xx (Fixed Voltage)

A fixed voltage version of the TPS744xx has a sense pin (SNS) so that the device can monitor its output voltage at the load device pin(s) as closely as possible. Unlike other TI fixed-voltage LDOs, however, this pin must ***not*** be left floating; it ***must*** be connected to an output node. See the TI application report, *Ultimate Regulation of with Fixed Output Versions of the TPS742xx, TPS743xx, and TPS744xx* (SBVA024), available for download from the TI website.

8.2.3 Using an Auxiliary Bias Rail

Figure 41 illustrates a typical application of the TPS744xx using an auxiliary bias rail. The auxiliary bias rail allows for designer to specify the system to have a low V_{DO}. The bias rail supplies the error amplifier with a higher supply voltage, increasing the voltage that it can apply to the gate of the pass device.

V_{BIAS} must be at least V_{OUT} + 1.62 V.

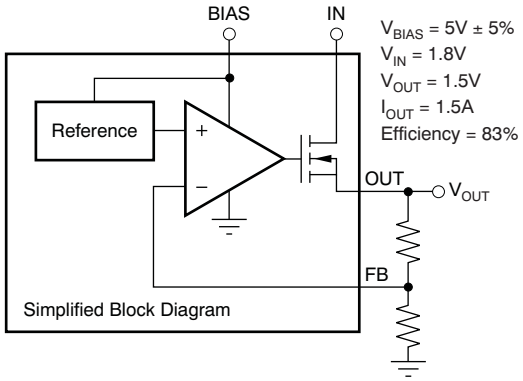


Figure 41. Typical Application of the TPS744xx Using an Auxiliary Bias Rail

8.2.4 Without an Auxiliary Bias

The TPS744xx family is capable of operating without a bias rail if $V_{IN} > V_{OUT} + 1.62$ V. Additional capacitance is advised for this scenario, with at least 4.7 µF of capacitance near the input pin. Figure 42 shows a typical application of the TPS744xx without an auxiliary bias.

If using the TPS744xx in this situation and under high load conditions, ensure that the printed circuit board (PCB) provides adequate thermal handling capabilities to keep the device in its recommended operating range. See *Power Supply Recommendations* for more information.

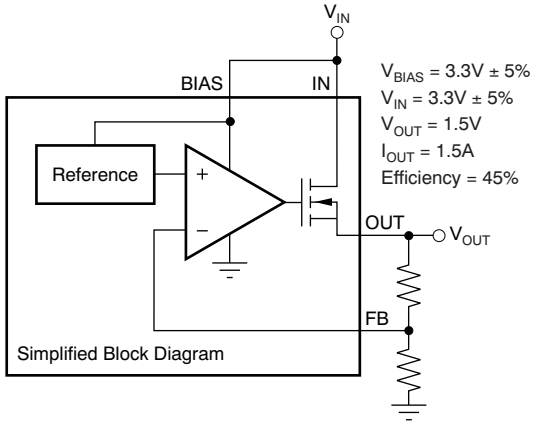


Figure 42. Typical Application of the TPS744xx Without an Auxiliary Bias

9 Power Supply Recommendations

The TPS744 is designed to operate from an input voltage between 1.1 V to 5.5 V, provided the bias rail is at least 1.62 V higher than the input supply. The bias rail and the input supply should both provide adequate headroom and current for the device to operate normally.

Connect a low output impedance power supply directly to the IN pin of the TPS744. This supply must have at least 1-µF of capacitance near the IN pin for stability. A supply with similar requirements should also be connected directly to the bias rail with a separate 1-µF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 29 should be connected as close as possible to the load. If BIAS is connected to IN, it is recommended to connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

10.2 Layout Example

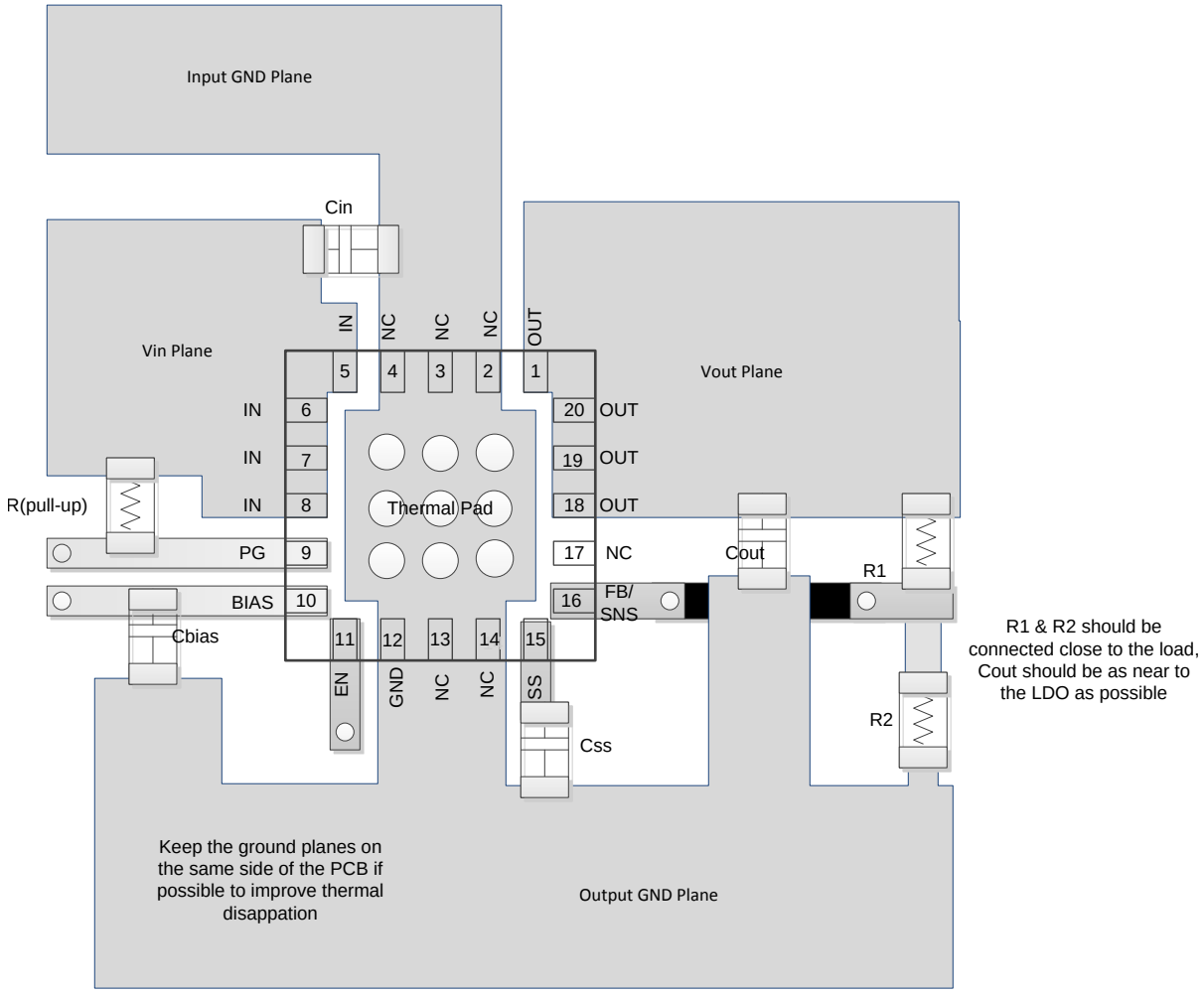


Figure 43. Layout Schematic (RGW Package)

10.3 Thermal Considerations

A better method of estimating the thermal measure comes from using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with corresponding formulas (given in Equation 5).

Thermal Considerations (continued)

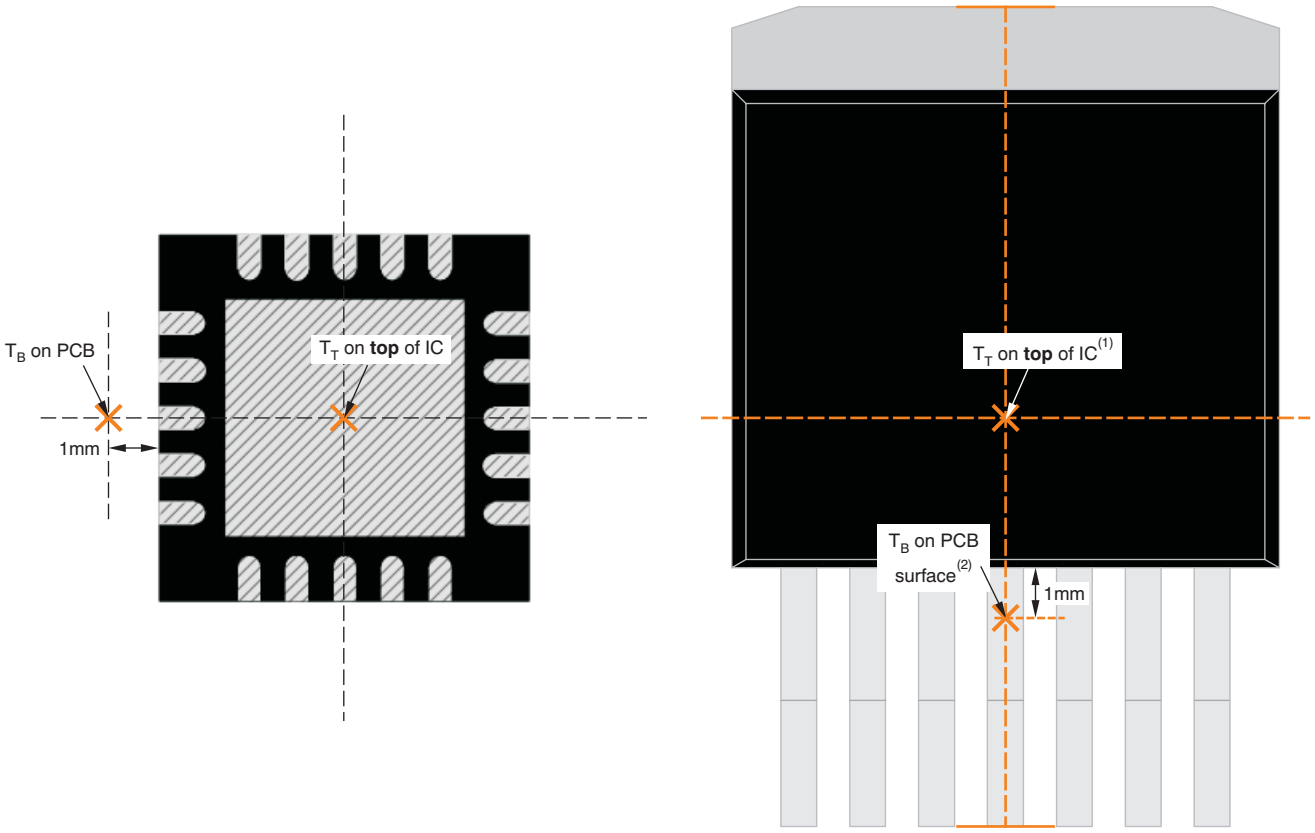
$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{5}$$

Where P_D is the power dissipation shown by Equation 6, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (as Figure 44 shows).

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.



(a) Example RGW (QFN) Package Measurement **(b) Example KTW (DDPAK) Package Measurement**

(1) T_T is measured at the center of both the X- and Y-dimensional axes.

(2) T_B is measured ***below*** the package lead **on the PCB surface**.

Figure 44. Measuring Points for T_T and T_B

Compared with θ_{JA}, the thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size, but they do have a small dependency on board size and layout. Figure 45 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Looking at Figure 45, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point-symmetric to an IC center. In the KTW package, for example (see Figure 44), silicon is not beneath the measuring point of T_T which is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point-symmetry, device heat distribution on the PCB is not point-symmetric, either, so that Ψ_{JB} has a greater dependency on board size and layout.

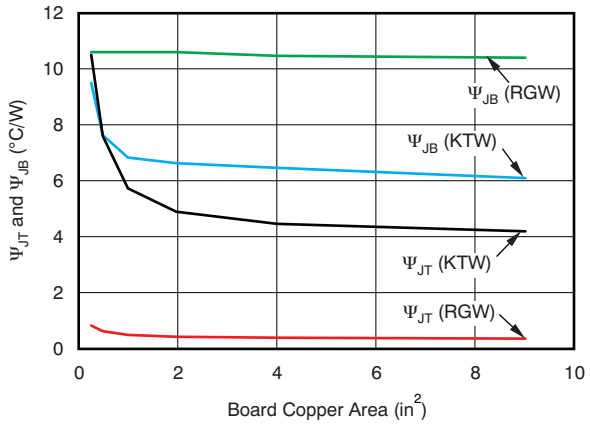


Figure 45. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using θ_{JC},Top to determine thermal characteristics, refer to the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com. Also, refer to the application note *IC Package Thermal Metrics* (SPRA953) (also available on the TI website) for further information.

10.4 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

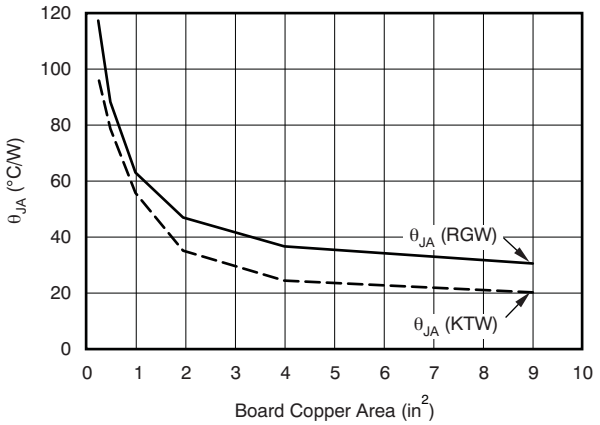
Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the QFN (RGW) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be estimated using Equation 7:

$$R_{\theta JA} = \frac{(+125^\circ C - T_A)}{P_D} \quad (7)$$

Power Dissipation (continued)

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 46.



Note: θ_{JA} value at board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

Figure 46. Θ_{JA} vs Board Size

Figure 46 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in *Estimating Junction Temperature*.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Application report: *Using New Thermal Metrics* (SBVA025)
- Application report: *IC Package Thermal Metrics* (SPRA953)
- Application report: *Ultimate Regulation of with Fixed Output Versions of the TPS742xx, TPS743xx, and TPS744xx* (SBVA024)

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74401KTWR	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	Samples
TPS74401KTWRG3	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	Samples
TPS74401KTWT	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	Samples
TPS74401KTWTG3	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TPS74401	Samples
TPS74401RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples
TPS74401RGWRG4	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples
TPS74401RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples
TPS74401RGWTG4	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS74401 :

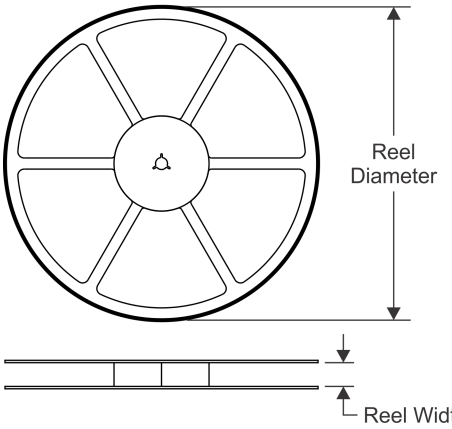
- Enhanced Product: TPS74401-EP

NOTE: Qualified Version Definitions:

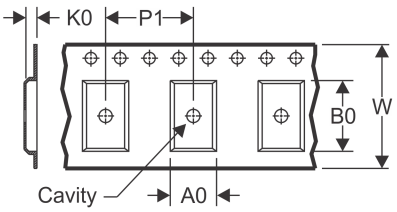
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

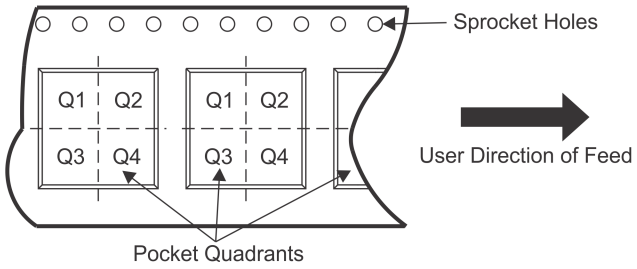


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

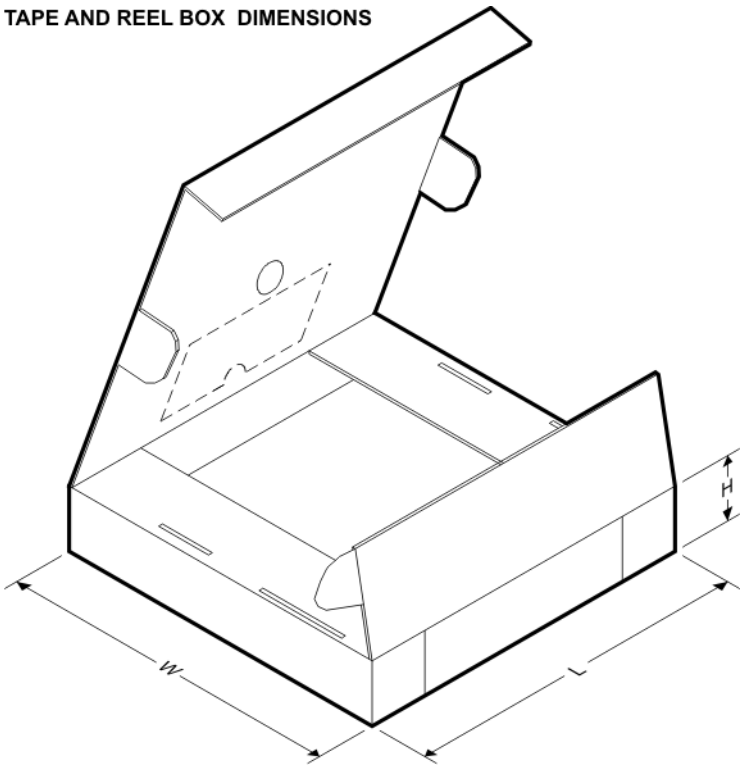
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74401KTWR	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74401KTWT	DDPAK/ TO-263	KTW	7	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74401RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74401RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

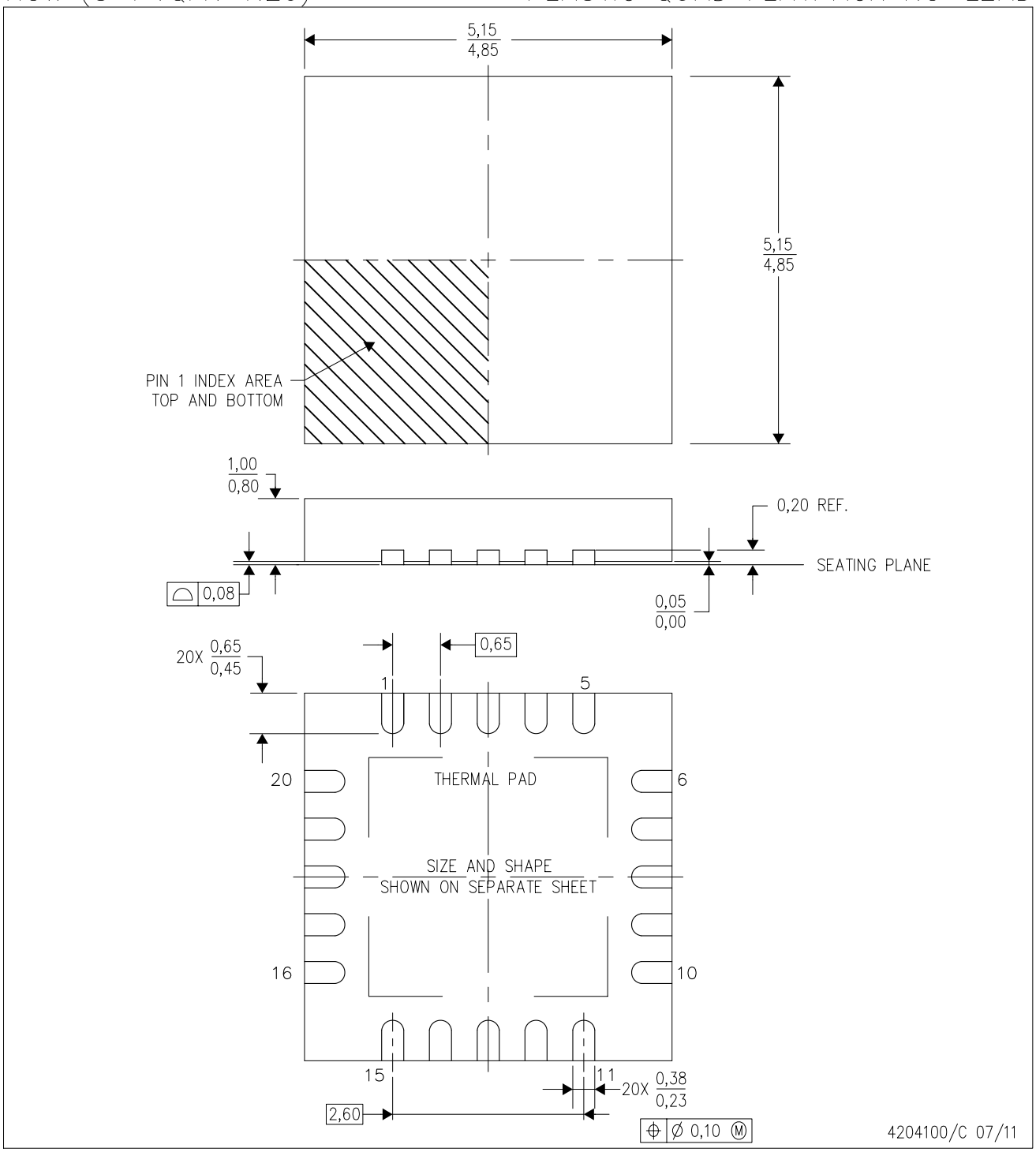
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74401KTWR	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0
TPS74401KTWT	DDPAK/TO-263	KTW	7	50	367.0	367.0	45.0
TPS74401RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74401RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

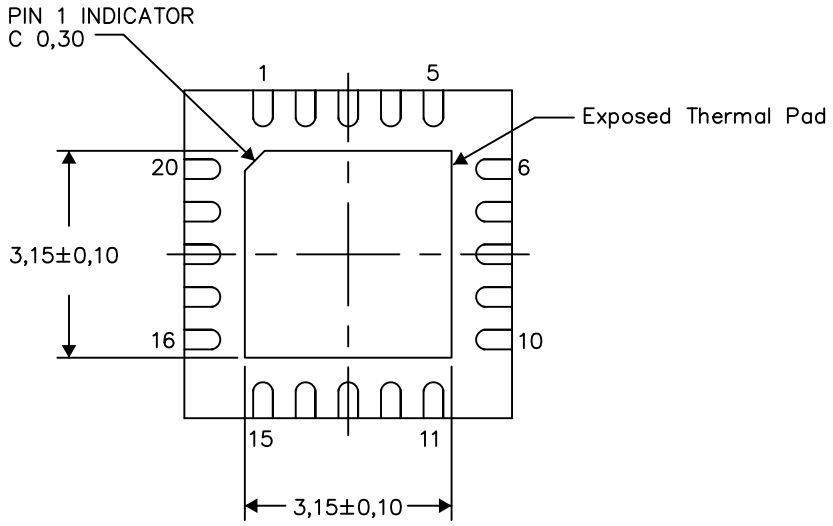
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



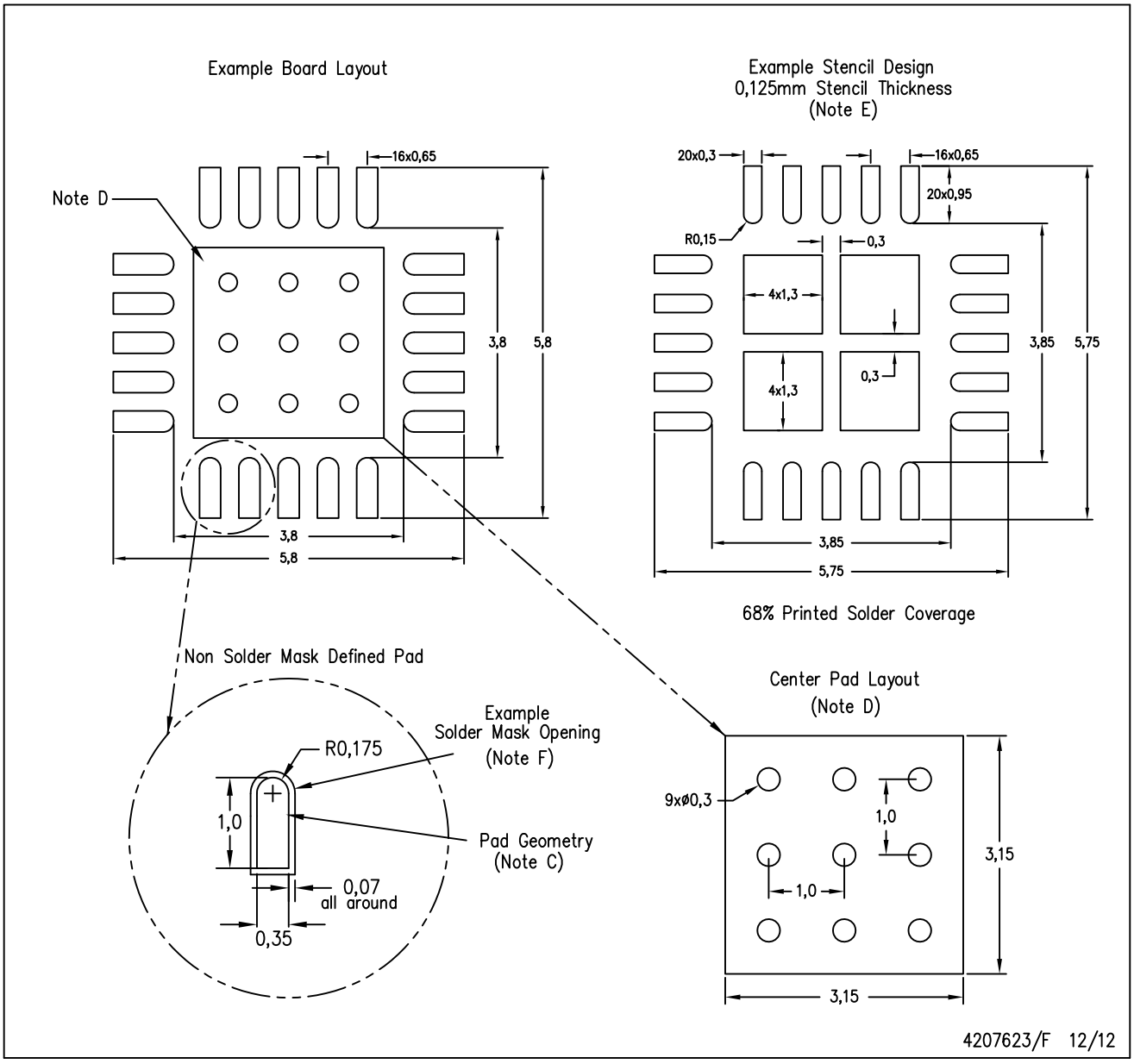
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/K 12/12

NOTE: All linear dimensions are in millimeters

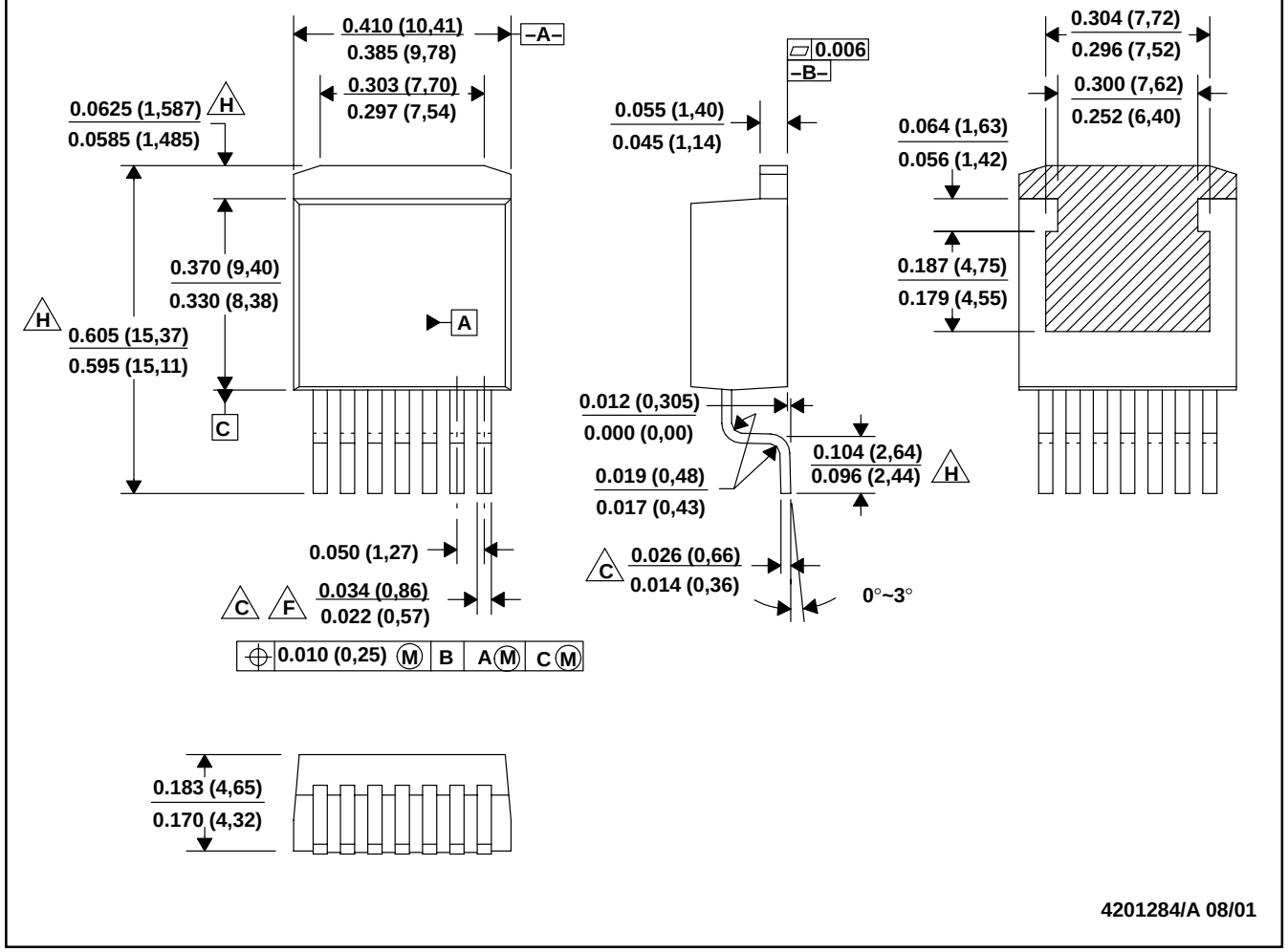
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

MPSF015 – AUGUST 2001

KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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