Document Number: MRF7P20040H
Rev. 2, 12/2010

√RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7P20040HR3
MRF7P20040HSR3

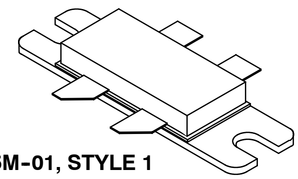
Designed for CDMA base station applications with frequencies from 1800 to 2200 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 32 Volts, I_{DQA} = 150 mA, V_{GSB} = 1.5 Vdc, P_{out} = 10 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

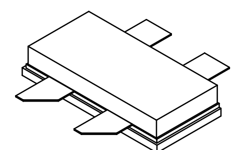
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2025 MHz	18.2	42.6	7.3	-34.8

- Capable of Handling 5:1 VSWR, @ 32 Vdc, 2017.5 MHz, 50 Watts CW (1) Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 3 dB Compression Point ≃ 50 Watts CW (1)

2010-2025 MHz, 10 W AVG., 32 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



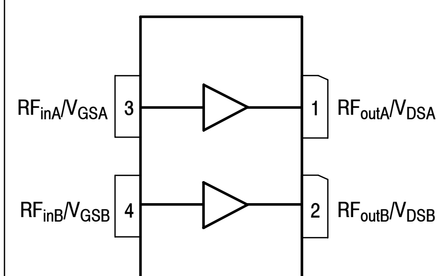
CASE 465M-01, STYLE 1
NI-780-4
MRF7P20040HR3



CASE 465H-02, STYLE 1
NI-780S-4
MRF7P20040HSR3

Features

- Production Tested in a Symmetrical Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel. For R5 Tape and Reel option, see p. 15.



(Top View)

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (2,3)	T_J	225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	42.4 0.17	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (3,4)	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 10 W CW, 32 Vdc, I_{DQA} = 150 mA, V_{GSB} = 1.5 Vdc, 2017.5 MHz Case Temperature 82°C, 40 W CW(1), 32 Vdc, I_{DQA} = 150 mA, V_{GSB} = 1.5 Vdc, 2017.5 MHz	$R_{\theta JC}$	 2.11 1.50	°C/W

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/-Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	B (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics [1]					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 33.5 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 32 Vdc, I_{DA} = 150 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	2.7	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.325 Adc)	$V_{DS(on)}$	0.1	0.24	0.3	Vdc
Functional Tests [2,3] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 32 Vdc, I_{DQA} = 150 mA, V_{GSB} = 1.5 Vdc, P_{out} = 10 W Avg., f = 2025 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16	18.2	21	dB
Drain Efficiency	η_D	39	42.6	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.9	7.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	-34.8	-30	dBc
Input Return Loss	IRL	—	-17.8	-10	dB
Typical Performance [3] (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 32 Vdc, I_{DQA} = 150 mA, V_{GSB} = 1.5 Vdc, 2010-2025 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	35	—	W
P_{out} @ 3 dB Compression Point, CW [4]	P3dB	—	50	—	W
IMD Symmetry @ 15 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	8	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 15 MHz Bandwidth @ P_{out} = 10 W Avg.	G_F	—	0.04	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.013	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) [4]	ΔP1dB	—	0.006	—	dB/°C

1. Each side of device measured separately.
2. Part internally matched both on input and output.
3. Measurement made with device in a Symmetrical Doherty configuration.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

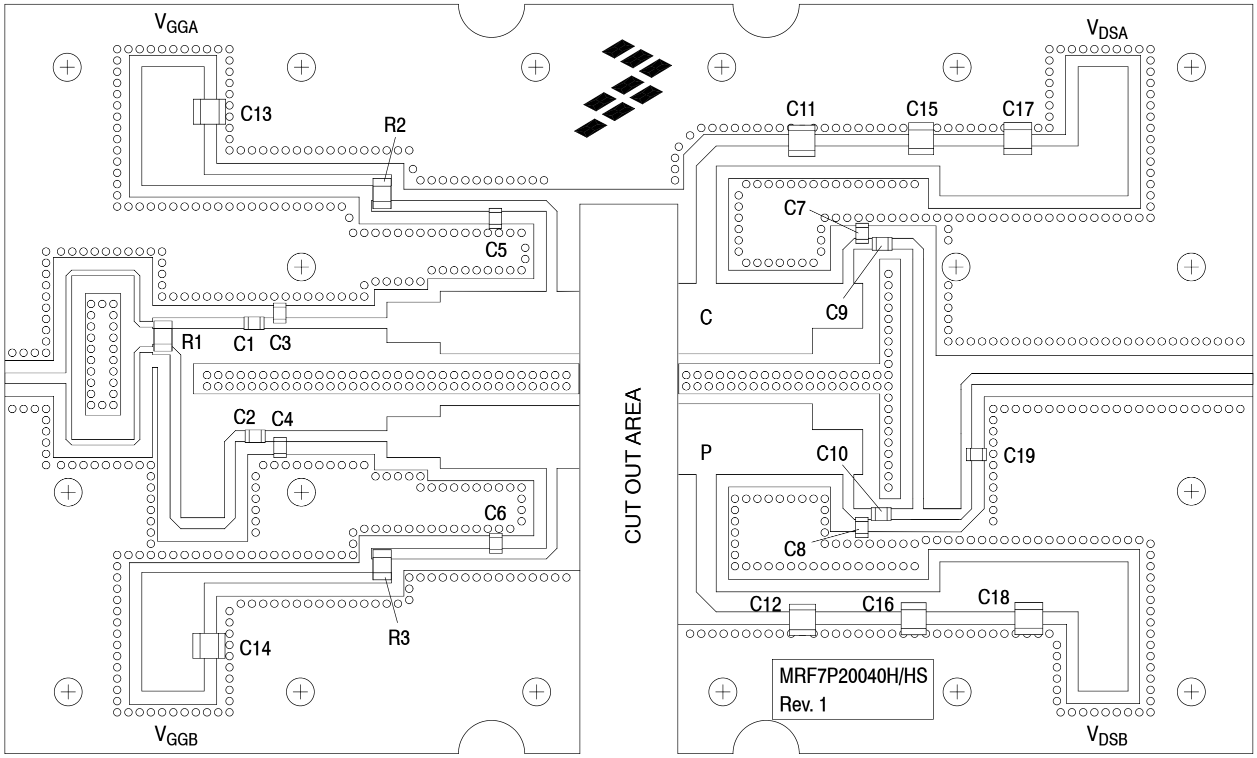


Figure 2. MRF7P20040HR3(HSR3) Test Circuit Component Layout

Table 5. MRF7P20040HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C9, C10	12 pF Chip Capacitors	ATC600F120FT250XT	ATC
C3, C4	2.4 pF Chip Capacitors	ATC600F2R4AT250XT	ATC
C5, C6	27 pF Chip Capacitors	ATC600F270FT250XT	ATC
C7, C8	1.1 pF Chip Capacitors	ATC600F1R1AT250XT	ATC
C11, C12	12 pF Chip Capacitors	ATC100B120FT1500XT	ATC
C13, C14	2.2 μF, 50 V Chip Capacitors	C3225X7R1H225KT	TDK
C15, C16	4.7 μF, 50 V Chip Capacitors	GRM43ER61H475MA88L	Murata
C17, C18	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C19	0.8 pF Chip Capacitor	ATC600F0R8AT250XT	ATC
R1	100 Ω, 1/4 W Chip Resistor	CRCW12061000FKEA	Vishay
R2, R3	12 Ω, 1/4 W Chip Resistors	CRCW120612R0FKEA	Vishay
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

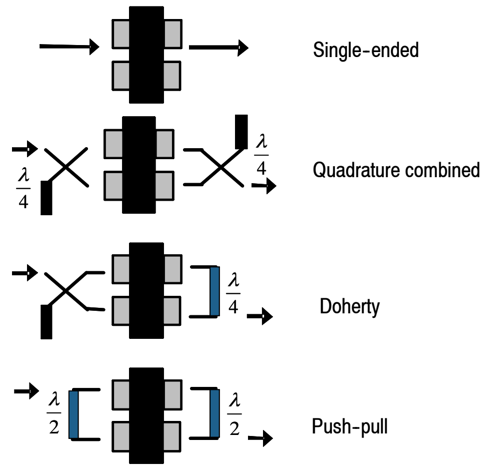


Figure 3. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

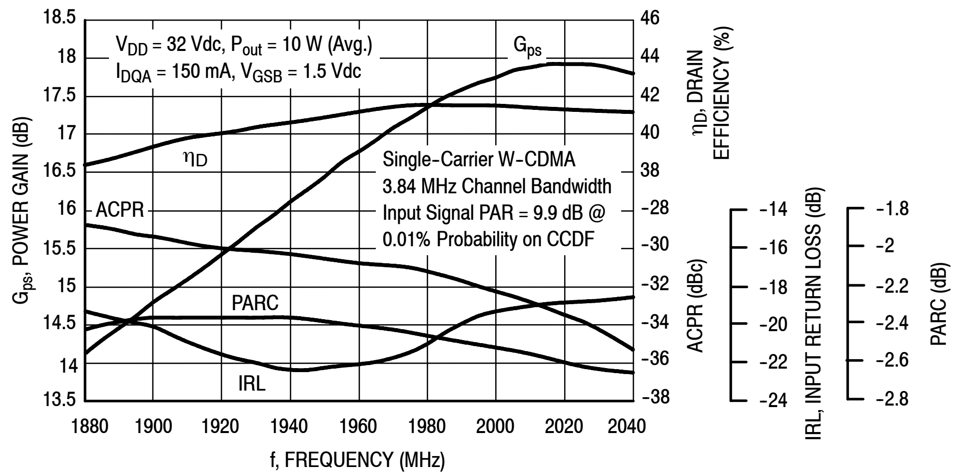


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 10 Watts Avg.

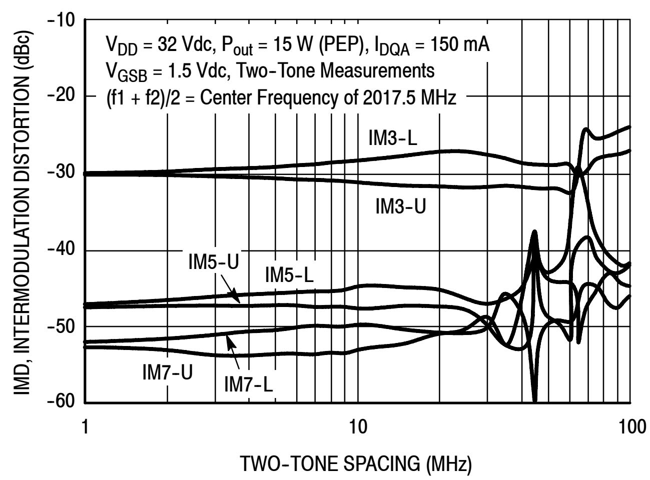


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

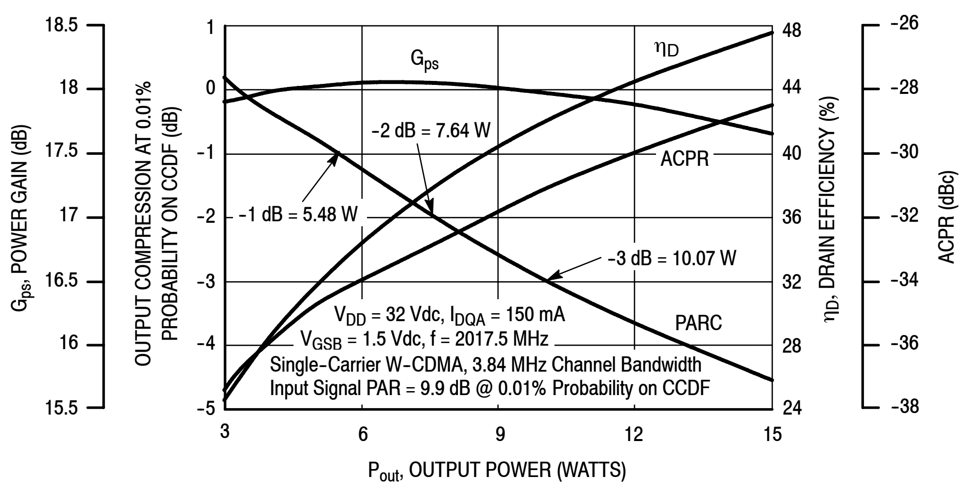


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

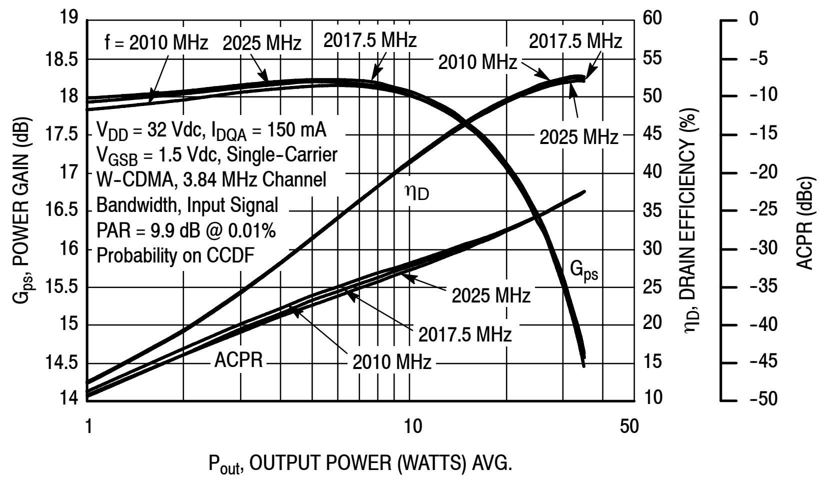


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

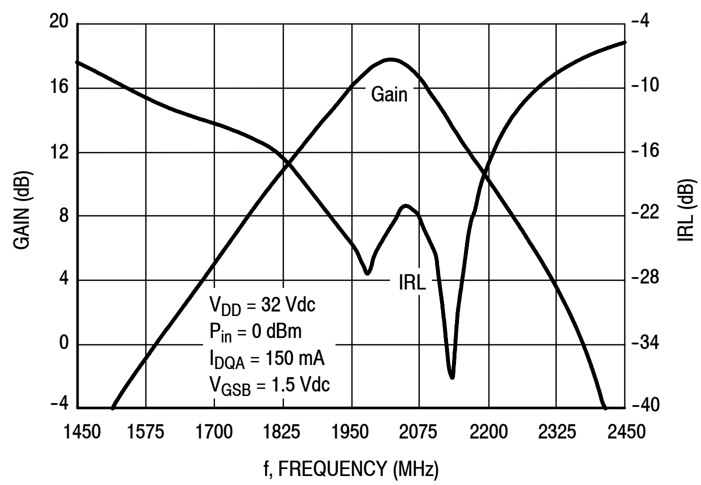


Figure 8. Broadband Frequency Response

W-CDMA TEST SIGNAL

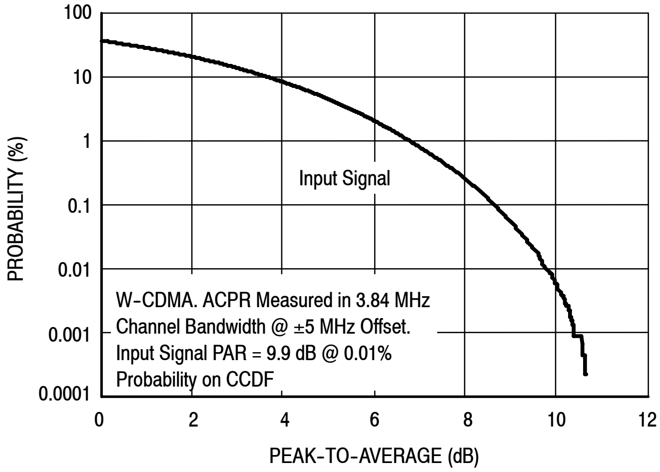


Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

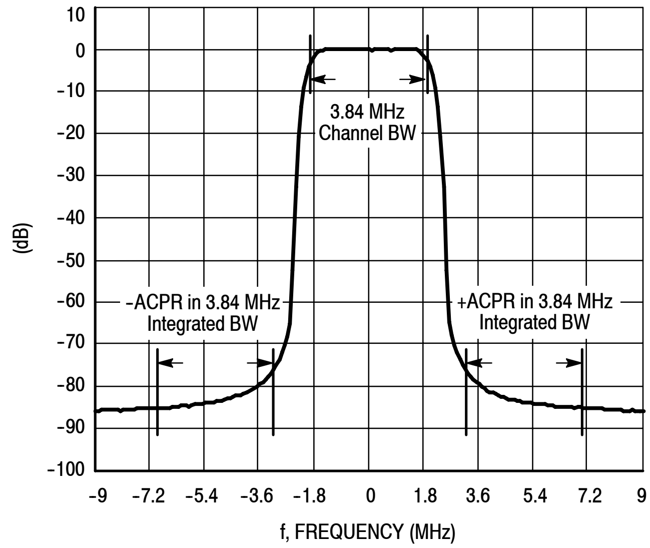


Figure 10. Single-Carrier W-CDMA Spectrum

V_{DD} = 32 Vdc, I_{DQA} = 150 mA, V_{GSB} = 1.5 Vdc, P_{out} = 10 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1995	6.80 - j13.11	14.67 + j4.09
2000	6.66 - j13.03	14.87+ j3.82
2005	6.52 - j12.93	15.08 + j3.58
2010	6.37 - j12.85	15.27 + j3.29
2015	6.22 - j12.78	15.45 + j3.00
2020	6.08 - j12.69	15.62 + j2.77
2025	5.94 - j12.60	15.80 + j2.44
2030	5.80 - j12.49	15.95 + j2.14
2035	5.65 - j12.40	16.08 + j1.82

Note: Measured with Peaking side open.

Z_{load} = Test circuit impedance as measured from drain to ground.

Z_{source} = Test circuit impedance as measured from gate to ground.

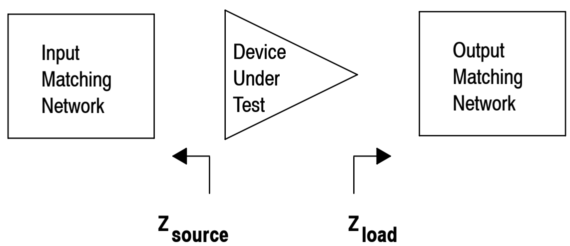


Figure 11. Series Equivalent Source and Load Impedance — Carrier Side

V_{DD} = 32 Vdc, I_{DQA} = 150 mA, V_{GSB} = 1.5 Vdc, P_{out} = 10 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
1995	8.45 - j12.85	5.83 - j10.09
2000	8.28 - j12.79	5.57 - j10.11
2005	8.11 - j12.70	5.32 - j10.08
2010	7.95 - j12.63	5.06 - j10.07
2015	7.79 - j12.56	4.80 - j10.06
2020	7.63 - j12.48	4.55 - j10.01
2025	7.50 - j12.40	4.32 - j9.96
2030	7.34 - j12.32	4.06 - j9.88
2035	7.19 - j12.24	3.82 - j9.81

Note: Measured with Carrier side open.

Z_{load} = Test circuit impedance as measured from drain to ground.

Z_{source} = Test circuit impedance as measured from gate to ground.

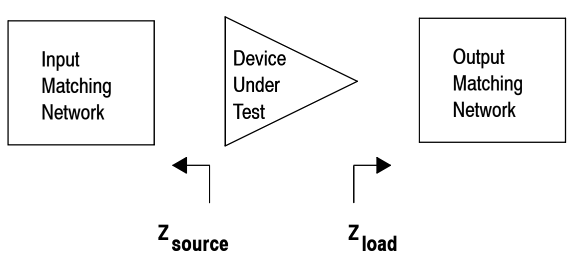
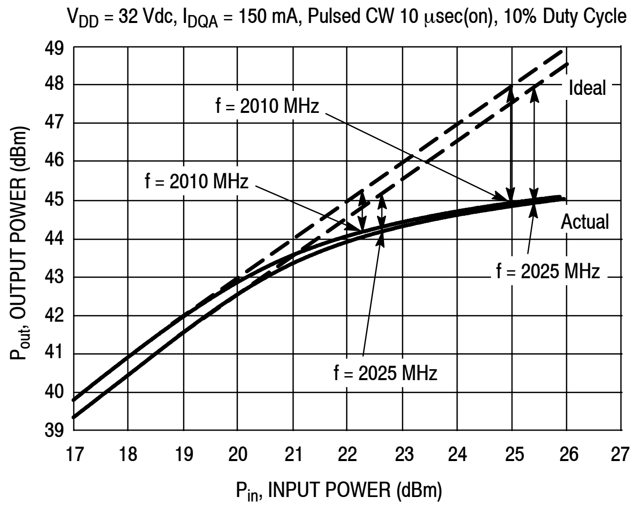


Figure 12. Series Equivalent Source and Load Impedance — Peaking Side

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 32 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
2010	26	44.1	31	44.9
2025	26	44.2	31	44.9

Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
2010	P1dB	2.49 – j18.56	15.82 – j0.28
2025	P1dB	2.66 – j19.78	15.78 + j0.52

Figure 13. Pulsed CW Output Power versus Input Power @ 32 V

NOTE: Measurement made on the Class AB, carrier side of the device.

V_{DD} = 28 Vdc, I_{DQA} = 150 mA

f MHz	Max P_{out} (1)		Z_{source} Ω	Z_{load} Ω
	Watts	dBm		
1805	35	45.4	2.2 – j9.3	17.1 – j7.9
1880	35	45.5	2.3 – j11.3	14.0 – j4.2
1930	35	45.5	2.4 – j13.0	14.7 – j5.9
2025	35	45.5	3.5 – j17.3	15.5 – j8.0
2110	34	45.3	3.8 – j20.6	15.4 – j9.3
2200	35	45.5	5.6 – j25.8	14.4 – j9.4

(1) Maximum output power measurement reflects pulsed 3 dB gain compression.

Z_{source} = Test circuit impedance as measured from gate contact to ground.

Z_{load} = Test circuit impedance as measured from drain contact to ground.

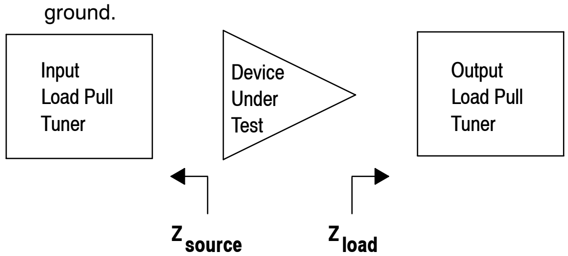


Figure 14. Carrier Side Load Pull Performance — Maximum P3dB Tuning

V_{DD} = 28 Vdc, I_{DQA} = 150 mA

f MHz	Max Eff. (1) %	Z_{source} Ω	Z_{load} Ω
1805	66.6	2.2 – j9.3	17.6 + j9.5
1880	70.1	2.3 – j11.3	16.1 + j9.8
1930	69.8	2.4 – j13.0	14.2 + j8.9
2025	67.7	3.5 – j17.3	13.8 + j6.2
2110	67.9	3.8 – j20.6	11.5 + j3.9
2200	70.3	5.6 – j25.8	9.6 – j0.6

(1) Maximum efficiency measurement reflects pulsed 3 dB gain compression.

Z_{source} = Test circuit impedance as measured from gate contact to ground.

Z_{load} = Test circuit impedance as measured from drain contact to ground.

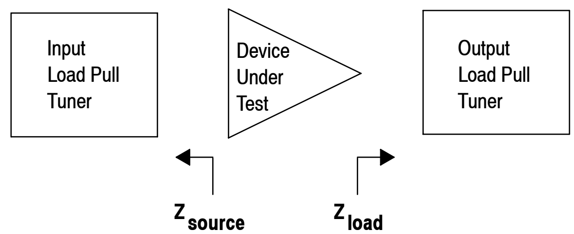
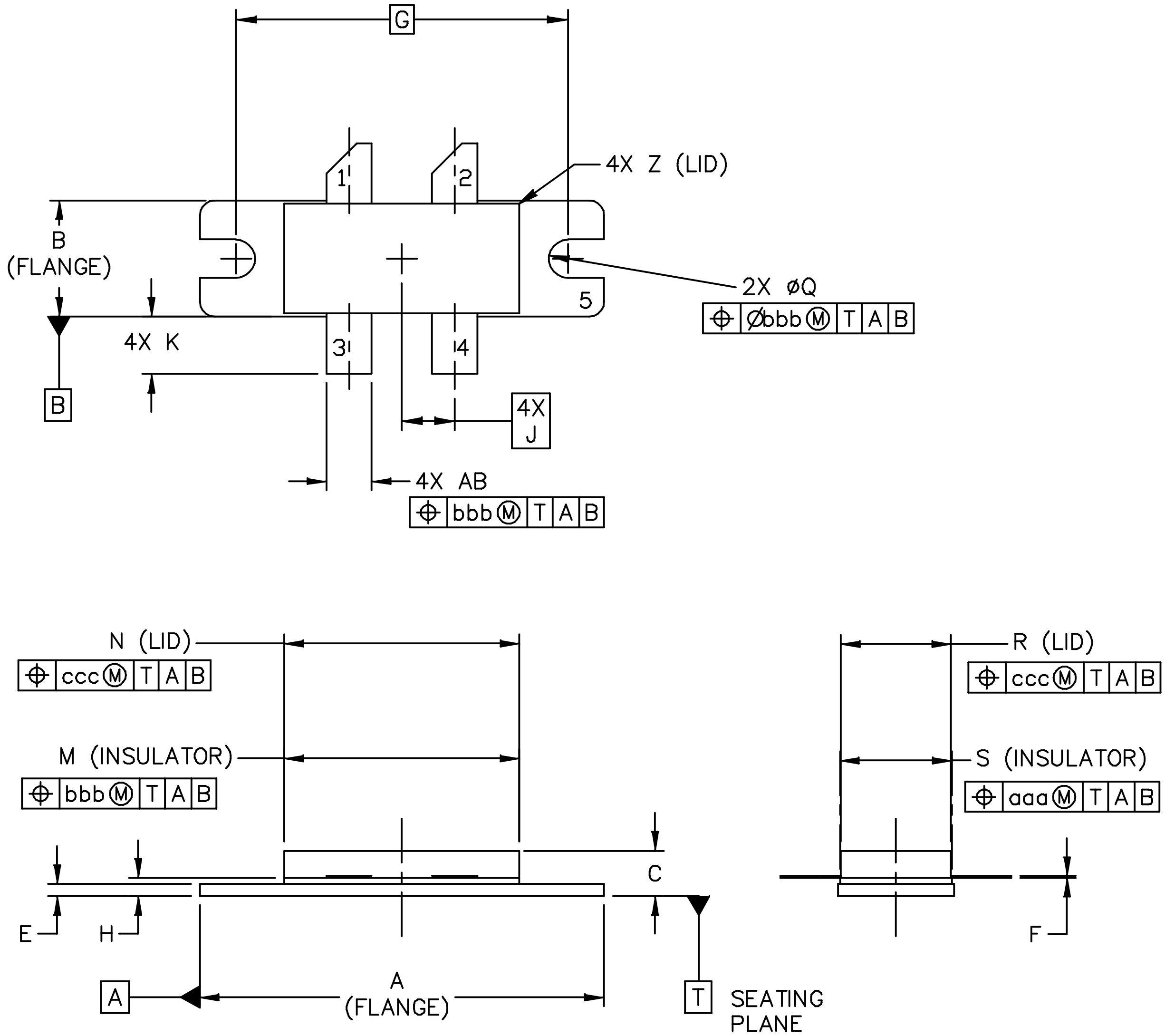


Figure 15. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

PACKAGE DIMENSIONS



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	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH.

3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	U		.040		1.02
E	.035	.045	0.89	1.14	Z		.030		0.76
F	.003	.006	0.08	0.15	AB	.145	.155	3.68	3.94
G	1.100 BSC		27.94 BSC						
H	.057	.067	1.45	1.7	aaa	.005		0.127	
J	.175 BSC		4.44 BSC		bbb	.010		0.254	
K	.170	.210	4.32	5.33	ccc	.015		0.381	
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
Q	⌀.118	⌀.138	⌀3	⌀3.51					

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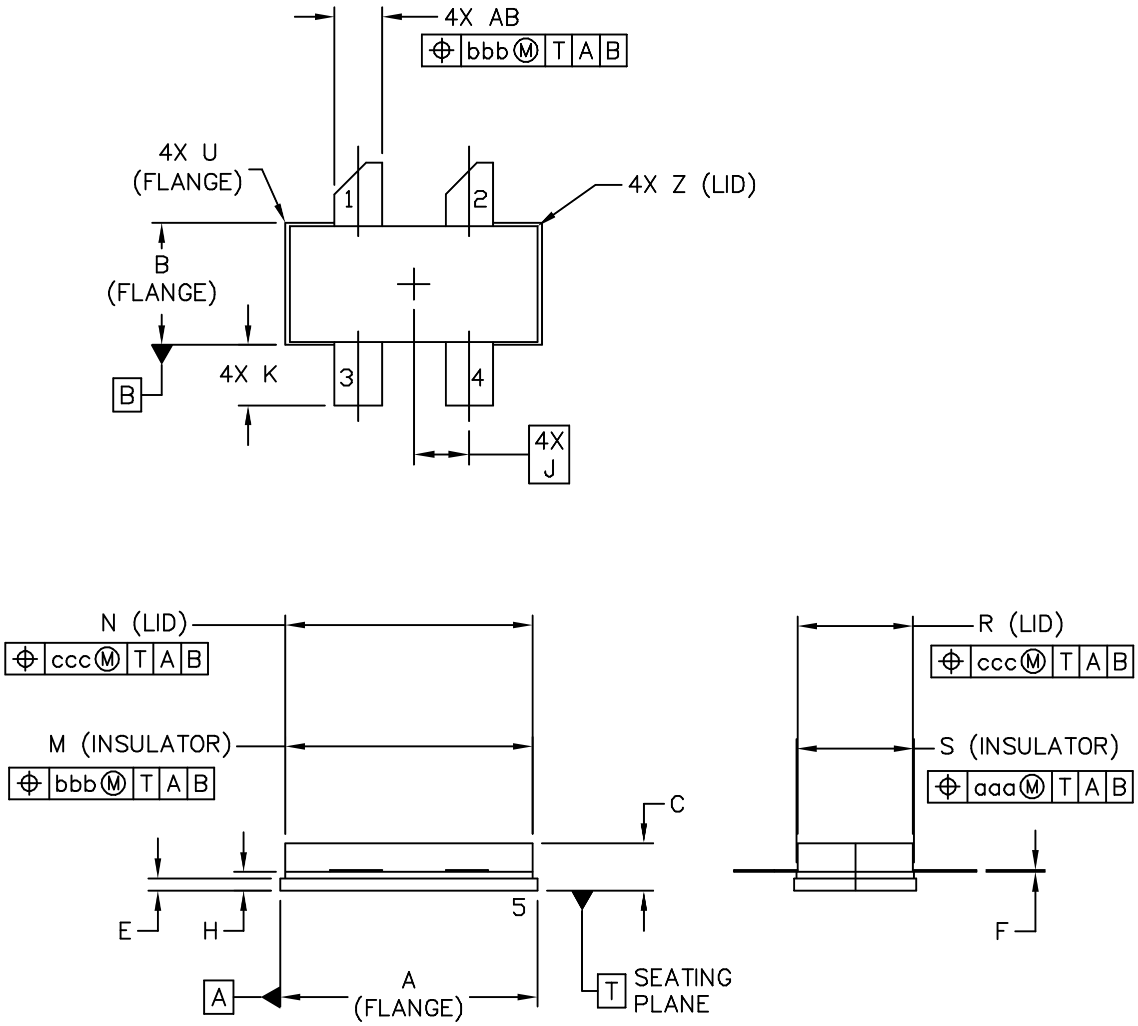
	CASE NUMBER: 465M-01	27 MAR 2007
	STANDARD: NON-JEDEC	



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	CASE NUMBER: 465H–02	27 MAR 2007
	STANDARD: NON–JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH.

3. DELETED

4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68	3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa	.005		0.127	
H	.057	.067	1.45	1.7	bbb	.010		0.254	
J	.175 BSC		4.44 BSC		ccc	.015		0.381	
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					

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TITLE: NI 780S-4	DOCUMENT NO: 98ASA10718D	REV: A
	CASE NUMBER: 465H-02	27 MAR 2007
	STANDARD: NON-JEDEC	

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

R5 Suffix = 50 Units, 56 mm Tape Width, 13 inch Reel.

The R5 tape and reel option for MRF7P20040H and MRF7P20040HS parts will be available for 2 years after release of MRF7P20040H and MRF7P20040HS. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased these devices in the R5 tape and reel option will be offered MRF7P20040H and MRF7P20040HS in the R3 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2009	• Initial Release of Data Sheet
1	Aug. 2009	• Removed IQ Magnitude Clipping from Typical Performance bullet, p. 1 and Functional Test header, p. 2 • Electrical Characteristics, DC tests: updated footnote to indicate each side of device measured separately, p. 2
2	Dec. 2010	• Updated frequency in overview paragraph from "2010 to 2025 MHz" to "1800 to 2200 MHz" per expanded load pull characterization shown in Fig. 14, Carrier Side Load Pull Performance — Maximum P3dB Tuning and Fig. 15, Carrier Side Load Pull Performance — Maximum Efficiency Tuning, p. 1 • Added CW Operation information to Maximum Ratings table, p. 1 • In Table 2, Thermal Characteristics, P_{out} = 10 W CW thermal resistance values changed from I_{DQA} 2.5/V_{GSB} 2.9 to 2.11°C/W and P_{out} = 40 W CW thermal resistance value changed from 2.3 to 1.50°C/W. Thermal values now reflect the use of the combined dissipated power from the carrier amplifier and peaking amplifier, p. 1 • Added Fig. 14, Carrier Side Load Pull Performance — Maximum P3dB Tuning and Fig. 15, Carrier Side Load Pull Performance — Maximum Efficiency Tuning to show load pull data for expanded frequency range presented in p. 1 overview paragraph, p. 10

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