# **Octal 3-State Noninverting Bus Transceiver**

# **High-Performance Silicon-Gate CMOS**

The MC74HC245A is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

The HC245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

#### **Features**

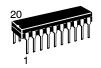
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard
- Chip Complexity: 308 FETs or 77 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



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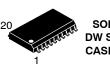
http://onsemi.com

#### **MARKING DIAGRAMS**

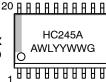


PDIP-20 **N SUFFIX CASE 738** 

MC74HC245AN **AWLYYWWG** 

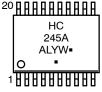


SOIC-20 **DW SUFFIX** CASE 751D





TSSOP-20 **DT SUFFIX** CASE 948E





SOEIAJ-20 **F SUFFIX CASE 967** 

<sup>20</sup><u>лппппппп</u> 74HC245A **AWLYWWG** 

= Assembly Location

= Wafer Lot WL. L YY, Y = Year WW, W = Work Week = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

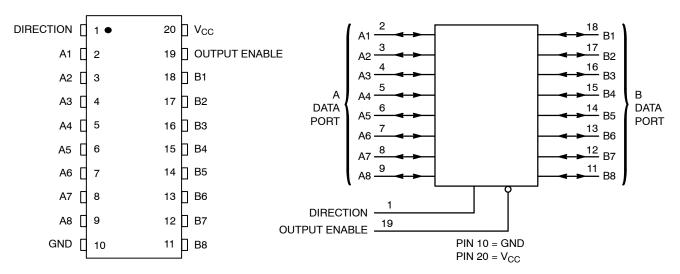


Figure 1. Pin Assignment

Figure 2. Logic Diagram

#### **FUNCTION TABLE**

Contro	I Inputs	
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	Н	Data Transmitted from Bus A to Bus B
Н	Х	Buses Isolated (High-Impedance State)

X = don't care

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74HC245ANG	PDIP-20 (Pb-Free)	18 Units / Rail
MC74HC245ADWG	SOIC-20 WIDE (Pb-Free)	38 Units / Rail
MC74HC245ADWR2G	SOIC-20 WIDE (Pb-Free)	1000 Tape & Reel
MC74HC245ADTG	TSSOP-20	75 Units / Rail
NLV74HC245ADTG*	(Pb-Free)	
MC74HC245ADTR2G	TSSOP-20	2500 Tape & Reel
NLV74HC245ADTR2G*	(Pb-Free)	
MC74HC245AFG	SOEIAJ-20 (Pb-Free)	40 Units / Rail
MC74HC245AFELG	SOEIAJ-20 (Pb-Free)	2000 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

#### MAXIMUM RATINGS (Note 1)

Symbol	F	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5  to  +7.0	V
V <sub>IN</sub>	DC Input Voltage		$-0.5$ to $V_{CC}$ $+0.5$	V
V <sub>OUT</sub>	DC Output Voltage	(Note 2)	$-0.5$ to $V_{CC}$ $+0.5$	V
I <sub>IK</sub>	DC Input Diode Current		±20	mA
I <sub>OK</sub>	DC Output Diode Current		±35	mA
I <sub>OUT</sub>	DC Output Sink Current		±35	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin		±75	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin		±75	mA
T <sub>STG</sub>	Storage Temperature Range		-65  to  +150	°C
TL	Lead Temperature, 1 mm from Case t	for 10 Seconds	260	°C
TJ	Junction Temperature Under Bias		+150	°C
$\theta_{\sf JA}$	Thermal Resistance	PDIP SOIC TSSOP	67 96 128	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 30% to 35%	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 > 1000	V
I <sub>LATCHUP</sub>	Latchup Performance	Above V <sub>CC</sub> and Below GND at 85°C (Note 6)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow.
- I<sub>O</sub> absolute maximum rating must observed.
   Tested to EIA/JESD22-A114-A.
- Tested to EIA/JESD22-A115-A.
   Tested to JESD22-C101-A.
- 6. Tested to EIA/JESD78.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	<b>–</b> 55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time $V_{CC}$ = 2.0 V (Figure 3) $V_{CC}$ = 4.5 V $V_{CC}$ = 6.0 V	0 0 0	1000 500 400	ns

### DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gu	aranteed Li	mit	
	_		V <sub>CC</sub>	-55 to		_	
Symbol	Parameter	Test Conditions	V	25°C	≤ 85°C	≤ 125°C	Unit
$V_{IH}$	Minimum High-Level Input Voltage	$ \begin{vmatrix} V_{out} = V_{CC} - 0.1 \text{ V} \\  I_{out}  \leq 20 \mu\text{A} \end{vmatrix} $	2.0 3.0	1.5 2.1	1.5 2.1	1.5 2.1	V
		Four = 20 ps.	4.5 6.0	3.15 4.2	3.15 4.2	3.15 4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V}$ $ I_{out}  \le 20  \mu\text{A}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$ \begin{aligned} &V_{in} = V_{IH} \\ & I_{out}  \leq 20 \; \mu A \end{aligned} $	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$ \begin{aligned} V_{in} = V_{IH} & \mid I_{out} \mid \leq 2.4 \text{ mA} \\ \mid I_{out} \mid \leq 6.0 \text{ mA} \\ \mid I_{out} \mid \leq 7.8 \text{ mA} \end{aligned} $	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$ \begin{aligned} &V_{in} = V_{IL} \\ & I_{out}  \leq 20 \; \mu A \end{aligned} $	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$ \begin{vmatrix} V_{in} = V_{IL} &  I_{out}  \leq 2.4 \text{ mA} \\  I_{out}  \leq 6.0 \text{ mA} \\  I_{out}  \leq 7.8 \text{ mA} \end{vmatrix} $	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
l <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μΑ
l <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State $V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	6.0	4.0	40	160	μΑ

## AC ELECTRICAL CHARACTERISTICS ( $C_L$ = 50 pF, Input $t_{\rm f}$ = $t_{\rm f}$ = 6 ns)

			Guaranteed Limit			
Symbol	Parameter	V <sub>CC</sub> V	–55 to 25°C	≤ <b>85</b> °C	≤ 125°C	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0 3.0 4.5 6.0	75 55 15 13	95 70 19 16	110 80 22 19	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 90 22 19	140 110 28 24	165 130 33 28	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to A or B (Figures 2 and 4)	2.0 3.0 4.5 6.0	110 90 22 19	140 110 28 24	165 130 33 28	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C <sub>in</sub>	Maximum Input Capacitance (Pin 1 or Pin 19)	-	10	10	10	pF
C <sub>out</sub>	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	_	15	15	15	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
$C_{PD}$	Power Dissipation Capacitance (Per Transceiver Channel) (Note 7)	40	pF

<sup>7.</sup> Used to determine the no–load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

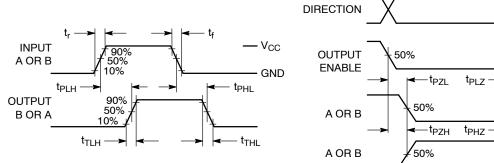


Figure 3. Switching Waveform

HIGH IMPEDANCE

 $V_{CC}$ 

 $\begin{array}{c} \text{GND} \\ \text{V}_{\text{CC}} \end{array}$ 

GND

HIGH

 $V_{\mathsf{OL}}$ 

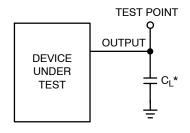
– V<sub>OH</sub>

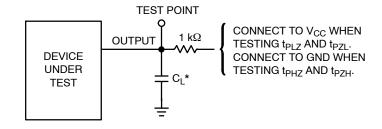
**IMPEDANCE** 

50%

, 10%-

90%-





<sup>\*</sup>Includes all probe and jig capacitance

\*Includes all probe and jig capacitance

Figure 5. Test Circuit

Figure 6. Test Circuit

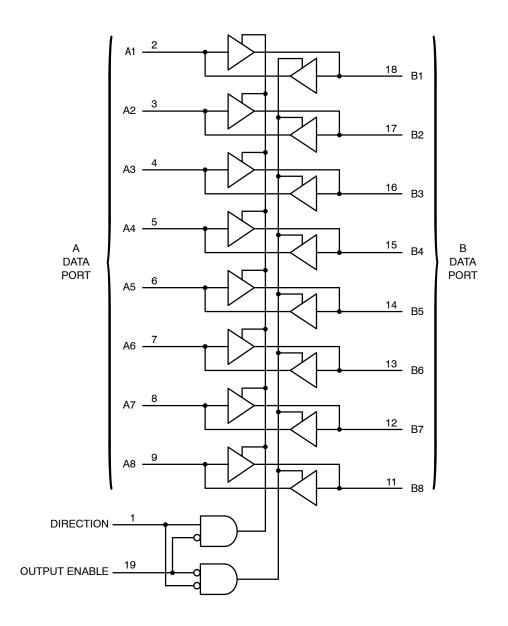
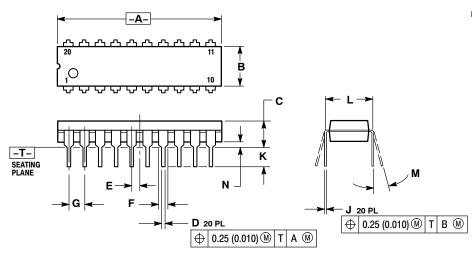


Figure 7. Expanded Logic Diagram

#### **PACKAGE DIMENSIONS**

#### PDIP-20 **N SUFFIX** PLASTIC DIP PACKAGE CASE 738-03 ISSUE E



#### NOTES:

- IOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

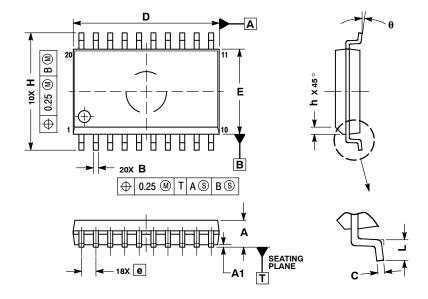
  2. CONTROLLING DIMENSION: INCH.

  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL

  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	1.010	1.070	25.66	27.17
В	0.240	0.260	6.10	6.60
С	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050	BSC	1.27	BSC
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300	BSC	7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

#### SOIC-20 **DW SUFFIX** CASE 751D-05 **ISSUE G**

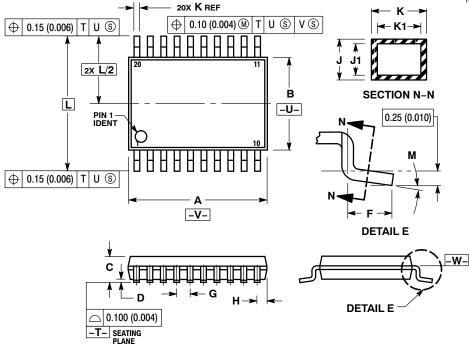


- NOTES:
  1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS				
DIM	MIN	MAX			
Α	2.35	2.65			
A1	0.10	0.25			
В	0.35	0.49			
С	0.23	0.32			
D	12.65	12.95			
Е	7.40	7.60			
е	1.27	BSC			
Н	10.05	10.55			
h	0.25	0.75			
Ĺ	0.50	0.90			
θ	0 °	7 °			

#### **PACKAGE DIMENSIONS**

#### TSSOP-20 **DT SUFFIX** CASE 948E-02 ISSUE C



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION:
  MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE

  - 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.

  - INTERLEAD FLASH OR PROTRUSION.
    INTERLEAD FLASH OR PROTRUSION.
    SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
    5. DIMENSION K DOES NOT INCLUDE
    DAMBAR PROTRUSION. ALLOWABLE
    DAMBAR PROTRUSION SHALL BE 0.08
    (0.003) TOTAL IN EXCESS OF THE K
    DIMENSION AT MAXIMUM MATERIAL
    CONDITION.

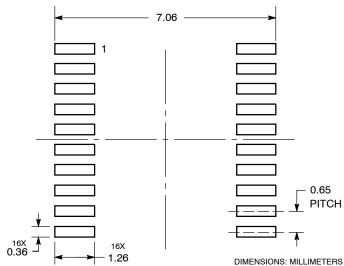
  - CONDITION.

    6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

    7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

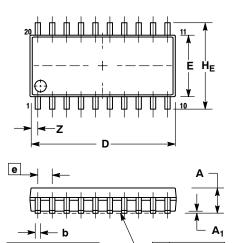
	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	0.65 BSC		BSC	
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0°	8°	

### **SOLDERING FOOTPRINT**



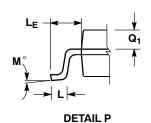
#### PACKAGE DIMENSIONS

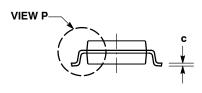
SOEIAJ-20 **F SUFFIX** CASE 967-01 **ISSUE A** 



0.10 (0.004)

0.13 (0.005) M





#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI
- DIMENSIONING AUTO . .
   Y14.5M, 1982.
   CONTROLLING DIMENSION: MILLIMETER.
   DIMENSIONS D AND E DO NOT INCLUDE
   CONTROLLING DIMENSIONS D AND ARE
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15
- (0.006) PER SIDE. I. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER
  RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

	MILLIN	IETERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
Α		2.05		0.081		
A <sub>1</sub>	0.05	0.20	0.002	0.008		
b	0.35	0.50	0.014	0.020		
C	0.15	0.25	0.006	0.010		
D	12.35	12.80	0.486	0.504		
E	5.10	5.45	0.201	0.215		
е	1.27	BSC	0.050	BSC		
HE	7.40	8.20	0.291	0.323		
L	0.50	0.85	0.020	0.033		
LE	1.10	1.50	0.043	0.059		
M	0 °	10°	0°	10°		
$Q_1$	0.70	0.90	0.028	0.035		
Z		0.81		0.032		

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